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D2.1

Design methodology and technologies for multi-mode radio Front-Ends

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Abstract:

The first main target of this task is to investigate the MEMS technology in term of using them for designing re-configurable radios and to build up a sufficient design for using this technology. The LETI does investigation to evaluate the added value of RF-MEMS with respect to system reconfigurability. In this context, a good knowledge of the RF-MEMS state of the art appears to be necessary in order to propose a study that is closely related to what is available, or what will be early available, in term of electronic functions, performances, size and fabrication facilities.

The second main target of this task is to investigate the substrate coupling mechanism. EPFL has focused on the development of methodologies for the analysis and optimization of substrate noise effects in RF mixed-signal circuits. Two methodologies have been elaborated: one for an early design verification, and another one for a final verification/optimization of the noise immunity of the circuits. A new approach, which combines a thorough physical comprehension of the noise coupling effects and accurate 3D substrate modeling tools and significantly accelerates the substrate model extraction and enables the use of the iterative optimization procedure, is proposed.

Keyword list: RF MEMS, substrate coupling, reconfigurability

Abbreviations

MC-CDMA	Multi-carrier CDMA
CDMA	Code Division Multiple Access
FBAR	Film Bulk Acoustic Resonator
RF MEMS	Radio frequency micromechanical systems
Agilent ADS	Agilent Advanced design software
MBVD	Modified Butterworth-Van Dyke
MS-SOC	Mixed-Signal System-On-Chip
EDA	Electronic Design Automation
VCO	Voltage Controlled-Oscillator
CMRR	Common-Mode Rejection Ratio
FDM	Finite-Difference Method

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Introduction

This document is the final version of Deliverable D2.1 "**Design methodologies and technologies for multi-mode radio front-ends**".

This deliverable summarizes the main work done by the LETI and EPFL with respect to Task 2.1: "Methodologies and technologies for ensuring configurability and adaptivity".

The first part of this report is devoted to the RF MEMS aspects (LETI) and the second part to the modeling techniques and verification methodologies for substrate coupling effects in multi-mode RF transceivers (EPFL).

1 MEMS TECHNOLOGY

1.1 RF MEMS in MuMoR Project

Although many studies were developed on RF-MEMS, system manufacturers still feel difficulties to employ them in the RF front-end. Two major reasons lie behind this reality. Firstly, estimation of the impact they could bring is not easy to appreciate. And secondly, few finalized products are available on market. Therefore, the utilization of micromachined components in RF systems stays risky. However, this new family might considerably modify the overall system approach, that's why projects like MuMoR are going to emerge.

Within the MuMoR project, investigations are done to evaluate the added value of RF-MEMS respect to system reconfigurability. In this context, a good knowledge of the RF-MEMS state of the art appears to be necessary in order to propose a study that is closely related to what is available, or what will be early available, in term of electronic functions, performances, size and fabrication facilities. Therefore we published two bibliographies on RF MEMS switches (WP2_leti_in_in_001) and on Film Bulk Acoustic Resonators (WP2_leti_in_in_003). The same kind of study will be soon published on MEMS RF tunable capacitors.

The next step is to develop a library of RF MEMS components and functions and to provide it to system designers to enable them to explore the impact of RF MEMS on front-end circuit designs. In return we await from designers new specifications to drive the technological developments. A first electrical model of a RF MEMS switch was provided to the partners (WP2_Leti_in_in_002), followed by two electrical models of Film Bulk Acoustic resonators (WP2_Leti_in_in_004). This model was used to build FBAR filters for Tx and Rx paths for UMTS. Specifications were provided to LETI by IMST and LETI brought to partners the corresponding models of filters (WP2_Leti_in_in_005) to be used in system level simulations in the Agilent design tool ADS.

We summarize our methodology to study MEMS based architectures in Figure 1-1. The two first steps of the methodology are the development of electrical models based on components fabricated in the LETI or on parameters derived from the literature. The designers will already have at this early stage the possibility to tune the parameters with a degree of freedom dictated by the technological state-of-the-art (box 2). Then, the designers have tools to analyze the impact of RF MEMS on systems, and to imagine new architectures. With the capability of tuning the parameters, they will isolate (box 4) the key parameters to optimize in order to fulfill their new systems requirements. In return, the RF MEMS designers can then simulate the new required components and extract the parameters of an upgraded model (box 5).

This scheme may be re-used several times to reach a level of stability in the MEMS-based systems specifications.

In parallel, we will take into account the progress of the bottom-up approaches (box 6), that is to say the technological developments on RF MEMS devices made in LETI, to get at the end (box7) realistic specifications to drive RF MEMS developments.

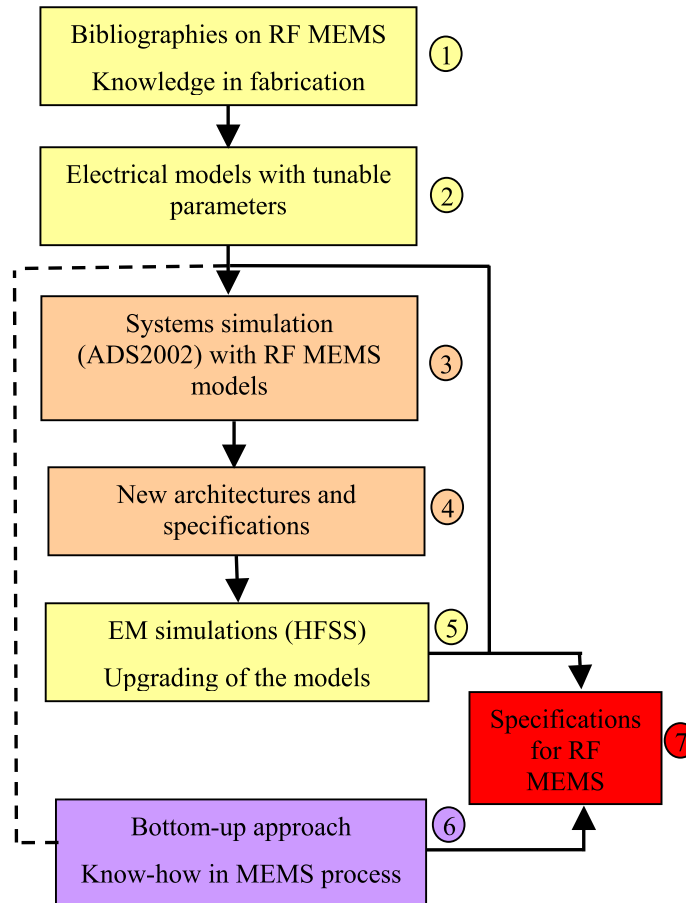


Figure 1-1 : Methodology based on a mixed approach

Additional aspects of this methodology are still under investigations. For instance, do we need to introduce thermo-mechanical effects in our models ? If yes, at which stage ? Do complicated models will slow down the system simulations ? Another question concerns the level of the systems studies : to ensure an overall gain of performance, the specifications of the MEMS-based systems has to deal with the complete system. Although some RF MEMS devices can be considered as RF functions, e.g. switches, others like tunable capacitors, are embedded into subsystems like VCO's. A further effort to model for instance tunable LC filters instead of a simple tunable capacitor will be certainly necessary in order to avoid to overload the designers and to give them useful tools.

1.2 RF MEMS State-of-the-Art

1.2.1 Switches

A bibliography on MEMS switches was published in September 2002, "**Overview of RF MEMS Switches**", WP2_leti_in_in_001. This document aims to different goals:

- To present the latest development in RF micromechanical system (MEMS) switches and the major actors (firms and universities) involved in that field.
- To expose the basic concepts of MEMS switches to a radio-frequency point a view.
- To give a quite exhaustive bibliography on RF MEMS switches.

112 papers were noticed from 1995 to 2002. The idea was to focused on different subjects (listed below) and to give the related basics concepts and the solutions founded in the literature.

The main subjects are :

- **RF performances** : we explained the differences between series and shunt configurations, Figure 1-2, that make the first one more suitable for low frequency applications (dc to 6 GHz) and the second for higher frequencies. We summarized in a table the RF parameters (insertion loss, isolation) for all switches that we noticed. Today, several switches have very small insertion loss, < 0.2 dB through a wide band of frequency (dc to 30 GHz). The isolation depends on the configuration. It can be > 50 dB at 2 GHz (LETI switch, [1]) or > 20 dB from dc to 40 GHz for the switch from Raytheon [2].

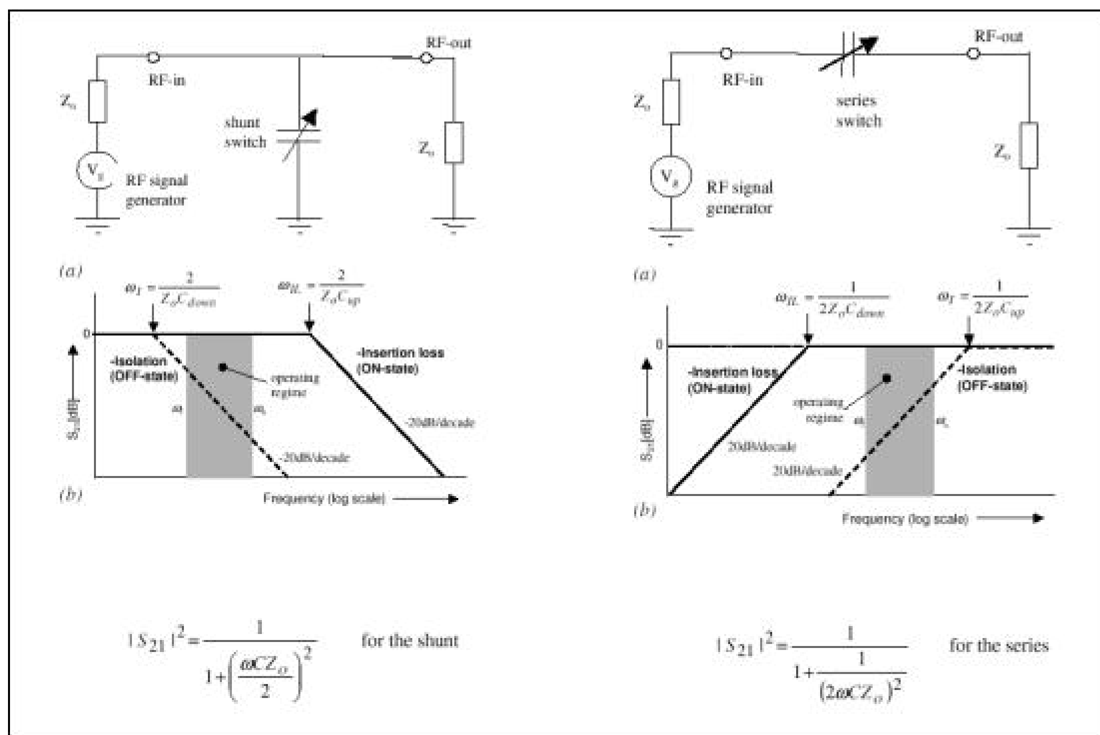


Figure 1-2 : RF commutation : series and shunt configurations

- **Actuation** : the force required for the mechanical movement can be obtained using thermal, electrostatic, magnetic or piezoelectric designs. We presented the main characteristics of each actuation principle and gave several examples. We also detailed the issue of switching speed.

Comparsion of Ten Actuator Methods

	Method	*Efficiency*	*Speed*	*Power Density*
1	Piezoelectric	very high	fast	high
2	Pneumatic	?	slow	high
3	Hydraulic	?	?	high
4	Electromagnetic	high	fast	high
5	Electrostatic	very high	fast	low
6	Thermomechanical	very high	medium	medium
7	Thermopneumatic	?	medium	medium
8	Shape Memory	low	medium	very high
9	Phase Change	very high	medium	high
10	Electrohydrodynamic	medium	medium	low

Ref: Gilbertson and Busch, http://nanothinc.com/nanosci/microtech/mems/ten-actuators/gilbertson.html
[2] and [7]: S. Shoji et al. "Microflow devices and systems", J. Micromech. Microeng. 4 (1994) 157-171

Figure 1-3 : Comparison of actuation principles

- **Reliability** : the reliability of MEMS switches (and of all MEMS devices) is a major concern for long term applications and is currently the subject of an intense research effort. The mechanical failure (metal fatigue or fracture) of well-designed micromachined cantilever or fixed-fixed beams is not a problem ([3], Rayhteon) since the beams are 75-350 µm long and are deflected only by 1-4 µm. Actually, many switches have been tested up to 100 billions cycles with no observed mechanical failure around the anchors. In dc-contact switches the failure mechanism is strongly related to the metal contact used, whereas in capacitive switches, the reliability is limited by dielectric charging. In both cases, the RF power has a strong effect on the reliability of the switches.

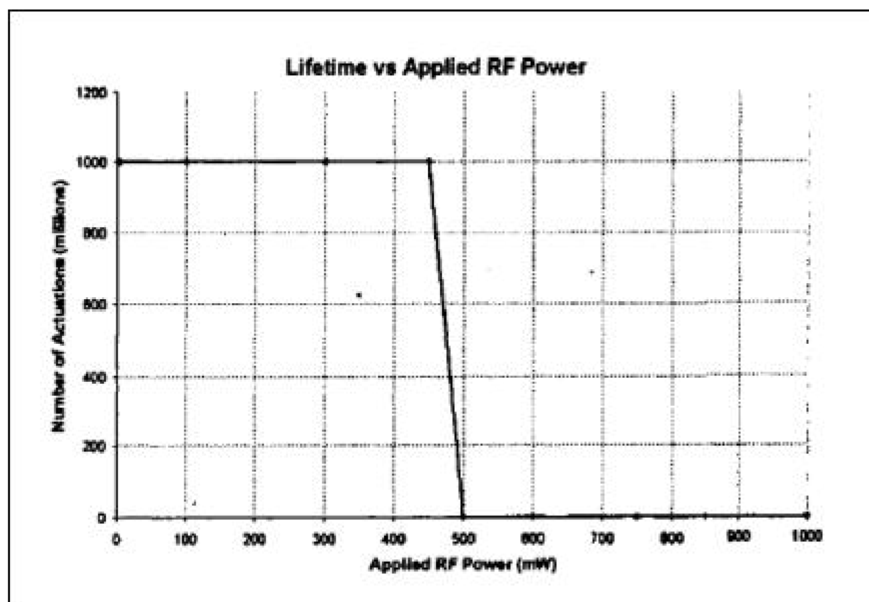
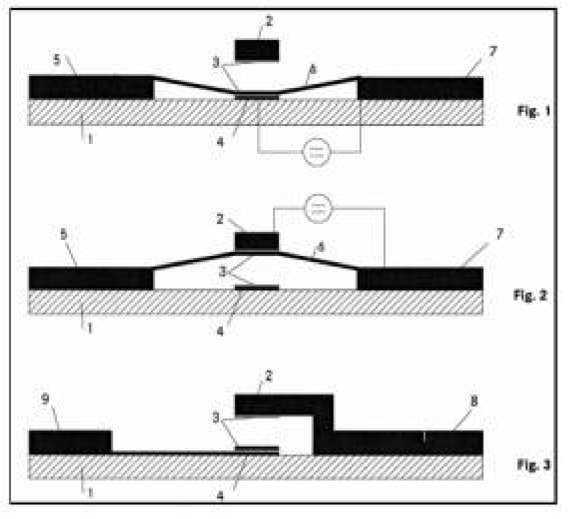


Figure 1-4 : MEMS switch lifetime versus RF power level, Raytheon [3]

▪ **Power applications** : depending of it application area, a RF MEMS switch will have to support few mW to tens of watts. We analysed the problems linked to power handling and we presented new concepts dedicated to power applications like "double anchor switch" from DaimlerChrysler [4].



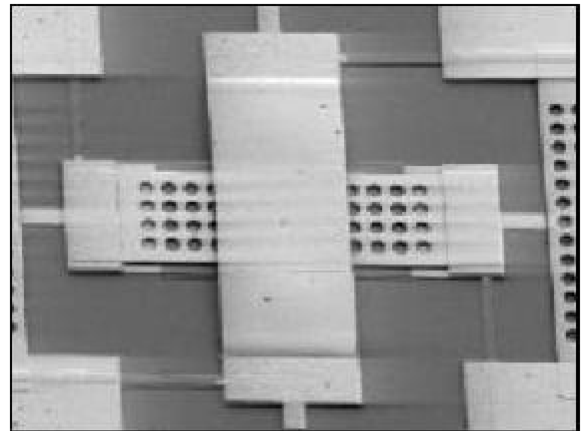


Figure 1-5 : Concept of a so called "double anchor switch" from DaimlerChrysler [4]

▪ **Packaging and integration** : low-cost, wafer-scale, high-yield, hermetic packaging techniques are essential for low-cost applications. Moreover CMOS controllers and voltage up-converters should be integrated with MEMS switches inside the hermetically sealed cavity. There is currently a lot of works in this area.

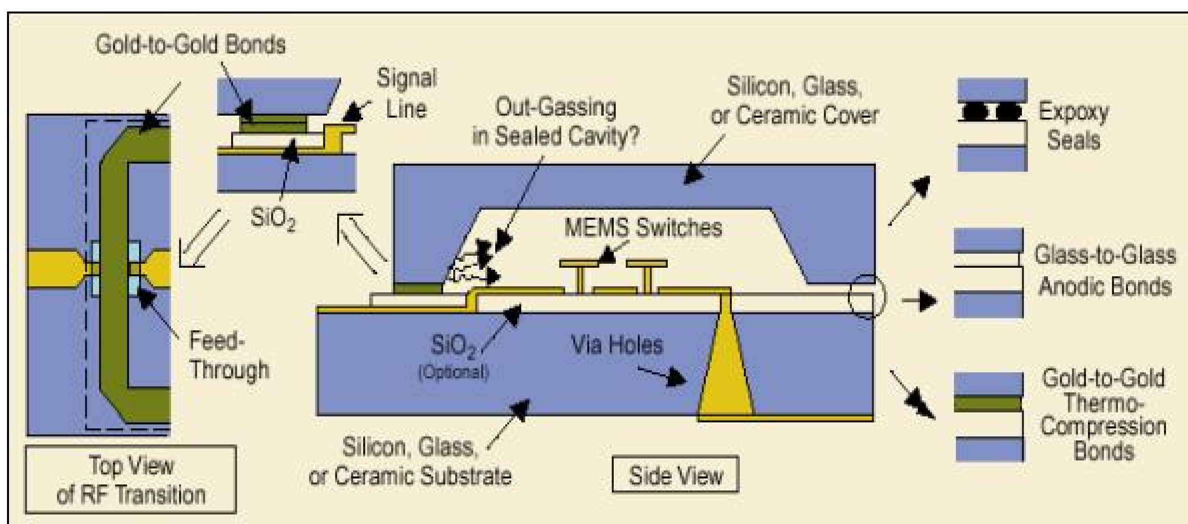


Figure 1-6 : Current-packaging and interconnects schemes for MEMS switches, [5]

- **Application areas of RF MEMS switches** : MEMS switches have outstanding isolation and insertion loss at microwave frequencies, so they can replace the GaAs switches in cellular telephones resulting in DC-power saving. They can also be used in phase shifters, which are essential for automotive or defense applications, in low-loss tunable circuits or in high performance instrumentation systems

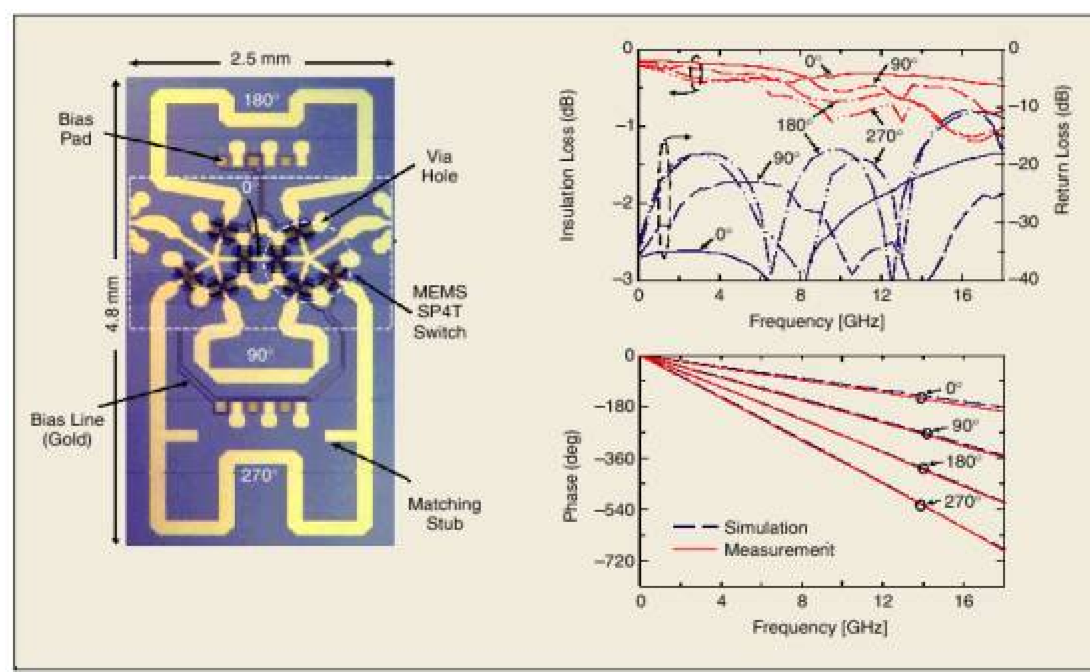


Figure 1-7 : 2-bits University of Michigan/Rockwell SP4T switched-line phase shifter, [6]

1.2.2 Film Bulk Acoustic Resonators

The document WP2_LETI_IN_IN_003, talking about FBAR technology, was published early in 2003. The objective was to provide a document which gives an overview on the FBARs and their applications. This component is promising to replace current ceramic filters and duplexers in wireless communication systems, like it is already the case for PCS applications, thanks to Agilent duplexers.

The main subjects which were developed in the document were :

- **An introduction to physical properties of resonators**, with the definition of piezoelectricity and crystallographic aspects of piezoelectric materials, and electromechanical properties of the material family. Figure 1-8 (at left) shows how the crystallographic repartition in the material leads to residual polarization under stress (piezoelectric effect). At right the diagram shows the interdependence of mechanical and electrical properties in piezoelectricity

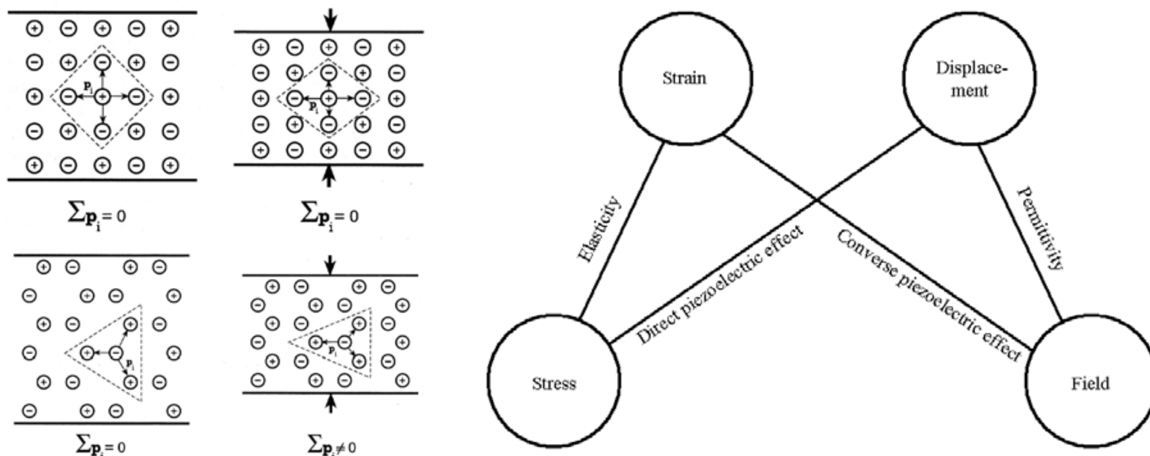


Figure 1-8 : Mechanical displacement under stress and induced polarization for symmetric and non-symmetric crystal (left). Relations among mechanical and electrical variables for a piezoelectric crystal (right)

- **The different kind of acoustic resonators** (Membrane, Air Gap or Solidly Mounted), their specific process issues and electrical responses. Figure 1-9 relates the three different kinds of FBARs

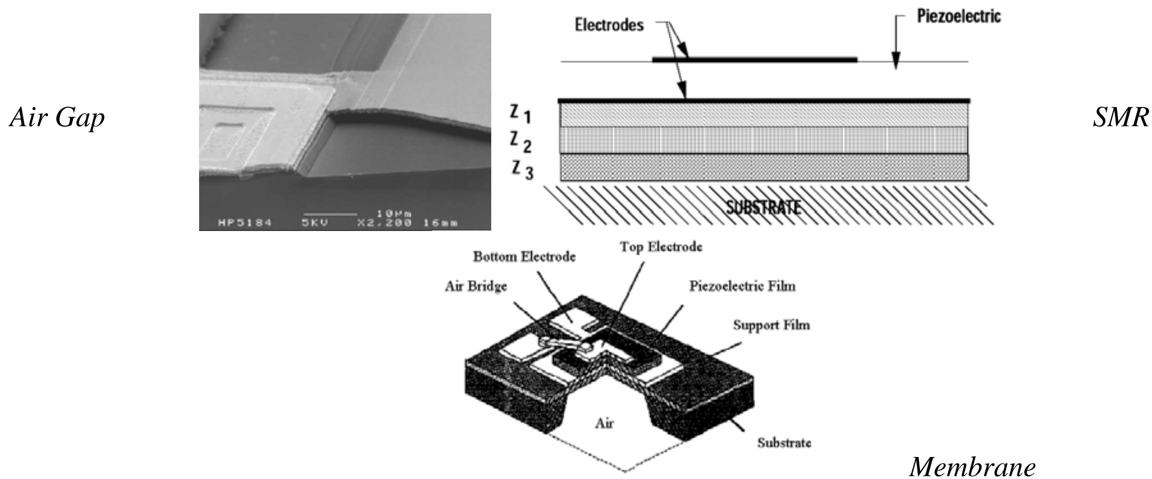


Figure 1-9 : Three different kinds of FBARs

- **The technical solution to improve the component behaviour**, like post-process for frequency tuning or temperature compensation. Here below, Figure 1-10, is shown the effect of electrodes apodization. Spurious modes are attenuated.

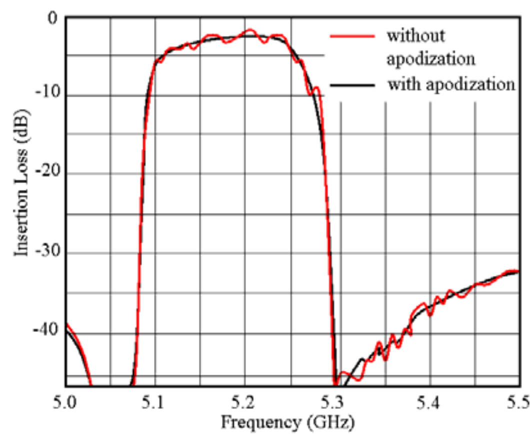


Figure 1-10 : The effect of Apodization on a FBAR filter around 5GHz.

- **The effect of the piezoelectric material on FBAR performances**, three material are mainly used, the aluminium nitride, the zinc oxide and the lead zirconate titanate, each of them presenting electrical and mechanical particularities.

- **The packaging issues**, the FBAR is a mechanical components that must be free to move, even if mechanical variation are in the nanometer range. Then special packaging is necessary to perform cavity and protect the component from aggressive environment. The next picture was extracted from a recent patent of Agilent Technologies, it represents a wafer level package.

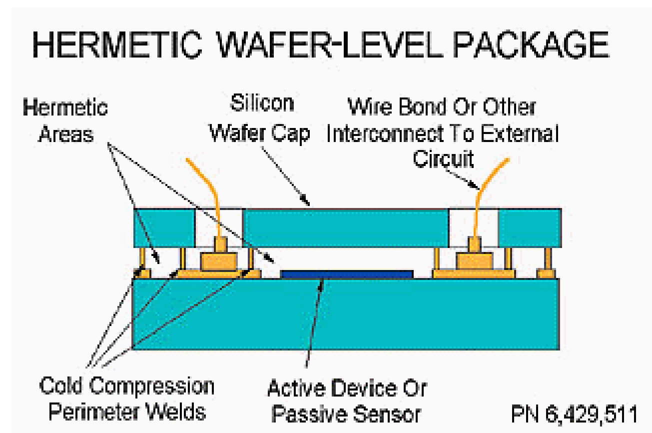
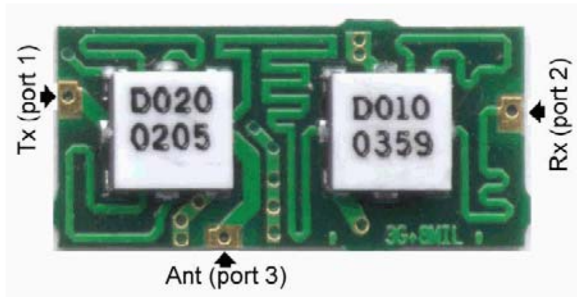


Figure 1-11 : Hermetic wafer level package from Agilent Technologies

- **The applications to filters and duplexers**, especially the Agilent duplexer that was designed to fit with PCS1900 application. The module and the related high level schematic view are shown below.



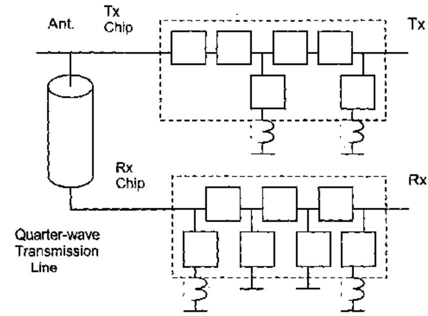
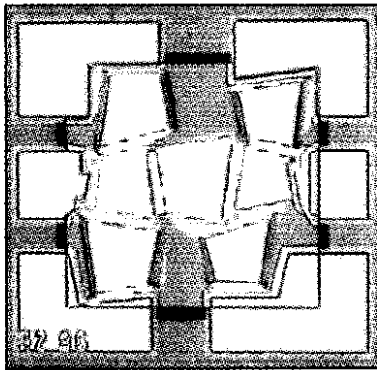


Figure 1-12 : Photography of the Agilent Technologies produced duplexer and simplified schematic (designed for CDMA PCS 1900 MHz)

The two packages contain the RX and the TX filters, which are in a ladder configuration. An example of filter die is given below



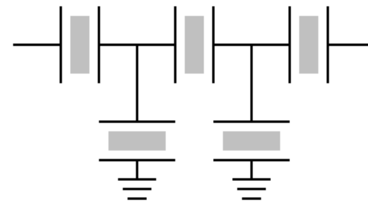
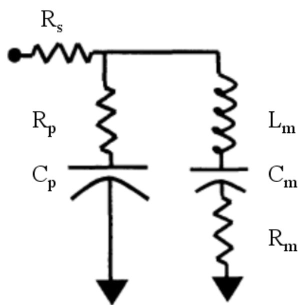


Figure 1-13 : Die of a ladder filter and equivalent electrical circuit. The circuit size is around 1mm^2.

- **Modelling and limitations of models**, mainly two models are referred in the literature, the MBVD and Mason model. Whereas the first is a lumped model for a limited range fitting around the resonance (see Figure 1-14 below), the second one is physical based model and provide a wide frequency band response.



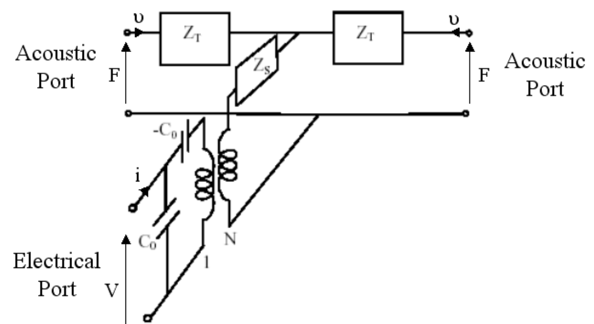


Figure 1-14 : Modified Butterworth-Van Dyke electrical model of a piezoelectric resonator around a resonance(left) and Mason wide band model of the piezoelectric layer (right).

- **An exhaustive patents and publications analysis**, with a statistical analysis since 1996. The patents are classified by subjects and owners, and the papers are grouped by authors and geographic location. The graph below shows that patent activity is growing rapidly, proving that FBAR technology is a promising subject for the next few years. Also we can see that Agilent, Nokia and TFR are the main owners.

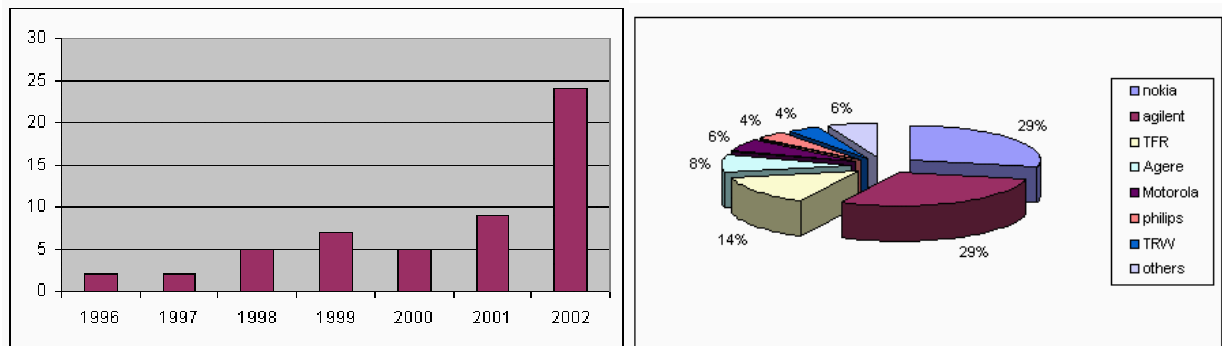


Figure 1-15 : Evolution of published patents, and main owners

The following pictures shows that companies and laboratories publications are almost in the same proportion, and that world wide laboratories have been working of FBAR technology, even if most of activity is located in USA.

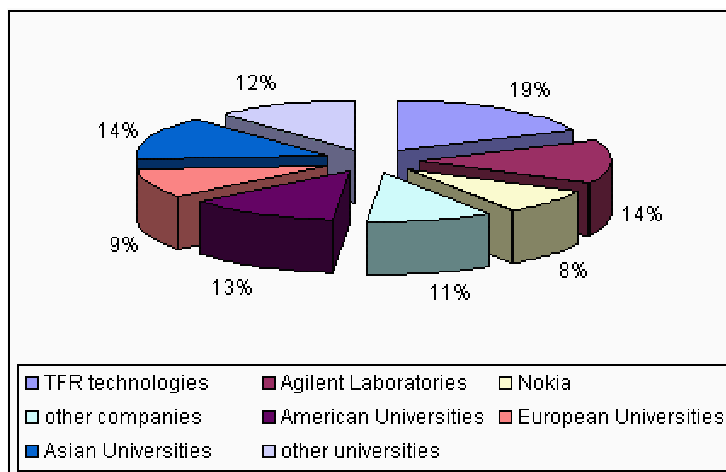


Figure 1-16 : Classification of the papers by entity.

1.2.3 Tunable Capacitors

A bibliography on RF MEMS tunable capacitors will be published as soon as possible. This document will have the same goals as the previous documents on switches and FBAR, that is to say :

- to expose the basic concepts of a MEMS tunable capacitors and the key issues to design them,
- to present the major actors (firms and universities) that worked on that component and their realizations through an exhaustive bibliography of papers and patents.

We found 53 patents related to RF MEMS capacitors from 1985 to 2003 and 60 papers from 1997 to 2003.

As we did for the Film Bulk Acoustic Resonators, we paid a special attention to patents related to MEMS tunable capacitors and we analyzed the evolution of publications of papers and patents for the last 10 years. In particular, we tried to underline the different tendencies.

There is an example in Figure 1-17 with the evolution of publication of patents since 1985 and versus their areas of application : pure RF MEMS tunable capacitors (with moving parts), tunable capacitors based on ferroelectric materials, patents related to systems within RF MEMS tunable capacitors, patents that focused only on a concept to obtain a tunable capacitor and finally patents on technology to fabricate them.

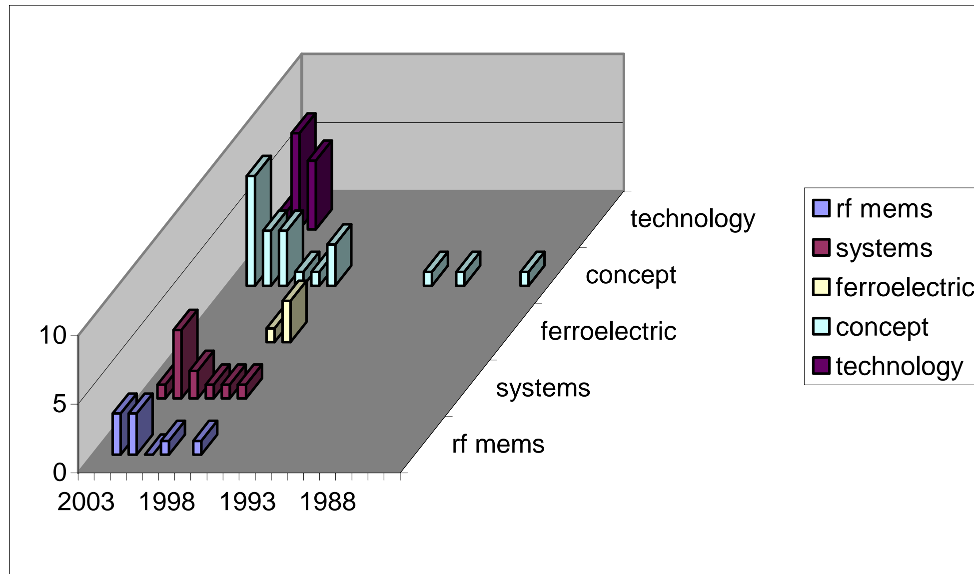


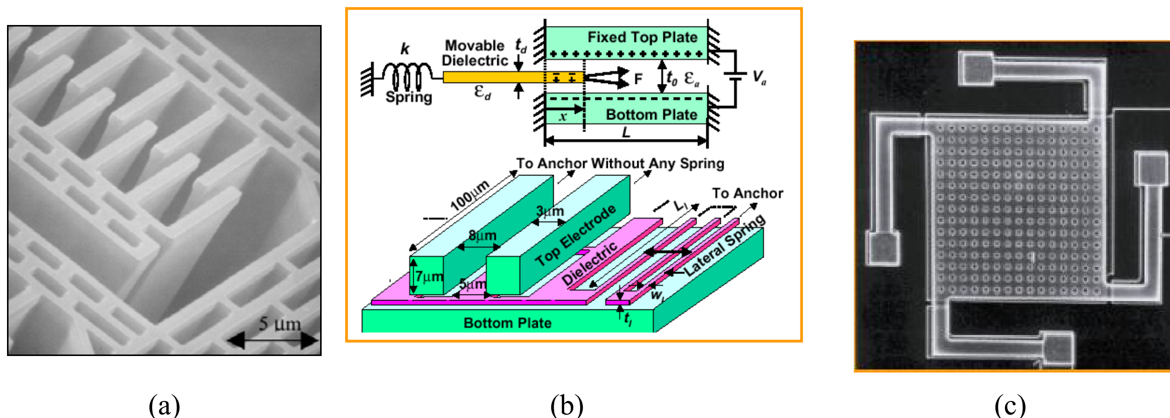
Figure 1-17 : Patents per subjects and per years, in number of patents.

The well-known equation to write the capacitance of a capacitor with two plates of area *A* separated by a gap *d* and a dielectric of constant ε is :

$$\mathbf{C} = \frac{\varepsilon A}{d} \qquad \textbf{eq. (1.1)}$$

It is clear from equation (1.1) that there are three physical parameters ε, *A* and *d*, that can be varied to obtain a tunable capacitor. So, the tunable capacitors can be classified according these 3 tuning parameters :

- *A* is varying results in the **area-tuning capacitors** like the interdigitated capacitors.
- ε is varying results in the **dielectric tunable capacitor** including the moveable dielectric capacitors and the ferroelectric capacitors.
- *d* is varying results in the **gap-tuning capacitors** like the two or three parallel plates capacitors or the zipping-action tunable capacitors.

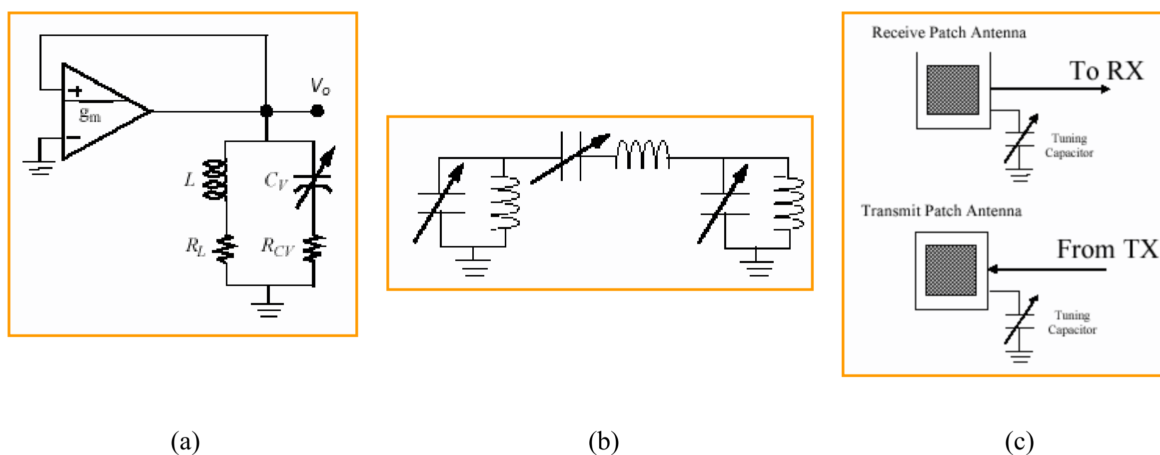


(a) (b) (c)

Figure 1-18 : Example of **area tuning capacitor** (a): the Rockwell Science Center interdigitated capacitor [7], **dielectric tunable capacitor** (b) : movable dielectric capacitor of University of Michigan [8], and **gap-tuning capacitor** (c) : the Berkeley electrostatic tunable capacitor [9]

We also deal with other subjects like :

- **Area of application of tunable capacitors** (Figure 1-19) : VCO's (a), phase shifters and impedance tuners (b), Antennas tuning (c). It will take a long time before MEMS varactors replace silicon and GaAs varactors, especially below 5 GHz, since solid-state devices result in excellent performances and do not have any special packaging requirements. Moreover the performances of planar oscillators are not limited by silicon varactors but by the loss of the planar inductors. Nevertheless, there is still a need for MEMS varactors : they have the potential of very high Q operation, especially at mm-wave frequencies, they can handle RF power and the can be designed to withstand large RF voltage swings and therefore result in very high IP3 tunable networks.



(a) (b) (c)

Figure 1-19 : Areas of applications of MEMS varactors

- **Reliability of MEMS varactors** : the reliability of MEMS varactors is much better than capacitive or series switches because the contact areas do not touch (except for the MEMS switched capacitors) and one can easily obtain billions of cycles. The main problem is charging of the dielectric layer (if used) which can create a progressive increase in the applied voltage. It can be solved by removing the dielectric layer between the capacitor plates and by limiting the applied voltage so as to ensure that a pull-down condition is never achieved.

- **Packaging** : MEMS varactors do not need to be hermetically sealed since they do not suffer much from charging or surface-contact problems resulting from humidity. However, if long-term operation is needed, it is best to hermetically sealed them.

1.3 RF MEMS Component Library

One of main goals of the task 2.1 of the MuMoR project is to create a virtual component library so that the RF-IPRs designs of subsystems based on RF MEMS can be carried out.

The most waited RF MEMS component for ensuring re-configurability is the **switch**, especially for the reconfigurable RF front-end addressed in the MuMoR project (Figure 1-20), which is mainly based on switching between different paths.

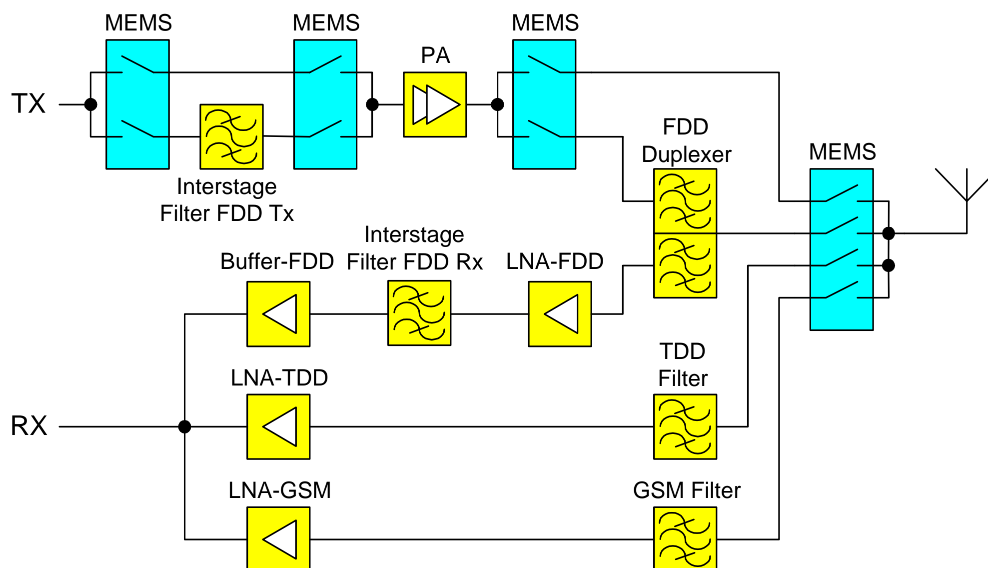


Figure 1-20 : MEMS-based reconfigurable RF front-end proposed in MuMoR Project

Fortunately, this interest of RF designers matches with the deep knowledge of LETI in developing RF MEMS switches. That the reason why LETI supply first to the partners of the project an electrical model of a switch. The LETI switch and its model is described in the next section.

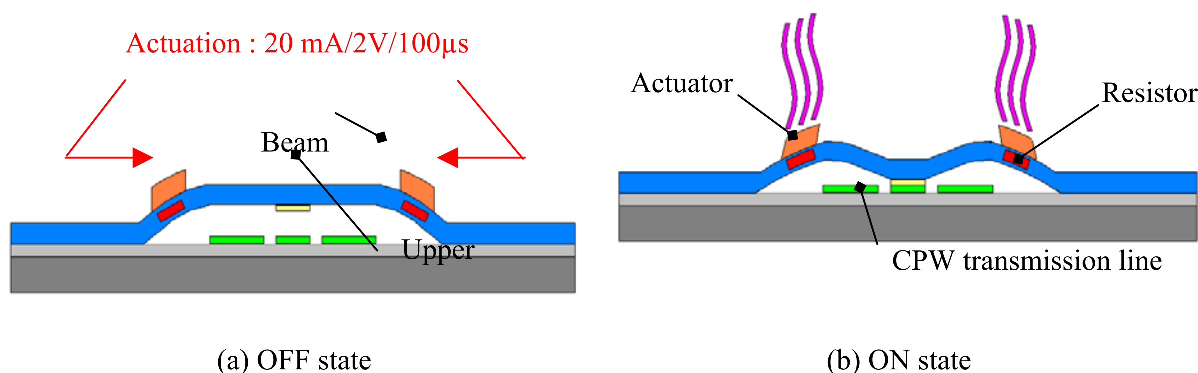
The second MEMS component added to this virtual library was **Film Bulk Acoustic Resonator (FBAR)**. This component seems to be promising for filter applications thanks to its great selectivity and quality factor, and its small size compared to current ceramic counterparts. Due to its quite "simple" technology of fabrication (there are no moving parts !), this component is the first RF MEMS device to appear on the market with the Agilent Technologies duplexer (see Figure 1-12) and it seems that is going to become a best-seller !

1.3.1 LETI RF MEMS Switch

A datasheet WP2_LETI_IN_IN_002 of the electrical model of the LETI MEMS switch was provided to the partners in October 2002 with 3 ADS 2002 files to use the model by their own.

- **Presentation of the device**

The switch operation and the design of the LETI switch was first presented. The LETI switch is thermally stimulated : by Joule effect, an electric current causes a local increase of the temperature of two resistors set localized symmetrically inside and close to both ends of a clamped beam, Figure 1-21 (a). The heat locally dissipated is transmitted by conduction to the neighborhood of the resistor. The local "actuation" film is deposited in this area. The differential thermal dilatation between the film and the beam leads to a flexion of the beam that finally establishes a mechanical contact between two conducting metallic lines, Figure 1-21 (b). This contact is also an electrical contact due to a small area metallic layer under the beam. An additional system based on an electrostatic actuation maintains the switch in the On state when the thermal actuation is removed.



(a) OFF state (b) ON state

Figure 1-21 : Switch operation of the thermally-actuated LETI switch [1]

The LETI switch is a series-configured metal-to-metal contact switch, based on the closing of a gap into the signal line of a CPW transmission line. This switch is produced using the standard techniques of microelectronics. Since all the steps are realized below 350°C, a direct integration on active devices is made possible (CMOS compatibility).

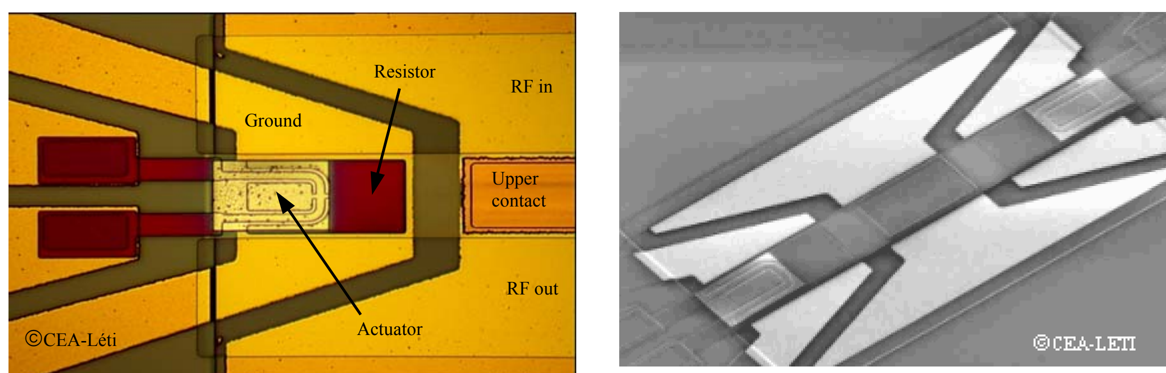


Figure 1-22 : Top view of the contact area and view of the beam

The lowest required actuation voltage is only 1.5 V. Most of the devices need 2 V for switching. The average actuation current is on the order of 20 mA which corresponds to a power consumption of 40

mW during 300µs. The electrostatic clamp system is still under development. It is designed to be less than 10 volts. The best result obtained was 15 volts.

The closure time is on the order of 100 µs. The switch is packaged in an inert atmosphere. This closure time can be made smaller. The initial aiming application of this switch, commutation of standards, doesn't require high switching speed.

The switches survived over a temperature range from –40°C to +80°C.Devices bonded have operated for over 8×10^{8} cycles when cold switched (with zero current flowing) and no degradation of the contact resistance was observed. Bonded devices were tested with a 10 W CW (Continuous Wave) input signal at 2.4 GHz. No test of long term reliability was made with such level of power.

- **Electrical modelling**

The LETI switch has been modelled separately for its two states : ON and OFF states. Finally the two models were both included in the same analog/RF schematic thanks to an ideal switch, see Figure 1-23. The first step was to modelled an CPW transmission line similar to the LETI switch in order to obtain physical values for the discrete elements of the model. Then the additional parameters of the model were derived from electromagnetic simulations of the switch thanks to a 3 D EM simulator (Ansoft HFSS). Finally, the values were optimised in ADS 2002 to fit RF measurements. Note that RF measurements are not de-embedding: the pads and RF transmission lines are part of the component, which is designed for a flip-chip reporting.

This model was optimised for the frequency range from 0.1 GHz to 6 GHz.

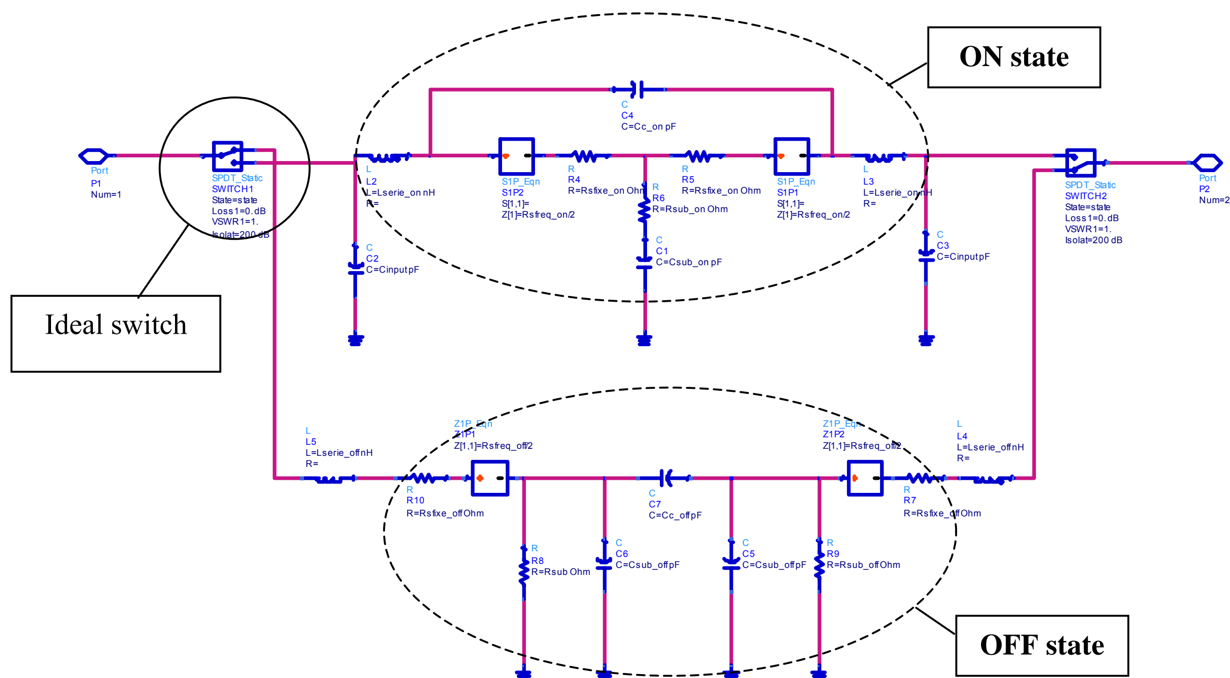


Figure 1-23 : Implementation in Agilent ADS 2002 of the LETI switch model

A schematic symbol was then defined (see Figure 1-24); only the parameter of the state of the switch is available : 1 = on state; 0 = off state.

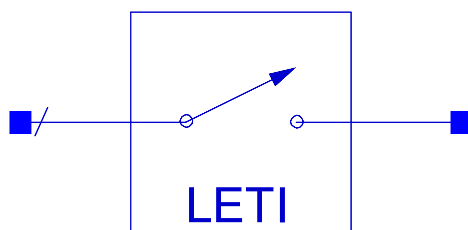


Figure 1-24 : Schematic symbol of the LETI switch

Finally we present here the comparison between measurements and model.

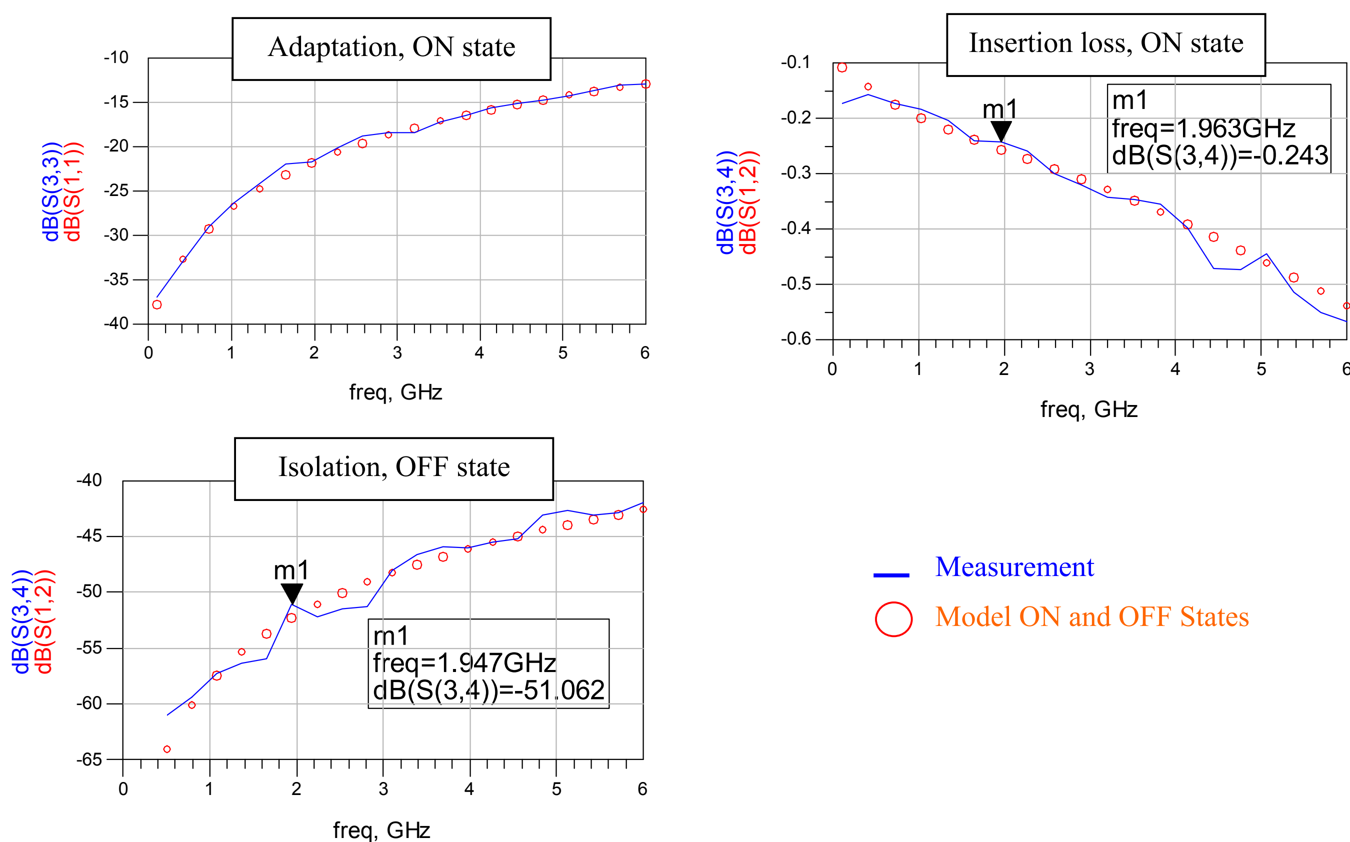


Figure 1-25 : S-parameters for measurements and model

1.3.2 Agilent FBAR Resonators

A datasheet of two electrical models for a Film Bulk Acoustic Resonator was provided in WP2_LETI_IN_IN_004. The first one was the Modified Butterworth-Van Dyke's model (MBVD), and the second one was the Mason's model. Based on Agilent publications, the default components values ware fixed such as the resonators exhibit critical frequencies around 2 GHz. Recently, an UMTS TX ladder filter based on the Mason's model was designed on the demand of IMST.

The MBVD model of the FBAR was provided in the form of a sub-network component like shown below. Inside the sub-network, we can see the relatively simple model, Figure 1-26 right.

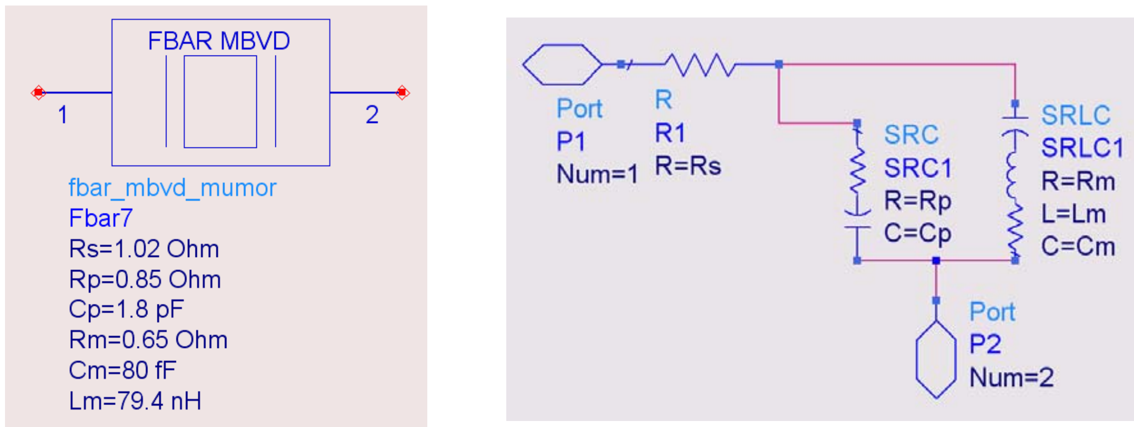


Figure 1-26 : sub-network component and embedded electrical model for MBVD

The Mason's model is quite more complicated, since it is based on physical layers acoustical and electrical properties. The figure below shows the electrical model of a piezoelectric and a non piezoelectric layer.

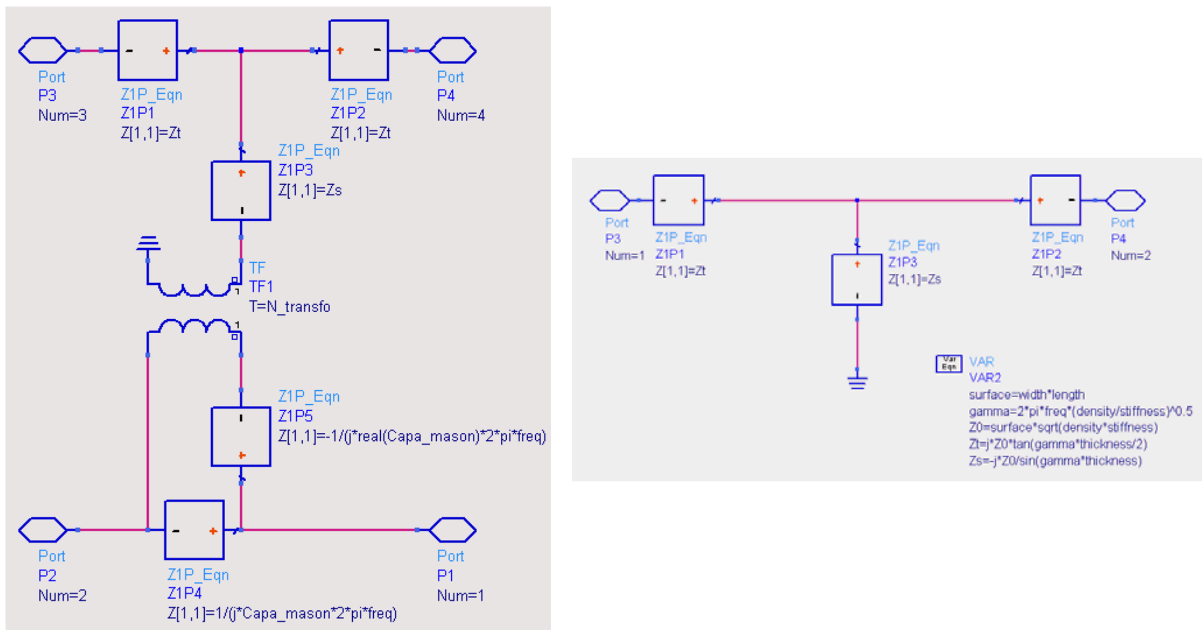


Figure 1-27 : Piezoelectric and non piezoelectric layer model to build a Mason's model

These two bricks can be used to build any component, depending on the material stacking of the acoustic resonator. The complete model is embedded in a sub-network component, like for the MBVD model.

1.3.3 FBAR Filters for UMTS Front-end

At the end of year 2003, IMST and LETI decided to investigate more precisely the feasibility of UMTS filters with FBAR technology. This MEMS technology offers the possibility to obtain low loss small filters and first of all allow to integrate these filters directly on chip what would be a big improvement.

All filters were designed according specifications given by IMST and notified in the document WP2_LETI_IN_IN_005; the default components values were chosen such a way that the filters can be realized with nowadays available technologies. To build the filters the Mason's model of a single FBAR resonator that was already provided to partners was used.

Three filters were designed and their electrical models (to be used in Agilent ADS design toll) were provided with the same document WP2_LETI_IN_IN_005 :

- The first model is for an **interstage TX filter** located between the PA-driver and the PA for UMTS FDD.
- The second is for an **interstage RX filter** between the external LNA and the mixer for UMTS FDD.
- The third one is a **duplexer** for frequency separation at the antenna for UMTS FDD.

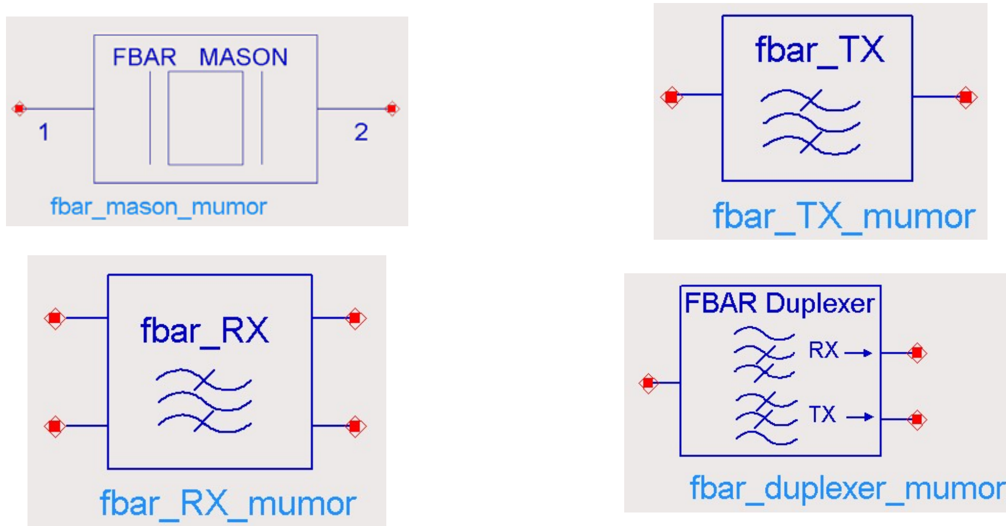


Figure 1-28 : Schematic symbols of the different models

We give here the example of the **interstage RX filter**. This filter will be placed between an external LNA and a mixer. According IMST, the filter has to have 200 ohms differential input and output and to agree attenuation requirements notified in Figure 1-29.

RX interstage filter							
Frequency	0Hz 2025MHz	2025MHz 2050MHz	2050MHz 2095MHz	2110MHz 2170MHz	2185MHz 2230MHz	2230MHz 2255MHz	2255MHz 12750MHz
attenuation	≥ 30 dB	≥ 15 dB	≥ 5 dB	≤ 3.7 dB	≥ 5 dB	≥ 15 dB	≥ 30 dB

Figure 1-29: Attenuation requirements for RX interstage filter

We choose a 2 cells lattice configuration which is very suitable for differential input/output filters. The small number of resonators, 8 resonators, enables to have very low insertion loss, see Figure 1-30.

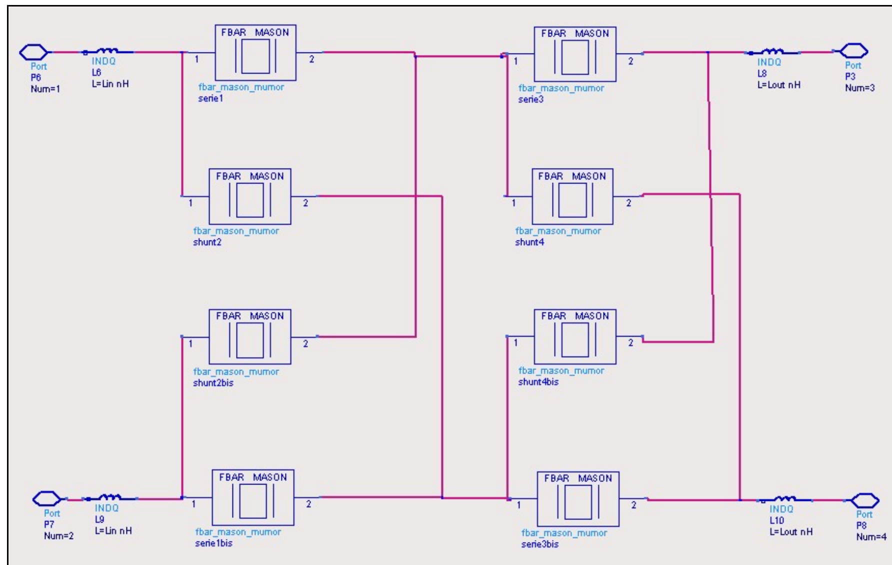


Figure 1-30 : Two cells lattice configuration for RX interstage filter

We obtained the following results :

- The minimum insertion loss is 0.75 dB at 2138 MHz, the maximum is 1.06 dB at 2110 MHz.
- The maximum ripple in a single 5 MHz channel is 0.1 dB for the first channel 2110-2115 MHz.
- The minimum matching (Sdd11 and Sdd22) in band is 14 dB at 2110 MHz.

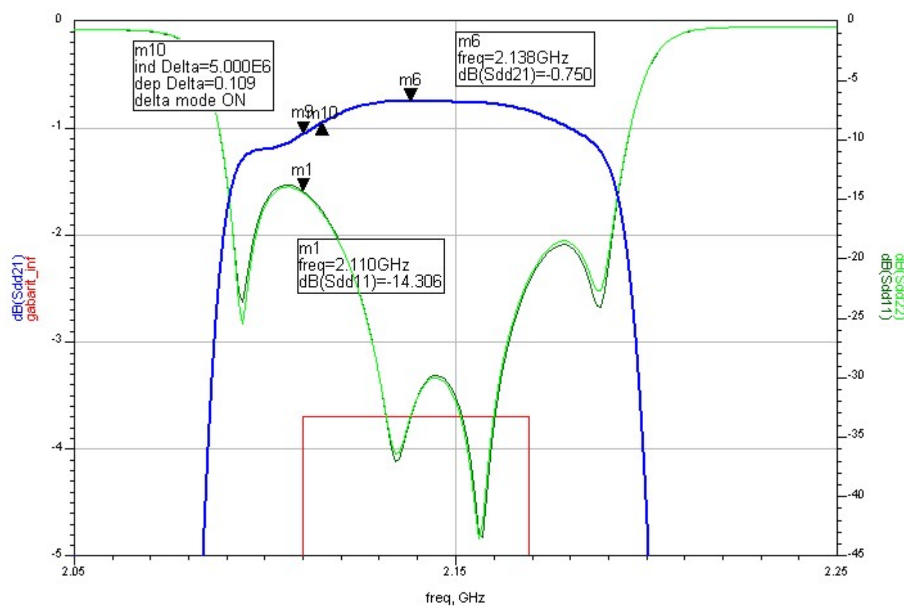


Figure 1-31 : Insertion loss (Sdd21 in dB) and matching (Sdd11 and Sdd22 in dB) for the RX interstage filter

- The maximum group delay ripple for a single 5 MHz channel is 0.42 ns which is 0.16 % of the chip rate (T_{chip} = 260.42 ns). Specification is to be below 2 %.

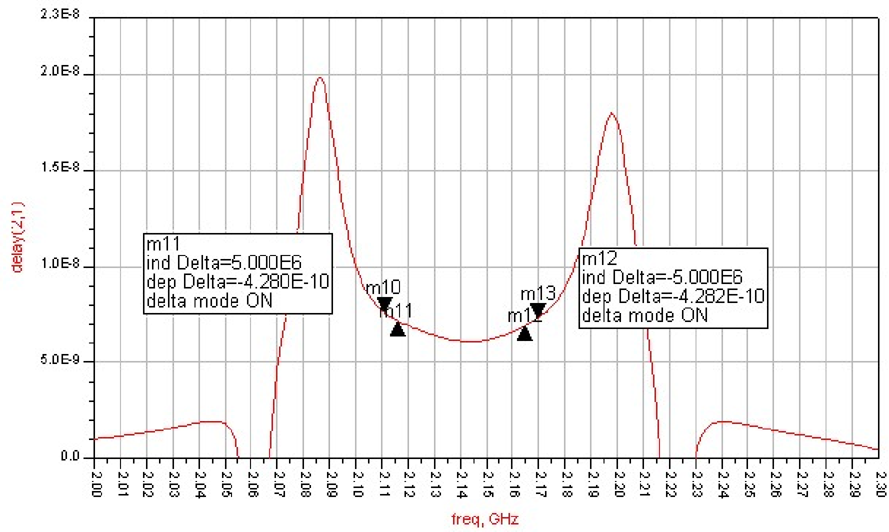


Figure 1-32 : Group delay on Sdd21 of the RX interstage filter

- There is considerable decrease in attenuation near the 2nd order resonance frequency. It can be bypass with a low pass filter.

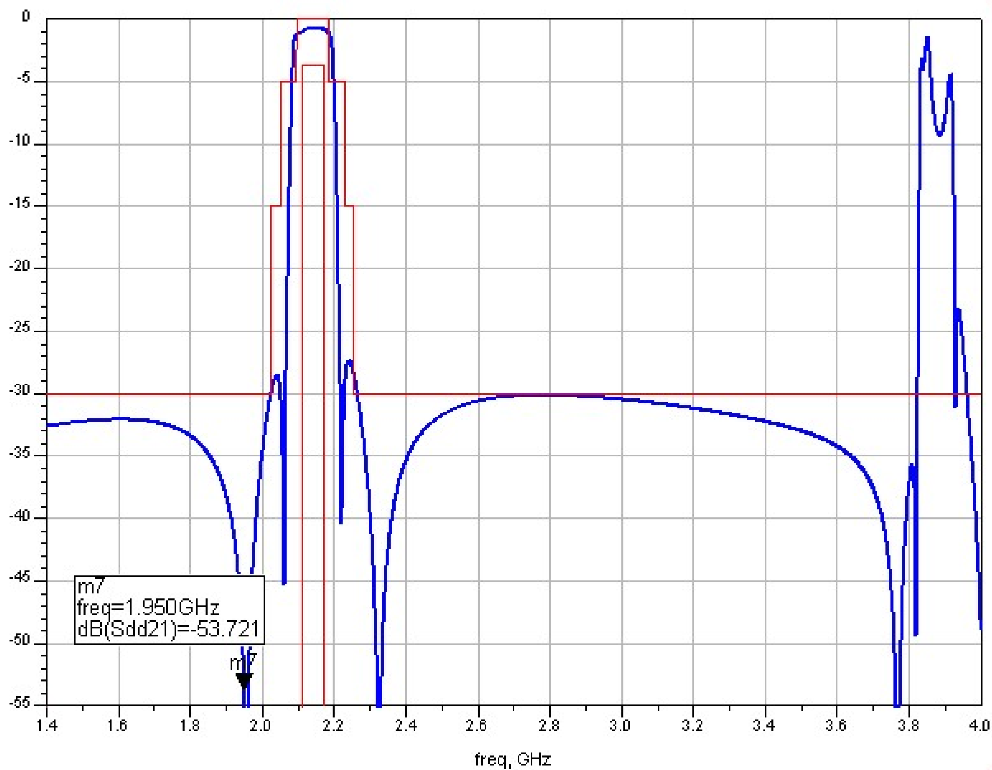


Figure 1-33 : Wideband response (Sdd21 in dB) of the RX interstage filter

The results for **the interstage RX filter** and for **the duplexer** can be found in the document WP2_LETI_IN_IN_005.

1.4 Conclusion

LETI has already supplied to partners models of two kinds of RF MEMS components : switches and FBAR resonators. These models are based on studies done by LETI (for the switch) or on data extracted from literature (for FBAR).

Two corresponding bibliographies were published to expose the basics concepts of these devices and to ensure that we propose models that are closely related to what is available, or what will be early available, in term of electronic functions, performances, size and fabrication facilities.

The electrical of the FBAR resonator were used to built filters for UMTS according specifications given by IMST. The goal is to investigate the feasibility of these filters with FBAR technology in term of RF performances. This MEMS technology offers the possibility to obtain low loss small filters and first of all allow to integrate these filters directly on chip what would be a big improvement. Notice that the default components values are chosen such a way that the filters can be realized with nowadays available technologies.

2 Modeling techniques and verification methodologies for substrate coupling effects in multi-mode RF transceivers

2.1 Introduction

Today's Mixed-Signal System-On-Chip (MS-SOC) can include, on a single chip, such heterogeneous designs as embedded DRAM, Digital, Analog, RF front-ends, complex Mixed-Signal, Microprocessor, DSP, etc. This situation leads to two seemingly contradictory requirements on design methodology: on one hand, higher levels of abstraction is needed to cope with the added complexity in design, while at the same time, the shrinking process technologies and the single-chip integration require inclusion of lower level details. The unprecedented impact of lower level physical effects such as interconnect parasitics, cross talk, as well as substrate bounce, IR drops, and inductance effects represent enormous challenges for electronics design automation (EDA) tool developers as well as for designers [10]. Currently, designers are often forced to drift away from the transistor level physical phenomena to higher levels in the design hierarchy, to be able to manage the increasing complexity of their designs. In this context, the potential of computer simulation and methodologies in aiding the design decisions is becoming evident.

For instance, the relentless drive towards a single chip integration of digital, analogue and RF sections has opened the door to a host of challenging noise coupling effects which should be controlled [11]. In the case of MuMor project the targeted objectives in term of consumption, high performance and high integration/low cost, push toward single chip solutions with minimum external components and minimum number of design iterations. The integration of the entire transceiver on a single chip is generally infeasible for such demanding applications. This is particularly due to the large cross-talk coming from the digital blocks. Zero-IF architecture was adopted for the reconfigurable MuMor transceiver since it lends itself to monolithic integration much more easily than do heterodyne receivers and suffers much less from mismatch-induced effects. The two principal limitations for this solution however can be dramatically heightened by the substrate coupling and supply noise. First, the DC offset which corrupts the signal and more importantly saturates the following stage. This problem is due to LO leakage and self-mixing. Second, the phase noise which leads to dramatic change in the frequency spectrum and timing properties [12-16]. This problem is accentuated by the switching noise coupled to the VCO through the substrate from the high speed divider/counter circuit of PLL or from digital sub-circuits.

The principal strategies to limit substrate noise coupling are [17-22]: Using multiple pins/wires assignment for on-chip power supply/ground, in order to reduce the value of the corresponding parasitic inductance; splitting supply lines and terminals of noisy and sensitive blocks; installing guard ring with dedicated on-chip ground; increasing the distances between noisy and sensitive circuits ; using on-chip decoupling capacitance; using special package like ball-grid array package or flipchip; adopting differential topology for analog design; using silicon-on-insulator or triple-well technology etc. However, without the ability to analyze the true effects of substrate noise, many of these techniques are often over deployed, resulting in longer design cycles and increased manufacturing costs. Thus it is highly desirable to select the correct noise avoidance strategy to save valuable silicon area and avoid the use of costly process or packaging solutions. On the other hand, the substrate coupling depends strongly on the kind of the circuit, the technology used, the layout, the substrate doping profiles, and package parasitics. A successful design-oriented methodology, that efficiently uses substrate modeling tools in the design flow, takes all these aspect into consideration. The substrate coupling problems will continue to lead to prolonged design cycles, and missed market opportunities.

In the framework of MuMor project, an innovative global methodology based on the 3D substrate modelling tools SubstrateStorm (developed initially in EPFL and commercialised now by Cadence) was developed [23]. The first ultimate objective is to verify early in design flow if the noise coupling will corrupt the functions of our system. This verification process enables us to make necessary design

changes before physical implementation of the system, resulting in a significant reduction of the delay and the cost of the operation. However, the verifications at these stages are highly domain/circuit specific and cannot be easily generalized or automated. Nevertheless, a general strategy to guide us in the early analysis can be formulated. This methodology was implemented in the design flow of the synthesizer. A first application of this methodology will show how the impact of the high speed Prescaler/Divider supply and substrate noise on the VCO spectrum purity can be evaluated and minimized before the layout implementation saving time and reducing the cost of the corrections. On the other hand, the substrate coupling is essentially a global problem that depends on the full-chip layout, the technology used, and the package parasitics. Therefore, a strategy considering all these aspects in an iterative noise-immunity optimization loop, at full-chip level, is developed. A successful application of this iterative strategy is only possible if a high speed substrate modeling extractor is available. Several investigations of the substrate noise coupling process were performed in order to capture their fundamental characteristics and simplify the substrate model extraction. Those simplifications accelerate significantly the substrate modeling with SubstrateStorm, avoid the dense matrix storage, and hence enable the implementation of the iterative noise–immunity optimization loop. Since this methodology is dedicated to post-layout verification its application to MuMor circuits will be achieved later. However, to evaluate its efficiency, several tests were achieved on a real design, that is representative of mixed-signal design style and complexity.

2.2 Early verifications in the design flow

The cost of design corrections grows exponentially as we go deeper in the design flow, and waiting till the full system implementation to verify noise-coupling problems generates an unsupportable additive delay and cost. To deal with this problem, we have developed the methodology entitled **SubCirI** and illustrated in Figure 2-1. The high level role of this methodology is to verify the analogue components and/or RF front-end early in the design flow, and to make sure that they will continue to meet the desired specifications even in their future noisy environment. This methodology will enable us to make decisions during the circuit-level design, and to focus on the analog and RF parts which don't meet the desired specifications in the presence of the digital switching noise. The possibility of redesigning sensitive sections to be more robust as well as redesigning perturbing sections to generate less noise is then considered. Eventually, the noise attenuation required to save the basic functionality of the system will be estimated. This information is very helpful to estimate the failure risk as a function of the technology and the package expected to be used. The blocks which meet specification with larger margin than required can also be relaxed, saving cost and power.

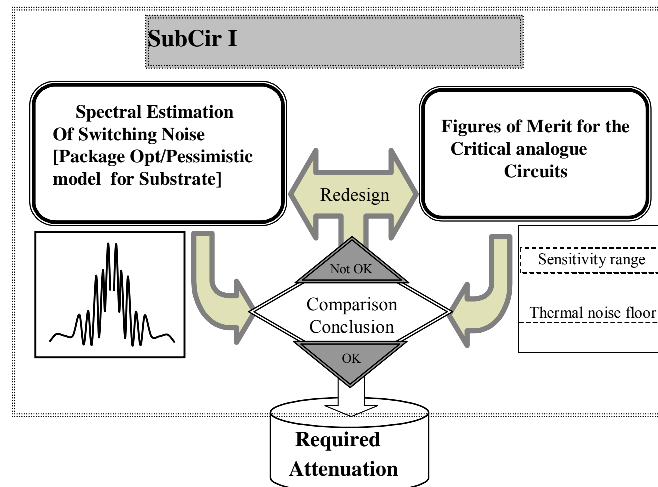


Figure 2-1 : Flow diagram of SubCirI methodology.

As shown in Figure 2-1, the successful construction of such methodology is only possible through a well-considered approach of three different aspects: the model of substrate and supply noise produced by perturbing circuits, the sensitivity to noise for analog and RF blocks and the estimation of the noise transfer functions from noisy blocks to sensitive parts. In our study, a worst case where the substrate is modeled as a single node, causing no attenuation of the noise between different placements of the chip is used in a first stage. Therefore, we can verify if the analogue and RF circuits meet the figures of merit defined by the designers, even in presence of substrate noise and eventually determine which attenuation is necessary for this.

2.2.1 Spectral estimation of switching noise

Several kinds of circuits can generate supply/substrate noise. In general, digital circuits are the noisiest parts of the chip. However, some analog cells, especially those with voltage/current transients or large signals such as power amplifiers, can be noise generators as well. For large circuits, the simulation at transistor-level makes the exact switching noise evaluation very demanding in terms of memory and extraction time and even infeasible in several cases. To deal with this complexity, useful techniques have been proposed in the literature [24-29]. The methodology of [25], for instance, uses a macro-model library of digital cells that includes package parasitics, in combination with VHDL switching events simulation, to generate the transient noise of digital circuits. Because of the high-level nature of the method, it seems to be the most compatible approach for our SubCirI methodology. In the case of low and medium size perturbing circuits, SPICE-like simulator is sufficient to simulate the power spectral density of their noise, as will be seen in section 2.5.

2.2.2 Noise effects on analogue circuits

The principal impact of the noise on analog circuits is to limit the minimum signal that can be processed with acceptable quality and therefore, to limit their sensitivity. The key metric, characterizing the circuit performances in a noisy environment, is the signal to noise ratio (SNR). However, the variety and complexity of analog cells makes a unified physical explanation of how the noise affects their performances almost impossible. Our requirement of evaluating whether the

analog/RF functionalities are corrupted is only possible with an accurate transistor-level analysis of each potentially sensitive circuit separately. The analog circuits of mixed-signal systems are often designed with a differential topology. Therefore, the supply and substrate noise appears as common-mode (CM) perturbations and should be rejected by the balanced operation. In reality however, neither are the circuits fully symmetric nor does their current sources exhibit an infinite output impedance. For instance, nominally-identical devices suffer from a finite mismatch due to uncertainties in each step of the manufacturing process. As a result, the analogue operations, even differential, can be seriously affected by the CM supply and substrate signals. The key metric that characterize the CM to differential conversion is the common-mode rejection ratio (CMRR). The CMRR is defined as the undesirable differential component produced by CM variations, normalized to the wanted differential output. Therefore, the CMRR is very good optimization parameters for SubCirI, enabling to evaluate the failure risk of analog operations in a noisy environment. On the other hand, many studies of noise impact on specific blocks such as Mixers, VCO, LNA have been published [15,19]. These works provide a very useful background for a successful application of our methodology.

2.3 Post-layout substrate modeling

In this section we will show how a good physical analysis of the noise coupling in Mixed-Signals-IC will enable us to build an efficient hierarchical post-layout modeling strategy. The substrate coupling verification flow will be broken into a set of independent modeling stages as shown in Figure 2-2.

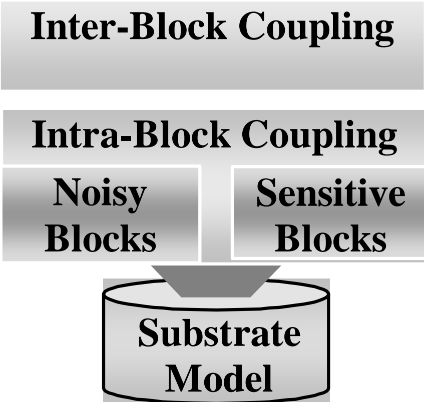


Figure 2-2 : Substrate Modeling Flow.

The crucial result we demonstrate here, is that the accuracy parameters governing the global substrate coupling, that is the inter-block coupling, are different from those governing the local transistor level coupling (i.e. intra-block coupling). As a result, we can accurately analyze the inter-block substrate coupling with a coarse local intra-block coupling representation. At the same time we can accurately analyze the transistor level substrate coupling with a coarse global inter-block substrate coupling representation.

2.3.1 Inter-block coupling

Several investigations of the substrate noise coupling process were performed in order to capture their fundamental characteristics. As most CMOS logic elements can be reduced or decomposed into CMOS inverters, the designed substrate noise evaluation chips (Figure 2-3) include *N* inverters with *N* varying from 12 to 1200.

For lightly doped substrate (the standard technology in RF ICs), it is obvious that the metal connecting the ground/*Vcc* substrate contacts provides the lower impedance path to spurious signals. In addition, the power supply noise is generally several orders of magnitude higher than spurious currents injected through the Sources/Drains into the substrate [19,20]. As a consequence, our analysis will target the parasitic coupling between *Vcc*/ground contacts of the various blocks. On the other hand, the FET and bipolar transistors have a capacitance to the substrate in the range of few fF and $Z(1fF) \sim 1M\Omega$ (at 0.15GHz), which can be considered as infinite compared to typical substrate resistances. Consequently, we can predict that their presence around on-chip ground/*Vcc* contacts have no effects on the isolation between the ground/*Vcc* contacts. However, at the same time, the impedance of the transistors to substrate decreases at high frequency and for large circuits.

Therefore, the first questions that emerge are: according to these considerations can we consider only ground/*Vcc* contacts of the chip while formulating the substrate model, and what the limit of that model is in terms of frequency and number of transistors? To answer these questions, simulations are performed on several chips with 12 inverters for the smaller and 1200 inverters for the larger. A typical tested chip schematic and layout are illustrated in Figure 2-3. During this study, we will extract an accurate 3D model for the substrate of each chip, using the FDM-based extractor SubstrateStorm [23] with very fine meshes, we will add the netlist of the circuits (i.e. inverters) and a typical package model (wires inductances =5nH), and afterwards we perform the simulation of the transfer function V_{out}/V_{in1}. As shown in Figure 2-3 the transfer function V_{out}/V_{in1} represents the isolation between the noisy inverters on-chip ground contacts and the sensitive on-chip ground contacts.

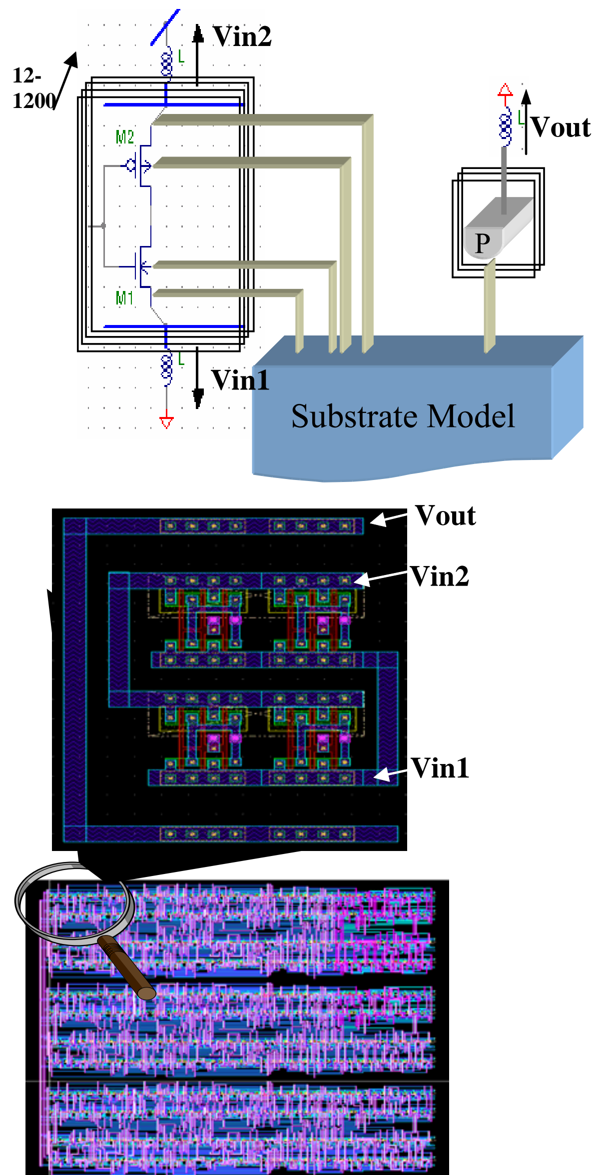


Figure 2-3 : Schematic and layout of substrate coupling evaluation chip

Two models will be compared. The first model is the *Full-SubModel,* where the substrate model of the full layout considering PMOS, NMOS, Wells, *Vcc* and ground contacts was extracted, the typical resulting network for one inverter is illustrated in Figure 2-4 (A). The second model is *the Simplified-Sub Model*, where the capacitors (i.e. nMOS to substrate capacitance and nwell to substrate capacitance) are considered as open circuits and so only ground contacts of the layout were considered for substrate modeling. The typical resulting network with *the Simplified-Sub Model* for one inverter is illustrated in Figure 2-4 (B).

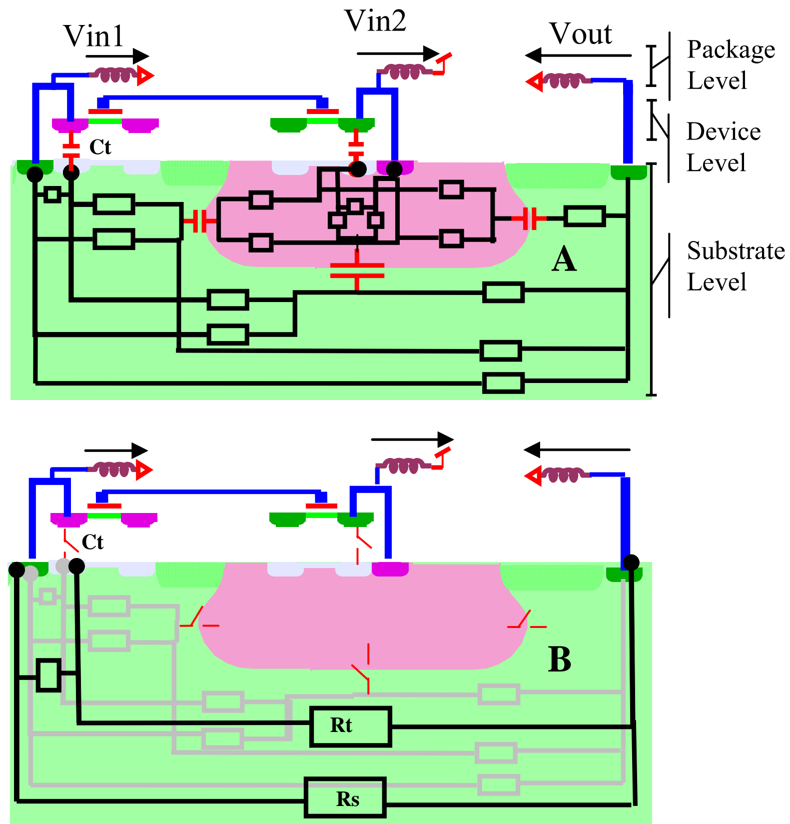


Figure 2-4 : Typical extracted network for one inverter: (A) with Full SubModel; (B) with Simplified SubModel

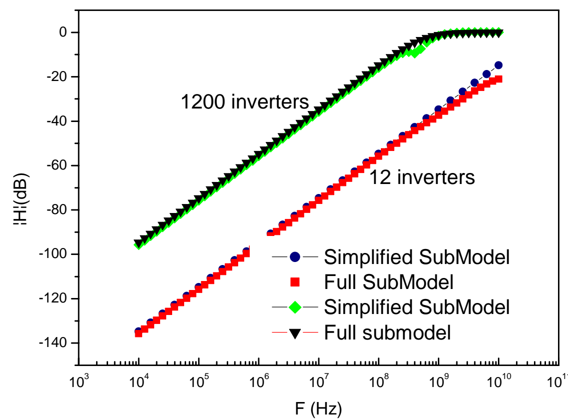


Figure 2-5 : On-chip ground-to-ground isolation (S=Vout/Vin1) for 12 and 1200 inverters as a function of frequency using simplified and full substrate models.

As shown in Figure 2-5, the simplified and full substrate models show an excellent agreement for all frequencies and numbers of inverters considered. The reason is as follows: the coupling path from *Vin1* to *Vout* can be decomposed into *N* parallel paths, and each path decomposed into two principal

coupling path (Figure 2-4 (B)) an indirect paths through the NMOS ($R_t+1/j\omega C_t$) in parallel with a direct path through the substrate (R_s). The term $|1/j\omega C_t+ R_t|$ is much larger than R_s for two reasons: the low value of C_t (~fF) and high value of R_t (indirect path). In addition, even if the equivalent impedance of the N indirect path ($R_t+1/j\omega C_t$) decreases for large circuits (i.e. large N) the equivalent impedance of the N direct path (R_s) also decreases proportionally, and thus, remain the dominant coupling paths. Note that the package substrate system ($V_{out}\approx jL\omega/(R_s+jL\omega)$) becomes a high pass filter, with a corner frequency of R/L.

For a final validation of the simplified model and a more realistic accuracy comparison, measurements on a real design (Figure 2-6) that is representative of mixed signal design style and complexity are achieved. The tested circuit (Figure 2-6) is a transceiver dedicated to ISM applications [30-32]. In this circuit the power amplifier (block I) is the strongest noisy block [32] and we would like to evaluate the isolation between their on-chip ground contacts and those dedicated to the other subcircuits of the chip (block II). The on-chip contacts of the chip are, however, physically inaccessible due the package, and the on-chip AC ground to ground transfer function considering the substrate, the package and the devices of the chip, such as those extracted by simulation and shown in Figure 2-5, are impossible to achieve experimentally. To overcome this limitation, we have achieved DC measurements of the resistance equivalent to the distributed network linking the substrate ground contacts of the PA to the substrate ground contacts the other blocks. In fact, the package parasitics has only a negligible effect on DC measurements and hence the on-chip ground to ground substrate model can be measured from the outside that is through the package corresponding nodes. Afterwards, we have added to the measured substrate model the package model and the schematics of the circuits and we have used a SPICE-like simulator to achieve the AC simulation of the ground to ground isolation. The results are illustrated by the curve "Measured SubModel" in Figure 2-6. For comparison the same simulation is achieved, but instead of the measured network, an extracted network using FDM and considering only ground contacts of the layout (i.e. Simplified SubModel of Figure 2-4 (B)) is used. The results are illustrated by the curve FDM-SubModel in Figure 2-6 and as expected the simplified substrate models shows a good agreement with the measured one for all the considered frequencies.

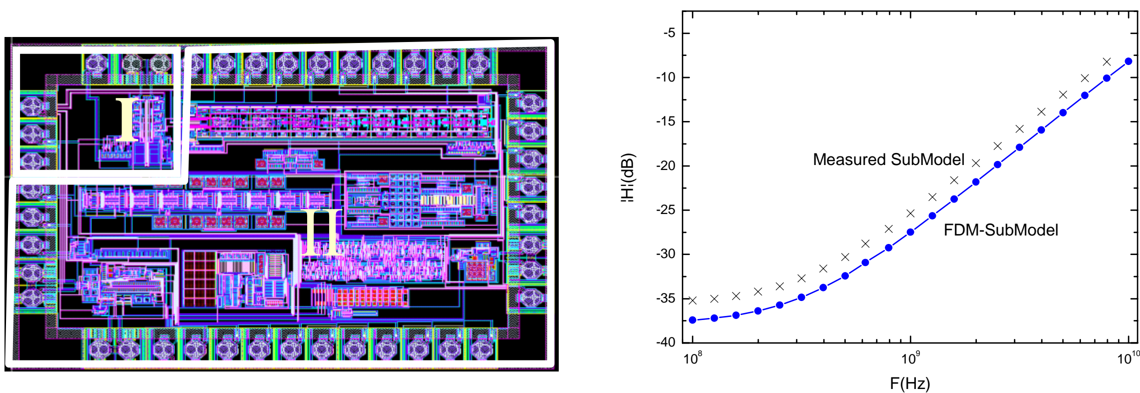


Figure 2-6 : The Transceiver Chip and the ground to ground isolation between the PA (block I) and the other subcircuits of the chip (block II).

The second question now is: according to the fact that *Vcc* contacts are isolated using n-well in CMOS technology, can-we neglect *Vcc*-to-*Vcc* and *Vcc*-to-ground coupling and consider only ground contacts of the layout when we perform the substrate model? To answer this question, simulations of the noisy-*Vcc* to sensitive-ground isolation (*Vout/Vin2 Figure 2-4 (A)*) were performed for the chips with 12 to 1200 inverters of Figure 2-3 and compared with *Vout/Vin1*. The results are shown in Figure 2-7. The values of ground-to-ground isolation (*Vout/Vin1*) are very low compared to *Vcc*-to-ground isolation (*Vout/Vin2*) values in low frequency range and within the same order of magnitude in the high frequency range. Therefore, the low frequency components of the power supply noise at *Vcc* are

effectively filtered by well-junction capacitances and the high frequency components is only attenuated. Hence, neglecting the *Vcc* and wells in the substrate model can lead to an underestimation of the high frequency noise effects.

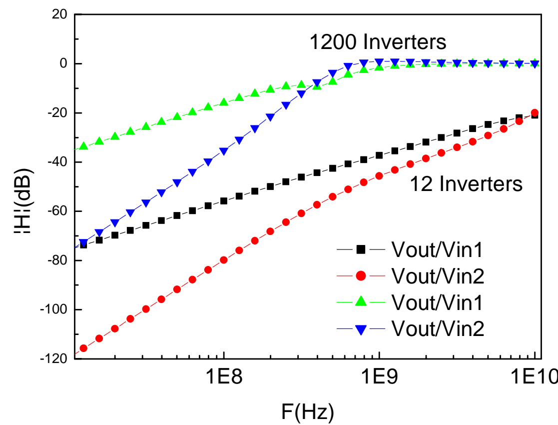


Figure 2-7 : On-chip Vcc-to-ground isolation (Vout/Vin2) and ground-to-ground isolation (Vout/Vin1).

In conclusion, by considering only a layout with *Vcc*, ground contacts and wells for substrate model we can analyze and compare the isolation between various blocks of the circuits without any significant loss of accuracy and with a considerable gain in terms of execution time and memory used. Note that all these simulations were repeated for various positions of the inverters and sensitive contacts on the chip, and exactly the same conclusions were made.

2.3.2 Intra-block transistor-level coupling

Once the block-to-block substrate coupling is well represented, we are interesting on the intra-block coupling. For this, we will distinguish between the noisy block modeling and the sensitive block modeling.

2.3.2.1 Sensitive analog block

The sensitive analog blocks can require a more accurate substrate model. In fact, for some analogue circuits, the substrate resistances can have a direct effect on their performances, independently of the noise coupling. For instance, the noise figure of an LNA can be affected by the substrate resistance thermal noise. The substrate resistances can also result in a change in the input/output matching of LNA, reducing its gain and its reverse isolation [34-37]. Moreover, The standard process technologies, produces substrate with three-dimensional (3-D) contacts (wells, collectors), vertical and lateral doping profiles (channel stop, well, triple-well, buried layer, heavily doped bulk substrate, etc.), and complex 3D structures (trench oxide, thick metal, integrated inductor, bonding path…). Windowing strategy, considering only this analogue sensitive part of the chip (e.g. block (A) in Figure 2-8) will be used to extract this inter-block substrate network. The full substrate model considering all elements of the layout will be used for this part in order to maximize the accuracy of the analysis.

2.3.2.2 Noisy blocks

In addition to power supply noise, the switching activity of digital blocks injects spurious signals in the substrate through the reverse junction capacitances of transistors or by impact ionization (hot carriers). Transistor neighboring substrate contacts pick up the most of these signals. We can expect that the substrate model at transistor level will have an effect on this kind of noise. We can predict also, that connecting the bulk of each transistor directly to ground will represent the worst coupling case. The circuits optimized with this configuration will work, but with a larger margin than necessary. In the other hand each transistor is linked to substrate ground by impedance equal to (Rs+1/jCw). As C is of about few fF, the substrate resistances play only a negligible role in this coupling. In conclusion for all noisy blocks, we can connect the bulk of NMOS transistors directly to ground (respectively PMOS to Vcc) without a significant loss of accuracy.

Finally the full resulting network after inter and intra-block methodology application is illustrated in Figure 2-8.

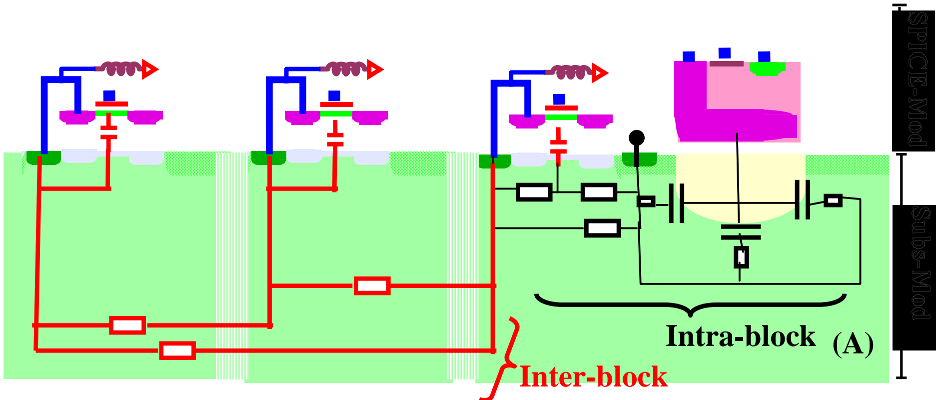


Figure 2-8 : MS-SOC substrate model example with inter-block and intra-block resulting network.

2.4 Methodology for a final optimization

The final stage of ou methodology is named **SubCirII,** and its flowchart described in Figure 2-9. In this approach, we use the full package and substrate model in an iterative verification procedure of large varieties of isolation strategies. The visited strategies are those mentioned in section I, that is: floorplanning, guard ring placement, pinning strategy, etc. This methodology will enable us to achieve the best noise rejection, by choosing the best isolation techniques for a given technology, circuit and package. We can also verify if we can meet the attenuation specified in SubCirI without changing the package or splitting the digital and the analog parts of the circuits.

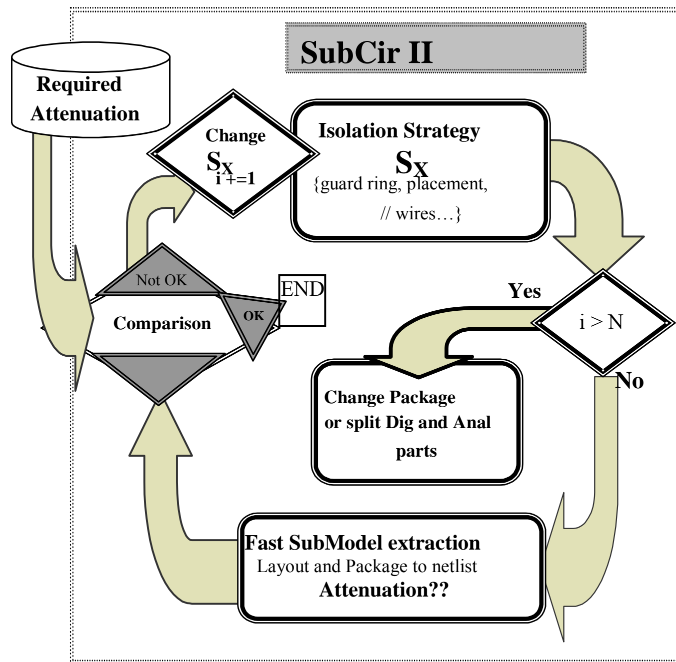


Figure 2-9 : Flow diagram of SubCirII methodology.

The attenuation between sensitive and perturbing parts of the circuits depends essentially on substrate, package, and wire parasitics. The simplified substrate model validated in Section 2.3.1 fits very well the low computational efforts and accuracy requirements of this iterative method. In fact, the verification and comparison of large variety of isolation strategies are necessary to achieve the best noise rejection. Therefore, we will use a suite of tools based on numerical finites-differences method (FDM) SubstrateStorm after simplifying the Layout as explained in section 2.3.1. The base feature of the numerical method (FDM) is the high accuracy of the generated 3D-substrate model, since it can handle lateral and vertical resistivity variations and also arbitrary substrate geometry.

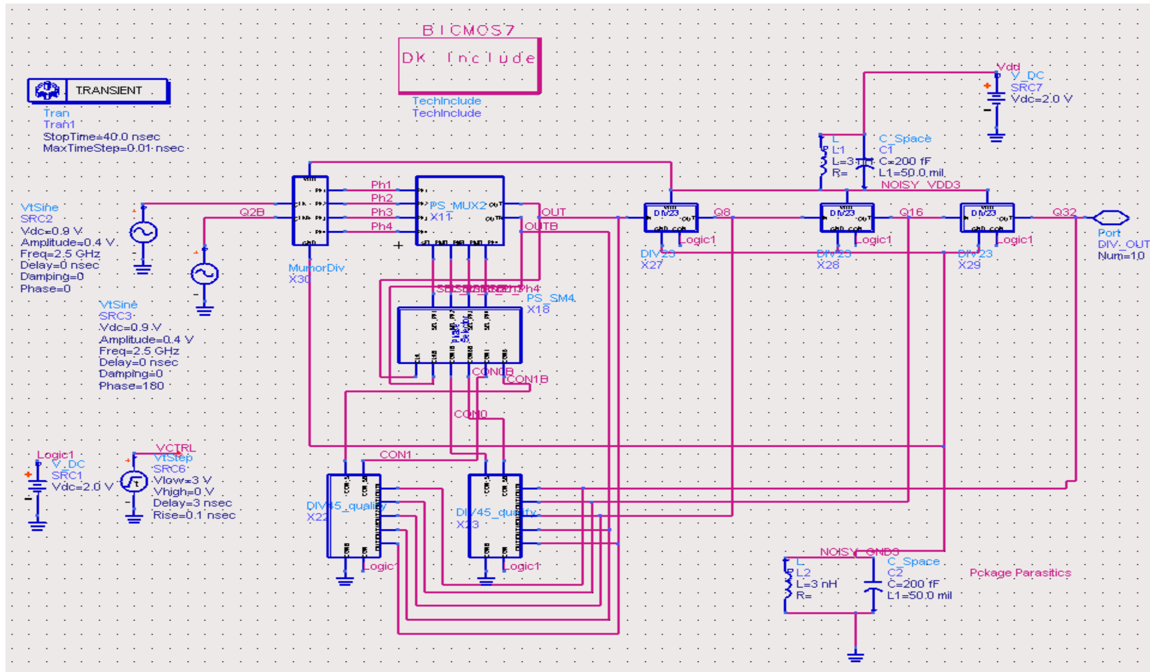
2.5 Case study

The main purpose of this section is to present some examples of the substrate analysis that are going on currently within MuMor project. The first study will show how to use the methodology, SubCirI, to help a single-chip integration of the synthesizer. According to our methodology (Figure 2-1), we focus on the oscillator as the potential “listener” and the Prescaler/Divider of the PLL as the possible “talker”. The divider is a continuously programmable 64 to 127 and their blocks diagram is shown in Figure 2-10. The divider and the oscillator (shown in Figure 2-11) was designed by EPFL to meet the specification of the Multi-mode (GSM-UMTS-HSPDA “TDD and FDD”) transceiver. The noise generated by the divider is shown in Figure 2-10. For the oscillators, this environmental noise translates to spurs by frequency modulation FM phenomena. In fact, the noise corrupts the dc voltage applied across the varactors, and varies the tank capacitance and hence the resonance frequency. Viewed as analog FM, this effect translates low-frequency noise components in the control path to region around the carrier. The example of spurious tones generated by the divider noise when arriving without attenuation to the control path of our oscillator is shown in Figure 2-11. In general, to preserve

a required SNR in the adjacent channels, we can specify the maximum spurious tones that can be tolerated at different frequency offsets from the carrier. By comparing those maximum tolerated values with the spurious tones of Figure 2-11 we can decide if we should redesign sensitive sections (e.g. VCO) to be more robust. We can also redesigning perturbing sections (e.g. Divider) to generate less noise. Eventually, the noise attenuation required to save the basic functionality of the system will be estimated. All those analyses were currently under study, and will be used to estimate the failure risk as a function of the circuits topology, isolation strategies and the package used.

2.6 Conclusion

EPFL has focused on the development of methodologies for the analysis and optimization of substrate noise effects in RF mixed-signal circuits. The main results were published in the IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems journal [10]. Two methodologies were elaborated: one for an early design verification, and another for a final verification/optimization of the noise immunity of the circuits. A new approach, which combines a thorough physical comprehension of the noise coupling effects and accurate 3D substrate modeling tools and significantly accelerates the substrate model extraction and enables the use of the iterative optimization procedure, is proposed. These methodologies will be employed to verify the functionality of the components of the MuMor RF system, and to make sure that they meet the specified figures of merit before being assembled together. The RX/TX integration capabilities for full duplex radios will be investigated to optimize area and cost by studying the impact of the different isolation strategies and by choosing the best radio subsystem partitioning. The priority will be the full integration of the frequency synthesizer.



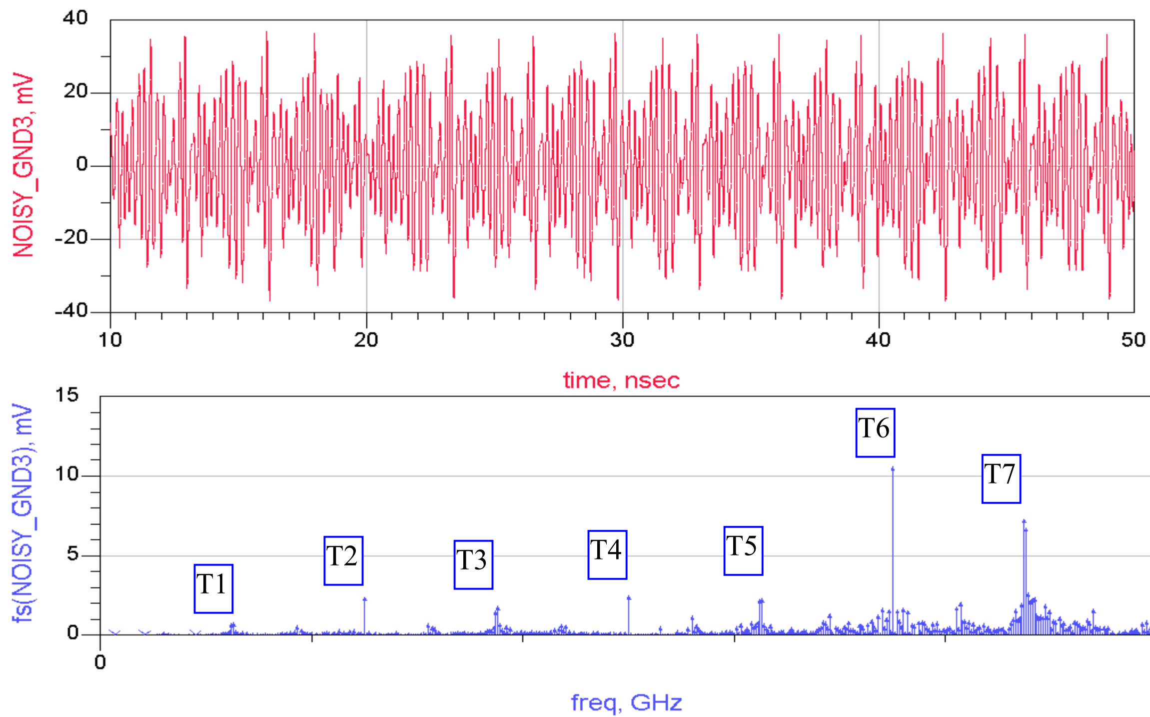
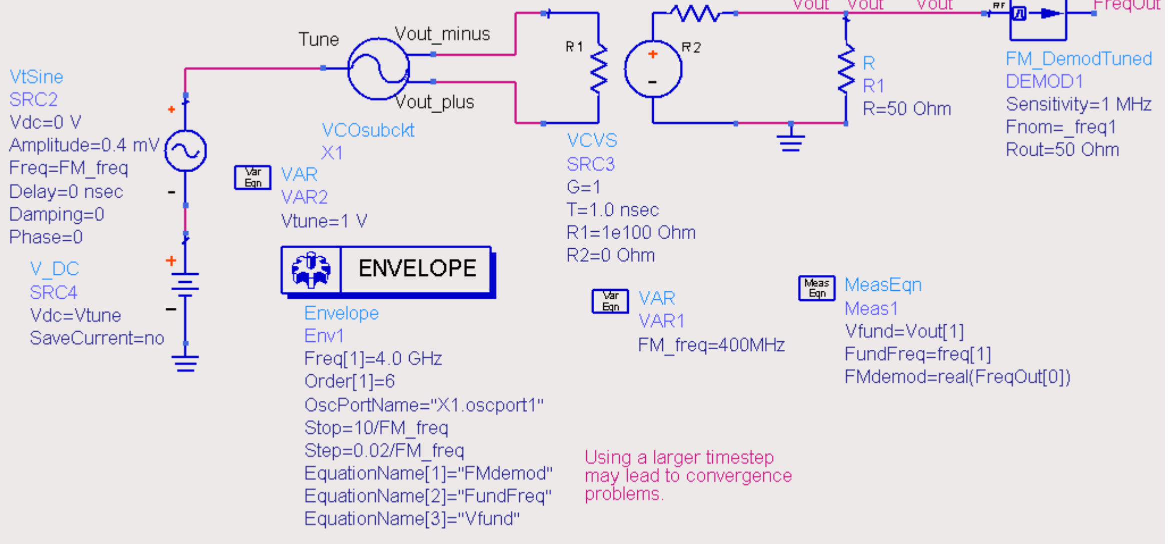


Figure 2-10 : Divider diagram blocks and its on-chip ground noise waveform and spectrum.



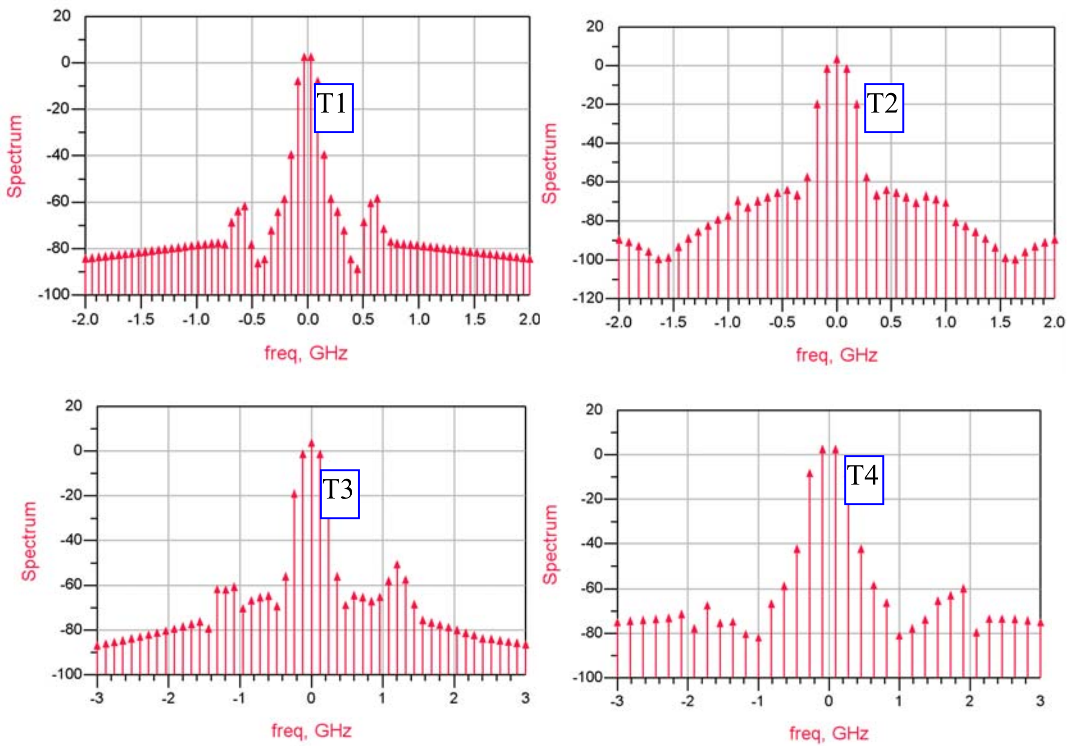


Figure 2-11 : FM spurs generated at the output of the VCO by the tones 1, 2, 3 and 4 of the divider noise.

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