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Digital Baseband Architecture Scenarios for a Multi -Mode Radio

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Abstract:

The main target of this task is the development of a multi -mode system architecture for the digital baseband part of a UMTS/TDD/FDD and HSDPA/FDD system. Future standard enhancements will be taken into account. Therefore a detailed block diagram of the target system has to be developed, showing the needed system functions, their parameters and requirements. The ultimate goal of the digital baseband architecture is a multi -mode, i.e. soft -configurable architecture, and the system architecture design will reflect this.

Keyword list: UMTS, HSDPA, FDD, TDD, Multi -mode, Architecture

Abbreviations/Terminology

ACK	Acknowledge
ADC	Analog to Digital Converter
BMC	Broadcast Multicast Control (optional, not implemented here)
BW	Bandwidth
CCSS	CoCentric System Studio (also simply called System Studio)
CDMA	Code Division Multiple Access
CPICH	Common Pilot Channel
CQI	Channel Quality Indicator
CRC	Cyclic Redundancy Check
DAC	Digital to Analogue Converter
DL	Down-Link
DPCCH	Dedicated Physical Control Channel
DPCH	Dedicated Physical Channel
DPDCH	Dedicated Physical Data Channel
FDD	Frequency Division Duplex
H-ARQ	Hybrid Automatic Repeat Request
HSDPA	High Speed Downlink Packet Access
HS-DPCCH	High Speed Dedicated Physical Control Channel
HS-PDSCH	High Speed Physical Downlink Shared Channel
HS-SCCH	High-Speed Shared Control Channel
IF	Intermediate Frequency
ISI	Inter-Symbol-Interference
L1	Physical layer as defined by 3GPP, also called PHY
L2	Protocol layer consisting of MAC, RLC, PDCP and BMC as defined by 3GPP
LLR	Log Likelihood Ratio
MAC	Medium Access Control
MAI	Multiple Access Interference
Mbps	Mega Bit Per Second
Mcps	Mega Chips Per Second
MMSE	Minimum Mean Square Error
MOSI	Multiple-Output-Single-Input. The term 'DL MOSI diversity' refers to STTD (two transmit antennas at Node B) and cell macro diversity.
NACK	Not Acknowledge

OVSF	OrthogonalVariableSpreadingFactor
P-CCPCH	PrimaryCommonControlPhysicalChannel
PDCP	PacketDataConvergenceProtocol
PHY	Physicallayerasdefinedby3GPP,alsocalledL1
P-SCH	PrimarySynchronizationChannel
QAM	QuadratureAmplitudeModulation
QPSK	QuadraturePhaseShiftKeying
RF	RadioFrequency
RLC	RadioLinkControl
RRC	RadioResourceController
RRCos	RootRaisedCosineFilter
Rx	ReceiverorReceived,dependsonthecontext
SIR	SymboltoInterferenceRatio
S-SCH	SecondarySynchronizationChannel
TDD	TimeDivisionDuplex
Tx	TransmitterorTransmitted,dependsonthecontext
UARFCN	UTRAAbsoluteRadioFrequencyChannelNumber
UE	UserEquipment
UL	Uplink
UTRAN	UMTSTerrestrialRadioAccessNetwork
WCDMA	WidebandCDMA

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1 Introduction

In this document an overall multi-mode architecture of the mobile terminal covering three modes, namely UMTS/FDD, UMTS/TDD, and HSDPA/FDD will be proposed. First of all, system requirements of the multi-mode re-configurable terminal will be presented. In order to explore and develop a re-configurable architecture, so many typical features specified in the standards need to be supported. In this way the required effort can be put in the scope of the project.

Before going into multi-mode architecture, each single-mode architecture will be examined separately, so that a clear understanding of the unique features of each mode and the similarities among all the three modes can be acquired. Then, a matrix-like block diagram will be proposed. Each row of this matrix refers to a specific mode, i.e. standard, and each column consists of all the similar functions belonging to different modes. The grouping of identical functions into columns will be done at functional level. Further column partitioning by further inspections in areas such as required processing speed, memory, and data size will be considered.

Interfacing between front-end and baseband parts in multi-mode system is of more importance than in the single mode system. Re-configurability and multi-mode features are the target for both parts, and their interfaces should reflect that. Here a general interface that is well capable of coping with the evolution of the front-end and baseband parts will be described. Also channel models for the verification of the different functionalities of the multi-mode system will be specified.

2 System Requirements

The system requirements for the supported modes will be defined here. This implies the definition of the 3GPP capability parameters as well as restriction to the standard in terms of supported physical channels and physical layer procedures and measurements, etc. The result is a list of all given operational modes and functionalities including the corresponding parameters.

2.1 Transmitter/Receiver Chains and Physical Channels to be implemented

When considering the different 3GPP modes UTS FDD and UMTS/TDD (3.84 Mcps) plus the corresponding HSDPA enhancements there are several different transmitter chains and corresponding receiver chains, which could be implemented. For the model implementation a reduction of these modes will be made by only supporting one of the TDD modes, which is the 3.84 Mcps UMTS TDD. Additionally it has to be distinguished between the implementation for the final design and the implementation mostly for the verification. Latter might be less optimised or reduced in functionality.

In this activity the focus is on terminal side. Thus UE Tx and Rx are preferably considered in the reference model for multi-mode implementation and in the selection of key IPs for implementation. However, model of UTRAN Rx and Tx are required for UE verification with at least having the functionality, which is required to act as a functional counterpart for the UE models in the test bench.

Table 2.1 shows, which of the possible Tx and Rx chains will be implemented for the design model and which will be implemented mostly for verification purposes.

	UMTS FDD		HSDPA FDD		UMTS TDD
	Uplink (UL)	Downlink (DL)	Uplink (UL)	Downlink (DL)	UL/DL
Transmitter chain	Design model	Focus on verification	Design model	Focus on verification	Design model
Receiver chain	Focus on verification	Design model	Focus on verification	Design model	Design model

Table 2.1: Transmitter and receiver chains to be implemented

Table 2.2 shows the implemented physical channels in uplink and downlink and their implementation in more detail.

Figure 2.1 shows

	UMTS FDD	HSDPA	UMTS TDD
Downlink	DPDCH/DPCCH CPICH P-SCH S-SCH	HS-PDSCH HS-SCCH	DPCH P-SCH S-SCH P-CCPCH
Uplink	DPDCH DPCCH	HS-DPCCH	DPCH

Table 2.2: Implemented physical channels

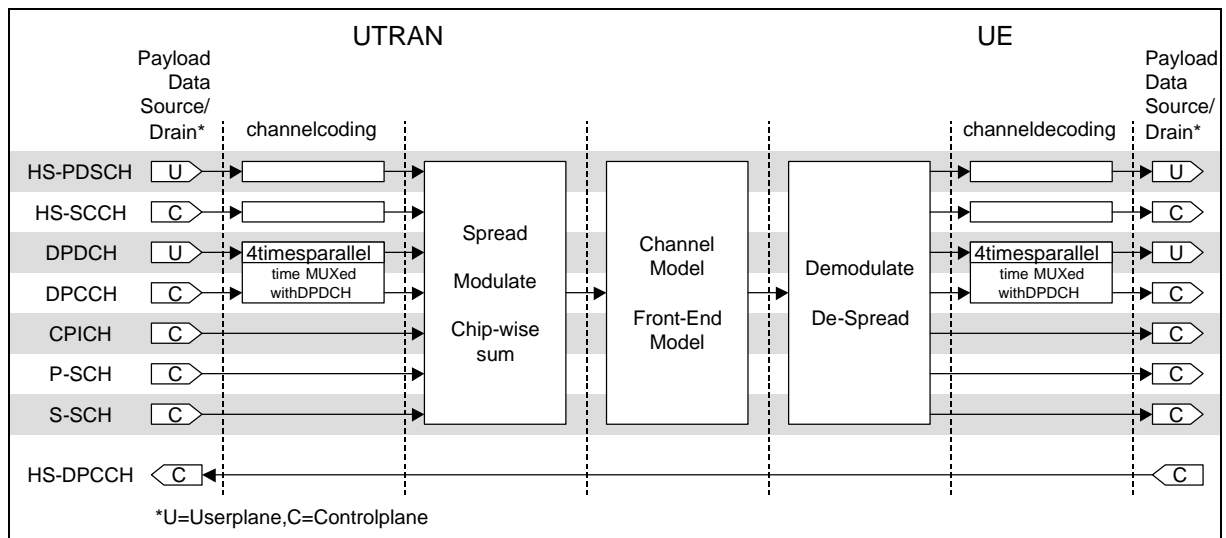


Figure 2.1: Physical channels implementation overview

2.2 High-level System Requirements

2.2.1 General

- The functional implementation is compliant with 3GPP Release 5
- Downlink Tx and Rx modems are supposed to use direct conversion
- Support for multiple dedicated data channels enabling concurrent applications
- Use a channel equalizer or other advanced receiver techniques at the DL Rx to reduce the chip interference compared to RAKE
- Rx synchronisation features:
 - Frame and slots synchronisation
 - Frequency synchronisation
 - Timing synchronisation
- Static link configuration at simulation start, no automatic link adaptation through higher layer assignment
- Complete wireless downlink simulated (all downlink channels through channel model and receiver model); uplink will be simplified
- Not supported:
 - Any handover related procedures and other requirements
 - Any power control related procedure and other requirements
 - Connection set-up (radio link establishment and release)
 - Flexible position of TrCHs in CCTrCh
 - Beamforming
 - MIMO
 - Tx diversity

2.2.2 UMTSFDDSSpecific

- None, the general requirements from the chapter above apply here

2.2.3 UMTSTDDSSpecific

- Not supported: Timing Advance procedure for UL

2.2.4 HSDPASpecific

- The packet data transmission rate of up to 10 Mbps in HSDPA mode should be examined and supported if feasible
- Two modulation schemes: 16-QAM and QPSK
- H-ARQ support

2.3 Higher Layer Interface

The physical layer interacts directly with the MAC layer and the RRC layer. Status and control primitives are exchanged to set up and configure radio bearers, to report measurements, to exchange data for transmission or data that has been received, and for further purposes.

This chapter describes the services, needed to interact with the RRC and MAC layer. All corresponding information elements have to be previously known by L1 and provided by higher layers or are measurement results (see 3GPP TS 25.331).

The list of the primitives listed here represents the information, which has to be exchanged between the physical layer and the protocol layers. The final implementation in the system has to be defined in detail.

2.3.1 Primitives between physical layer and MAC layer

The following primitives are used to enable signaling between MAC and physical layer.

Requirement (Reference: 3GPP TS 25.302)	MuMoR System Support
10.1.1 PHY -Access-REQ	Not supported
10.1.2 PHY -Access-CNF	Not supported
10.1.3 PHY -Data-REQ	Supported
10.1.4 PHY -Data-IND	Supported
10.1.5 PHY -CPCH_Status-REQ	Not supported
10.1.6 PHY -CPCH_Status-CNF	Not supported
10.1.7 PHY -Status-IND	Supported

Table 2.3: Primitives between L1 and MAC

2.3.2 Primitives between physical layer and RRC layer

The following primitives are used to enable signaling between RRC and physical layer.

Requirement (Reference: 3GPP TS 25.302)	MuMoR System Support
10.2.1.1 CPHY -Sync-IND	Supported
10.2.1.2 CPHY -Out-of-Sync-IND	Supported

Requirement (Reference:3GPPTS25.302)	MuMoRSystemSupport
10.2.1.3CPHY -Measurement-REQ	Supported
10.2.1.4CPHY -Measurement-IND	Supported
10.2.1.5CPHY -Error-IND	Notsupported
10.2.1.6CPHY -CPCH-EOT-IND	Notsupported
10.2.2.1CPHY -TrCH-Config-REQ	Supported
10.2.2.2CPHY -TrCH-Config-CNF	Supported
10.2.2.3CPHY -TrCH-Release-REQ	Notsupported
10.2.2.4CPHY -TrCH-Release-CNF	Notsupported
10.2.2.5CPHY -RL-Setup-REQ	Supported
10.2.2.6CPHY -RL-Setup-CNF	Supported
10.2.2.7CPHY -RL-Release-REQ	Notsupporte d
10.2.2.8CPHY -RL-Release-CNF	Notsupported
10.2.2.10CPHY -RL-Modify-CNF	Notsupported
10.2.2.11CPHY -Commit-REQ	Notsupported
10.2.2.12CPHY -CPCH-Estop-IND	Notsupported
10.2.2.13CPHY -CPCH-Estop-RESP	Notsupported
10.2.2.14CPHY -CPCH-Estop-REQ	Notsupported
10.2.2.15CPHY -CPCH-Estop-CNF	Notsupported
10.2.2.16CPHY -Out-of-Sync-Config-REQ	Supported
10.2.2.17CPHY -Out-of-Sync-Config-CNF	Supported

Table 2.4:PrimitivesbetweenL1andRRC

2.4 PhysicalLaye rProcedures

InthephysicallayerofaCDMAsystemtherearemanyproceduresessentialforthesystemoperation. These procedures have been naturally shaped by the CDMA -specific properties of the physical layer. Procedures are defined in 3GPPTS25.214 for the FDD and in 3GPPTS25.224 for the TDD option.

Table 2.5 gives an overview of defined procedures and how they will be supported in the MuMoR project for the FDD and TDD options.

Procedure	FDD	TDD	MuMoRSystem Support
SynchronisationProcedure	X	X	Partialsupport:Noradiolinkrelease andestablishment,onlymonitoring . Mainlycoveringthecellsearch
Powercontrol	X	X	Notsupported
Randomaccess	X	X	Notsupported
TransmitDiversity	X	X	Notsupported
IPDLlocation	X	X	Notsupported
TimingAdvance	-	X	Notsupported

NodeB Synchronization	-	X	Not supported
Discontinuous transmission	-	X	Not supported
DSCH Procedure	-	X	Not supported
HS-DSCH related procedure	X	X	Partial support: No compressed mode. Only FDD mode

Table 2.5: Support of physical layer procedures

As the MuMoR project is concentrating on the multi-mode aspects of UMTS/FDD, TDD and HSDPA/FDD and its impact on the signal processing architecture, the target implementation will consider only the synchronization procedure (mainly the cell search) from the UMTS system and the HS-DSCH procedure for the HSDPA/FDD option. Instead of signal processing most of the other procedures are based on control processing (State Machines).

2.5 UE Physical Layer Measurement Abilities

This chapter describes all necessary minimum requirements to fulfil the UE's L1 task to serve measurement requests of higher layers in the UE and UTRAN. The following measurement specifications apply to the UE in FDD mode, being neither a GSM nor GPRS capable terminal.

The level of support of physical layer measurements performed by the UE and reported to higher layers are defined. Only measurements are supported, which are required by the supported procedures and can be performed because the required physical channels are supported. Some measurements are relevant for both FDD and TDD mode. The measurements are defined in TS 25.215 for the FDD and in TS 25.225 for the TDD mode.

Table 2.6 gives an overview of defined measurements and how they will be supported in the MuMoR project.

Measurement	FDD	TDD	MuMoR System Support
CPICH RSCP	X	X	Not supported
CPICH Ec/No	X	X	Not supported
SIR	-	X	Not supported
Transport channel BLER	X	X	Supported
UTRA carrier RSSI	X	X	Not Supported
UE transmitted power	X	X	Not Supported
SFN-CFN observed time difference	X	X	Not Supported
SFN-SFN observed time difference	X	X	Not Supported
UE Rx - Tx time difference	X	-	Not Supported
P-CCPCH RSCP	X	X	Not Supported
Time slot ISCP	-	X	Not supported

Table 2.6: Support of UE measurement abilities

The unsupported measurements are mostly related to frequency and cell handover or power control and therefore not implemented.

2.6 UE Capability Parameters

UEs are not fully specified in terms of their radio access capability. To allow UEs of different complexities and capabilities being 3GPP compliant an amount of parameters has been defined

together with a range and granularity of valid values for each of them. UTRAN needs to respect the UE capabilities when configuring the radio bearers.

The capability parameters have to be considered separate from the physical layer parameters, which all have to be supported by any fully compliant implementation. The following table lists the UE radio access capability parameters, which are relevant for the physical layer base -band in FDD uplink and FDD downlink. For a more detailed definition of the parameters please refer to the 3GPP TS 25.306 document.

2.6.1 UMTS FDD/TDD Capability Parameters

The figures given here have been taken from the TS 25.306. The same document also gives reference to UE radio access capability combinations for all of the values to be used for test specifications and for conformance testing against reference radio access bearer (RAB) as well as more detailed explanation of the UE radio access capability parameter description used in Table 2.7.

The target system values given in Table 2.7 are for the reference simulation model. The performance capabilities for the HW/SW demonstrator might be lower due to implementation restrictions.

Relevance	UE radio access capability parameter	Value range	MuMoR System Value
Transport channel parameters in downlink	Maximum sum of number of bits of all transport blocks being received at an arbitrary time instant	640,1280,2560,3840,5120,6400,7680,8960,10240,20480,40960,81920,163840	163840
	Maximum sum of number of bits of all convolutionally coded transport blocks being received at an arbitrary time instant	640,1280,2560,3840,5120,6400,7680,8960,10240,20480,40960,81920,163840	163840
	Maximum sum of number of bits of all turbo coded transport blocks being received at an arbitrary time instant	640,1280,2560,3840,5120,6400,7680,8960,10240,20480,40960,81920,163840	163840
	Maximum number of simultaneous transport channels	4,8,16,32	4
	Maximum number of simultaneous CCTrCH	1,2,3,4,5,6,7,8	1
	Maximum total number of transport blocks received within TTI that end within the same 10 ms interval	4,8,16,32,48,64,96,128,256,512	512
	Maximum number of TFC	16,32,48,64,96,128,256,512,1024	1024
	Maximum number of TF	32,64,128,256,512,1024	1024
	Support for turbo decoding	Yes/No	Yes

Relevance	UE radio access capability parameter	Value range	MuMoR System Value
Transport channel parameters in uplink	Maximum sum of number of bits of all transport blocks being transmitted at an arbitrary time instant	640,1280,2560,3840,5120,6400,7680,8960,10240,20480,40960,81920,163840	163840
	Maximum sum of number of bits of all convolutionally coded transport blocks being transmitted at an arbitrary time instant	640,1280,2560,3840,5120,6400,7680,8960,10240,20480,40960,81920,163840	163840
	Maximum sum of number of bits of all turbo coded transport blocks being transmitted at an arbitrary time instant	640,1280,2560,3840,5120,6400,7680,8960,10240,20480,40960,81920,163840	163840
	Maximum number of simultaneous transport channels	2,4,8,16,32	2
	Maximum number of simultaneous CCH of DCH type (TDD only; for FDD there is always one CCH at a time)	1,2,3,4,5,6,7,8	1
	Maximum total number of transport blocks transmitted within TTI that start at the same time	2,4,8,16,32,48,64,96,128,256,512	512
	Maximum number of TFC	4,8,16,32,48,64,96,128,256,512,1024	1024
	Maximum number of TF	32,64,128,256,512,1024	1024
	Support for turbo encoding	Yes/No	Yes
FDD Physical channel parameters in downlink	Maximum number of DPCH/PDSCH codes to be simultaneously received	1,2,3,4,5,6,7,8	8
	Maximum number of physical channel bits received in any 10 ms interval (DPCH, PDSCH, SCCPCH)	600,1200,2400,3600,4800,7200,9600,14400,19200,28800,38400,48000,57600,67200,76800	76800
	Support for SF512	Yes/No	Yes
	Support of PDSCH	Yes/No	No
	Simultaneous reception of SCCPCH and DPCH	Yes/No	No

Relevance	UE radio access capability parameter	Value range	MuMoR System Value
	Simultaneous reception of SCCPCH, DPCH and PDSCH	Yes/No	No
	Maximum number of simultaneous S-CCPCH radio links	1	1
	Support of dedicated pilots for channel estimation	Yes/No	Yes
FDD Physical channel parameters in uplink	Maximum number of DPDCH bits transmitted per 10ms	600,1200,2400,4800,9600,19200,28800,38400,48000,57600	57600
	Support of PCPCH	Yes/No	No
TDD 3.84 Mcps physical channel parameters in downlink	Maximum number of time slots per frame	1..14	14
	Maximum number of physical channels per frame	1,2,3..224	224 (16 codes * 14 time slots)
	Minimum SF	16,1	16 (SF 1 not supported)
	Support of PDSCH	Yes/No	No
	Maximum number of physical channels per time slot	1..16	16
TDD 3.84 Mcps physical channel parameters in uplink	Maximum Number of time slots per frame	1..14	14
	Maximum number of physical channels per time slot	1,2	1
	Minimum SF	16,8,4,2,1	16 (others not supported)
	Support of PUSCH	Yes/No	No

Table 2.7: Value ranges for the physical layer radio access capability parameters

2.6.2 HS-DSCH Capability Parameters

For the UE supporting HSDPA mode several capability parameters have been defined. Other than for UMTS the valid values of these parameters cannot be chosen freely. A predefined HS-DSCH category defined by a fixed combination of capability parameters has to be chosen. The HS-DSCH UE capabilities are reclassified according to the following categories:

HS-DSCH category	Maximum number of HS-DSCH codes received	Minimum interval -TTI	Maximum number of bits of an HS-DSCH transport block received within an HS-DSCH TTI	Total Number of soft channel bits
Category 1	5	3	7300	19200
Category 2	5	3	7300	28800

Category3	5	2	7300	28800
Category4	5	2	7300	38400
Category5	5	1	7300	57600
Category6	5	1	7300	67200
Category7	10	1	14600	115200
Category8	10	1	14600	134400
Category9	15	1	20432	172800
Category10	15	1	28776	172800

Table 2.8:FDDHS -DSCHphysical layercategories

Theselectedcategoryforthe targetsystemiscategory10,asdescribedin Table 2.9.

HS-DSCH category	Maximumnumber ofHS -DSCH codesreceived	Minimuminter -TTI interval	Maximumnumberofbits ofanHS -DSCHtransport blockreceivedwithinan HS-DSCHTTI	TotalNumberof softchannelbits
Category10	15	1	28776	172800

Table 2.9:TheselectedFDDHS -DSCHphysical layercategory

3 Overview of the Constituting Singlemode Architectures

3.1 Baseband Architecture for UMTS/FDD

A general description of the link level for UL/DL of UMTS/FDD will be presented here, and functionality of the constituent blocks will be described. This section will give a clear understanding of the receiver algorithms in UMTS/FDD mode.

3.1.1 Baseband Signal Processing

An architectural overview of the baseband signal processing of UMTS/FDD will be given in this section.

The operational blocks within both receiver and transmitter are grouped based on the signal type that they process (sample, chip, physical channel and transport channel) and on their functional role (processing control or just processing). Table 3.1 and Table 3.2 show the receiver and transmitter operational block grouping.

	Sample Processing	Chip Processing	Physical Channel Processing	Transport Channel Processing
Rx Signal Processing Control	<ol style="list-style-type: none"> Rx Gain Controller. D.L Time Controller. Cell Searcher. 	<ol style="list-style-type: none"> Multipath Searcher and Channel Estimator. DL Training Sequences, Pilots and Codes Signatures Generator. Frequency Offset Estimator. 		<ol style="list-style-type: none"> CRC Check
Rx Baseband Signal Processing	<ol style="list-style-type: none"> A.D.C. Rx Pulse Shaper. Feedback Frequency Synchroniser. 	<ol style="list-style-type: none"> RAKE Receiver Forward Frequency Synchronizer. DL Soft Bit Mapper 	<ol style="list-style-type: none"> Physical Channel De-Mapper. 2nd De-Interleaver. Physical Channel De-Segmentation. Transport Channel De-Multiplexer. 	<ol style="list-style-type: none"> Radio Frame De-Segmentation. 1st De-Interleaver. DTX Removal. Rate De-Matching. Channel Decoder. Transport Block De-Concatenation and Code Block Desegmentation.

Table 3.1: Blocks within Baseband Receiver Signal Processing and Control for UMTS/FDD

	Sample Processing	Chip Processing	Physical Channel Processing	Transport Channel Processing
Tx Signal Processing	<ol style="list-style-type: none"> Tx Gain Controller. 	<ol style="list-style-type: none"> UL Pilots and Codes Signatures 		

Processing Control	Controller.	CodesSignatures Generator.		
Tx Baseband Signal Processing	1. PulseShaper. 2. TxTruncator 3. DAC	4. Spreaderand Modulator.	5. Transport Multiplexer. 6. PhysicalChannel Segmentation. 7. 2 nd Interleaver. 8. PhysicalMapper.	9. CRCAttachment. 10.TransportBlock Concatenationand CodeBlock Segmentation. 11.ChannelCoder. 12.RadioFrame Equalizer. 13.1 st Interleaver. 14.RadioFrame Segmentation. 15.RateMatching.

Table 3.2:BlockswithinBasebandTransmitterSignalProcessingandControlforUMTS/FDD

Figure 3-1showsthe‘BasebandReceiverSignalProcessingandControl’ signalflow,where:

- ❑ ‘AnalogueRxSignal’ isthereceivedsignalfromtheRF FrontEnd
- ❑ ‘RxSetGain’ representstherequiredRFgaininordertooperatetheADCsatoptimumscalegain
- ❑ ‘FeedbackControlParameters’ usedforclose -loopfrequencyandtimecontrol.
- ❑ ‘CellParameters’ forUTRAFDDthisisjustthescramblingcodenumberthatwillbeusedto generateDLTrainingSequences,PilotsandCodesSignatures(scramblingandOVSFcodes).
- ❑ ‘PhysicalChannelsSoftBits’ arethebitmappedcodechannelsymbols.
- ❑ ‘TrChDe -MuxSoftBits’ arethede -multiplexedTransportchannelssoftbits.
- ❑ ‘ReceivedDLData’ representsthereceived,decodedandCRCcheckedinformationbits.

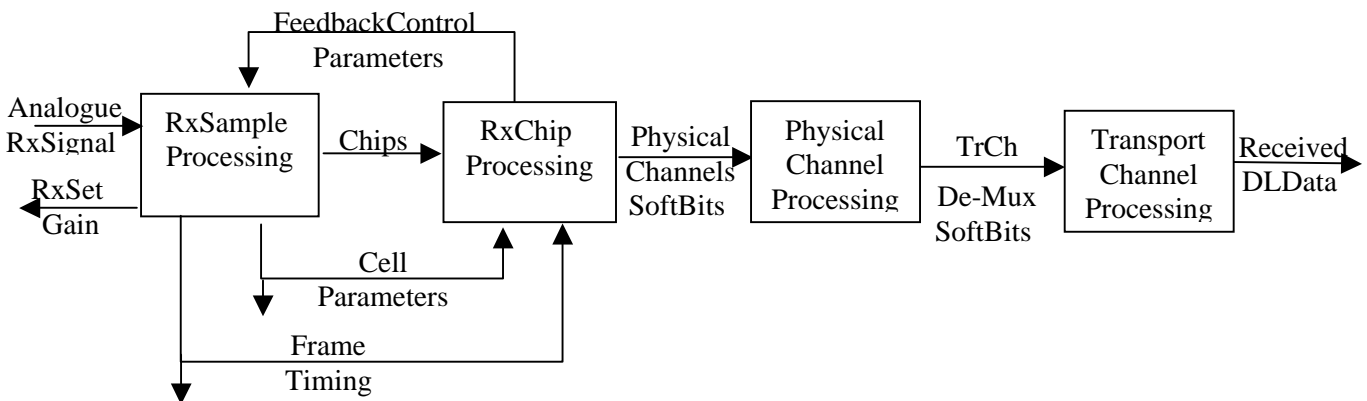


Figure 3-1:BasebandReceiverSignalProcessingandControl,SignalFlow

Figure 3-2 showsthe‘BasebandTransmitterSignalProcessingandControl’ signalflow,where:

- ❑ ‘ULData’ representsthehigherlayerdatathathastob e transmittedon uplink.
- ❑ ‘TrChRateMatchedBits’ aretheratematchedTransportchannelsbits.
- ❑ ‘PhysicalChannelsBits’ arethebitsthathavetobymappedto codechannelsymbols,modulated andspread.

- 'AnalogueTxSignal' is the signal sent to the RF -Front End transmitter.
- 'CodeChannelsGains' and 'TxPower' are the code channel normalized gains and the required transmission power. These are used to set the transmitter gains.

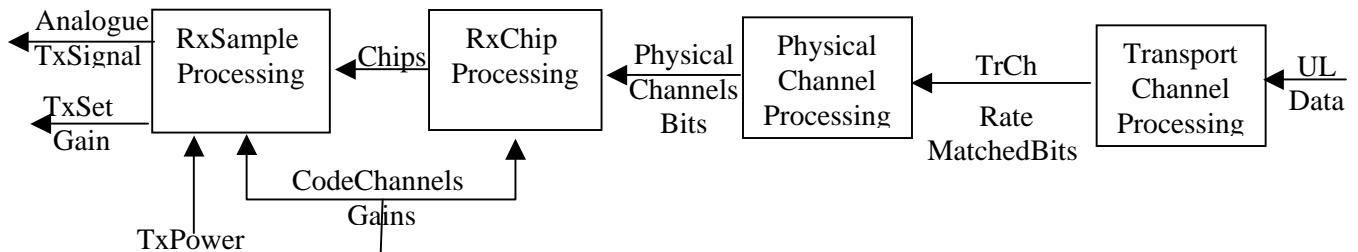


Figure 3-2: Baseband Transmitter Signal Processing and Control, Signal Flow

3.1.2 FDD Baseband Sample Processing

Figure 3-3 shows the signal flow within the 'Transmitter Baseband Sample Processing' where the process flow could be described as follows:

- The Up link 'chips' to be transmitted are pulse shaped and rate converted by the 'Tx Pulse Shaper'.
- The pulse shaped samples are bit equalized at an optimum word length by the 'Tx Truncator'.
- The level of word truncation of the 'Complex Samples' is set by the 'Tx Gain Controller' and will depend on the normalized gains of the code channels ('Code Channels Gains') describing the uplink physical channel.
- Finally the digital samples are converted to the 'Analogue Tx Signal' by the DACs and the 'RF Front-End' gain is set by the 'Tx Gain Controller'.

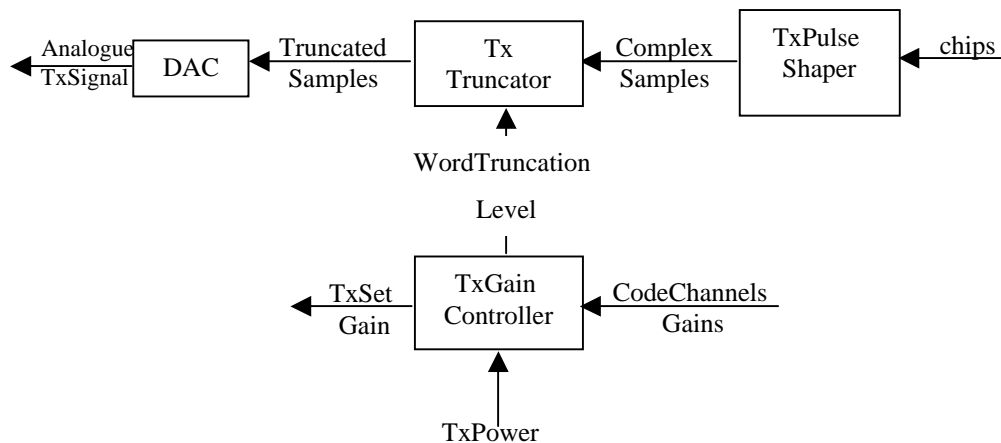


Figure 3-3: Transmitter Sample Processing, Signal Flow

Figure 3-4 shows the signal flow within the 'Receiver Baseband Sample Processing'. Process flow wise, the 'Receiver Sample Processing' could be described as follows:

- The gain seen at the ADC input is measured and controlled by the 'Rx Gain Controller'.
- Assuming an 'early -late' close -loop time control, the 'Early, In -time and Late Chips Fingers' are obtained by the 'Rx Pulse Shaper' which filters and decimates the 'Complex Samples' to chip rate. The chip finger offset ('DL Chip Offsets') and the frame timing are readjusted by the 'DL Time Controller' based on the multipath gains (MPGains) feedback.
- The 'Initial Timing' and the 'Cell Parameters' are given by the 'Cell Searcher'.

- Finally the chip fingers are frequency synchronized and sent to the 'RxChipProcessing'.

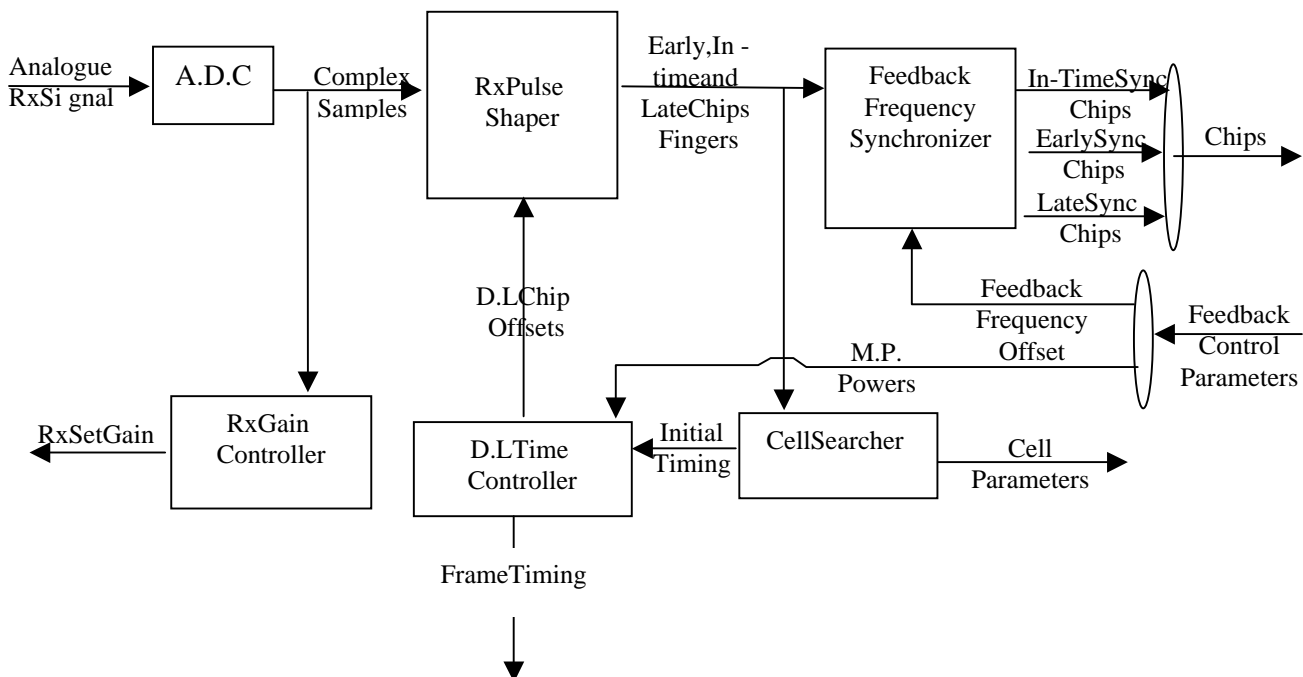


Figure 3-4: Receiver Sample Processing, Signal Flow

3.1.2.1 Pulse Shaping (Transmit and Receive)

The pulse shaping filter at the transmitter is specified in 3GPP 25.101 as a root-raised-cosine (RRCos). Transmit and receive pulse shaping filters together, try to minimize the inter-chip-interference, by satisfying the Nyquist criterion through the appropriate raised cosine pulse shaping. However, some amount of inter-chip-interference will still be induced through the frequency selective behaviour of the multipath channel.

Figure 3-5 and Figure 3-6 show the typical signal processing for transmitter and receiver pulse shaping elements. The receiver delay element is controlled by the receiver 'DL Time Controller' in order to maximize the SIR at the output of the RAKE receiver.

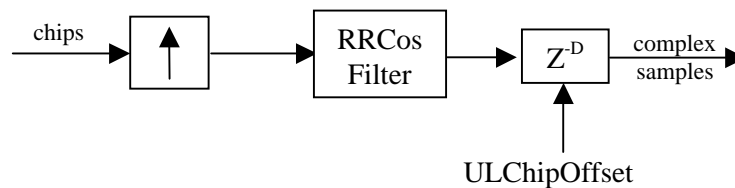


Figure 3-5: Typical Tx pulse shaping (controlled delay for TDD only)

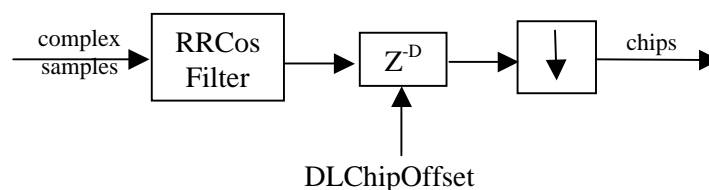


Figure 3-6: Typical Rx pulse shaping (controlled delay for both FDD and TDD)

For UL (transmitting) only one pulse shaping element exists at all times. For DL there could be more than one DL sources with different chip offsets (if DL diversity is considered). A way to minimize

the number of 'Pulse Shaping Elements' required, is to use a union based method for generating chips with same offsets, but allocated to different sources.

3.1.2.2 Cell Searching

The purpose of Initial Cell Searcher is to acquire timing information of the nearest (or strongest) base station. In 3GPP specifications, there are 2 synchronization channels used in the downlink of each cell, namely as Primary Synchronization Channel (P-SCH) and Secondary Synchronization Channel (S-SCH). There is also a common pilot channel (CPICH). Cell search process consists of 3 steps using these 3 channels for synchronization, code group identification and cell identification. The first step is to find slot timing using P-SCH, the second step is to find frame timing and code group using S-SCH, and the third step is to identify the cell specific scrambling code using CPICH. During STEP 3 of the cell search procedure, the UE determines the exact primary scrambling code used by the found cell. The primary scrambling code is typically identified through symbol-by-symbol correlation over the CPICH with all codes within the code group identified in STEP 2. There are 8 scrambling codes in each code group. After the primary scrambling code has been identified, the Primary CCPCH can be detected. And the system and cell specific BCH information can be read.

If the UE has received information about which scrambling codes to search for, steps 2 and 3 above can be simplified.

3.1.2.3 DL Time Control

This block tracks the time varying delay of each path associated with the fingers of the rake receiver. This tracking can be based on early-late delay discriminator approach. In this approach, the metrics for time control are the 'M.P. Gains', which are the power sums of the 'early', 'in-time' and 'late' multipath weights (see section 3.1.3.3). The 'DL Time Control' will adjust the timing to follow the highest of these power gains (peak search approach).

This tracking strategy implies that the 'Cell Search' does an initial chip level synchronization (acquisition) and the reported timing is within the fractional delay resolution requirements. If this is not the case or the offset changes by a value larger than the delay resolution requirements, the time difference between the 'chip fingers' shall be set at a value larger than the 'Pulse Shaping Delay Resolution' and gradually reduced (i.e. bisected). In this case, the current time change could be calculated using a 2nd order polynomial peak search on the 'M.P. Powers'.

3.1.2.4 Feedback Frequency Synchronization

The need of carrier synchronization at this point on the signal flow is mainly motivated by the need to reduce sinc-aliasing code-channel 'smearing' (which causes co-channel interference) and to improve the quality of the multi-path estimation. Implementation-wise this process could be implemented as a 'Digital Controlled Oscillator' and digital complex mixers for complex sine-wave multiplication of the received chips.

The main contribution to the carrier frequency offset are the 'Doppler Shift' (vehicular speed limited to 250 km/h) and instability of both Node B and User Equipment local oscillators (constrained by the conformance requirements) and could be shown that maximum carrier offset is around 20 kHz. Therefore the synchronization after pulse shaping causes an ignorable spectral distortion (compare $RRCoS\text{BW} = 3.84\text{MHz} \cdot 1.22$ with 20 kHz), but reduces the amount of processing.

Note that frequency synchronization shall be done for all chip fingers ('early', 'in-time' and 'late').

3.1.3 FDD Baseband Chip Processing

Figure 3-7 shows the signal flow within the 'Transmitter Baseband Sample Processing' where the process flow could be described as follows:

- The 'Physical Channels bits' are modulated by the 'Spreader and Modulator' into the transmitted 'chips'.

- The 'Spreader and Modulator' multiplexes the 'Pilot Bits' within DC PCH and uses the 'Ch Signatures' generated by the 'UL Pilots and Codes Signatures Generator'.

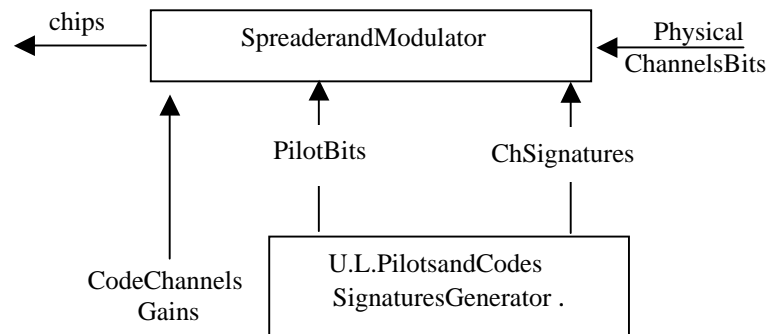


Figure 3-7: Transmitter Chip Processing, Signal Flow

The block diagram of Figure 3-8 shows the signal flow within the 'Receiver Baseband Chip Processing and Control'.

Process flow wise, the 'Receiver Chip Processing' could be summarized as follows:

- The 'Multipath Searcher' estimates the 'in-time' multipath channel complex weights (MP Weights) and uses the 'in-time', 'early' and 'late' power gains (MP Powers) to search the multipaths. The power gains will be fed back to the 'DL Time Controller' for time tracking.
- The 'RAKE Receiver' first combines the 'In-Time Sync Chips' with the 'MP Weights' and then descrambles and despreads the result using the 'Ch Signatures'. The RAKE Receiver will output the 'Code Channels Soft Symbols'. Under certain conditions an optional level of equalization could be considered within the rake receiver.
- The residual frequency offset is estimated using the 'Code Channels Soft Symbols'.
- The 'Forward Symbols Frequency Synchronizer' compensates the channels residual frequency.
- Finally, the 'Physical Channels Soft Bits' are obtained by bit mapping and diversity combining of the 'Channels Sync Symbols'.

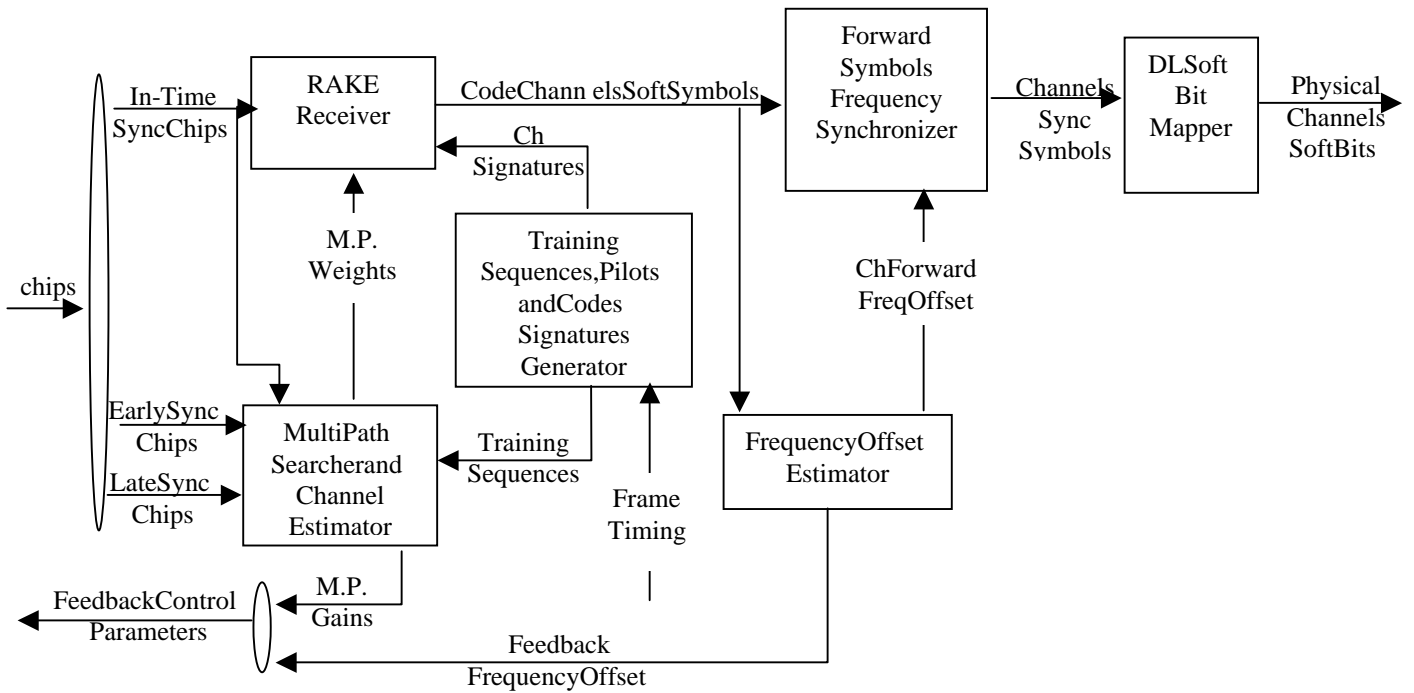


Figure 3-8: Receiver Chip Processing, Signal Flow

3.1.3.1 Transmitter Spreading and Modulation

Spreading is applied to the physical channels. It consists of two operations. The first is the channelisation operation, which transforms every data symbol into a number of chips, thus increasing the bandwidth of the signal. The number of chips per data symbol is called the Spreading Factor (SF). The second operation is the scrambling operation, where a scrambling code is applied to the spread signal.

With channelisation, data symbols on so-called I- and Q-branches are independently multiplied with an OVSF code. With the scrambling operation, the resultant signals on the I- and Q-branches are further multiplied by complex-valued scrambling code, where I and Q denote real and imaginary parts, respectively.

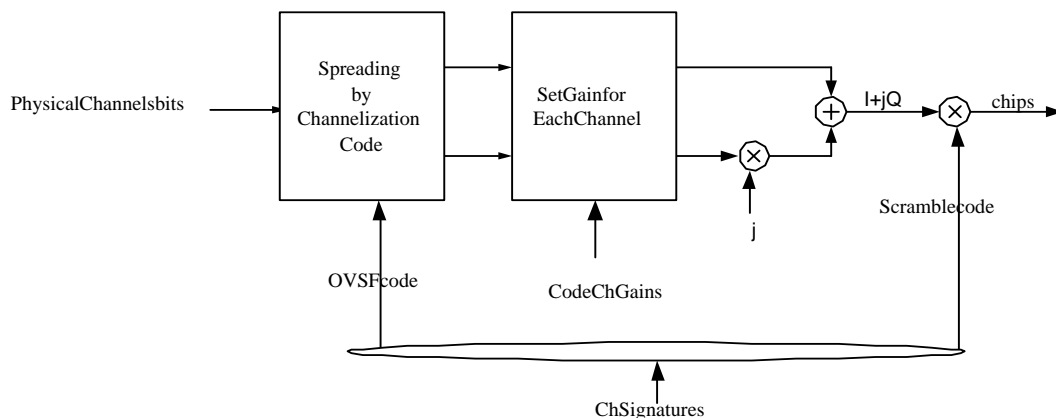


Figure 3-9: Spreading for uplink

3.1.3.1.1 DPCCH/DPDCH/HS-DPCCH

Figure 3-10 illustrates the principle of the uplink spreading of DPCCH, DPDCHs and HS-DPCCH. The binary DPCCH, DPDCHs and HS-DPCCH to be spread are represented by real-valued sequences,

i.e. the binary value "0" is mapped to the real value +1, the binary value "1" is mapped to the real value -1, and the value "DTX" (HS-DPCCH only) is mapped to the real value 0. The DPCCH is spread to the chip rate by the channelisation code c_c . The n :th DPDCH called DPDCH_{*n*} is spread to the chip rate by the channelisation code $c_{d,n}$. The HS-DPCCH is spread to the chip rate by the channelisation code c_{HS} . One DPCCH, up to six parallel DPDCHs, and one HS-DPCCH can be transmitted simultaneously, i.e. $1 \leq n \leq 6$.

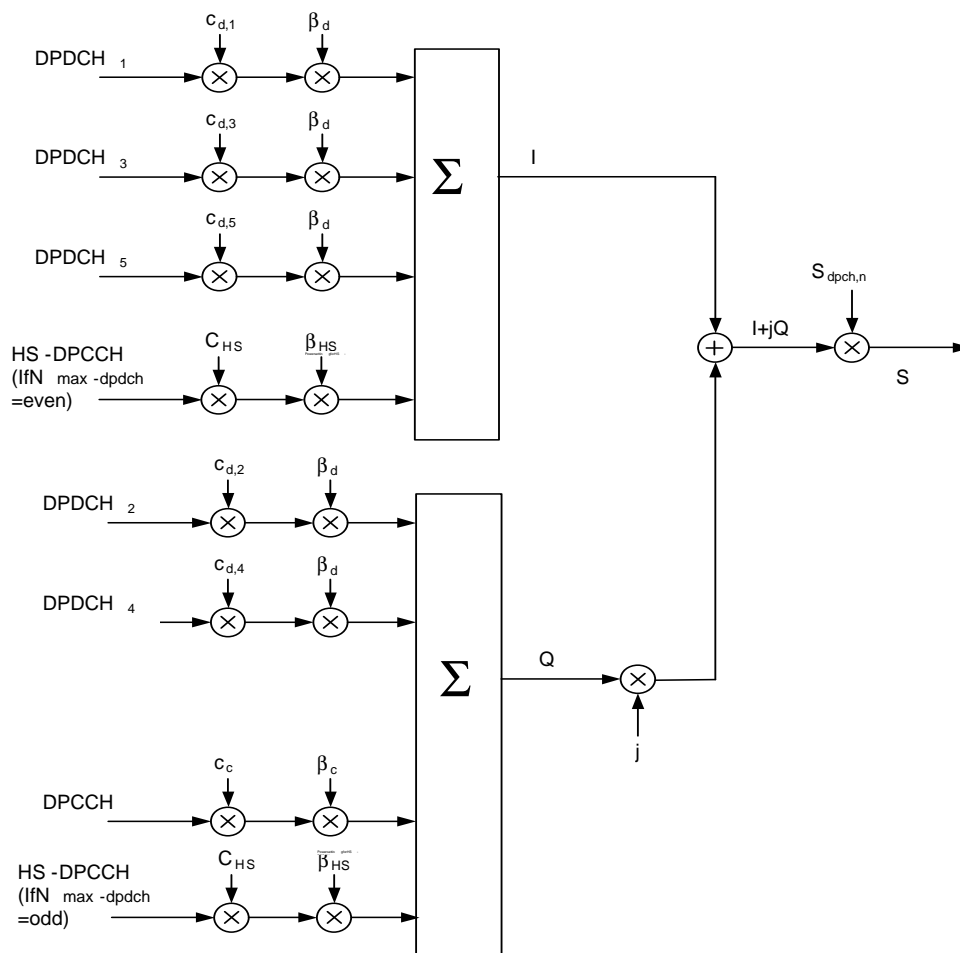


Figure 3-10: Spreading for uplink DPCCH, DPDCHs and HS-DPCCH

After channelisation, the real-valued spread signals are weighted by gain factors, β_c for DPCCH, β_d for all DPDCHs and β_{HS} for HS-DPCCH (if one is active).

After the weighting, the stream of real-valued chips on the I- and Q-branches are then summed and treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code $S_{dpch,n}$. The applied scrambling code is aligned with the radio frames, i.e. the first scrambling chip corresponds to the beginning of a radio frame. For more details, see the specification 3GPP TS 25.213 v5.1.0.

3.1.3.2 Modulation

See the specification 3GPP TS 25.213 v5.1.0.

3.1.3.3 Multipath Searching and Channel Estimation

Figure 3-11 shows the block diagram of a 'Multipath Searching' for a single downlink source.

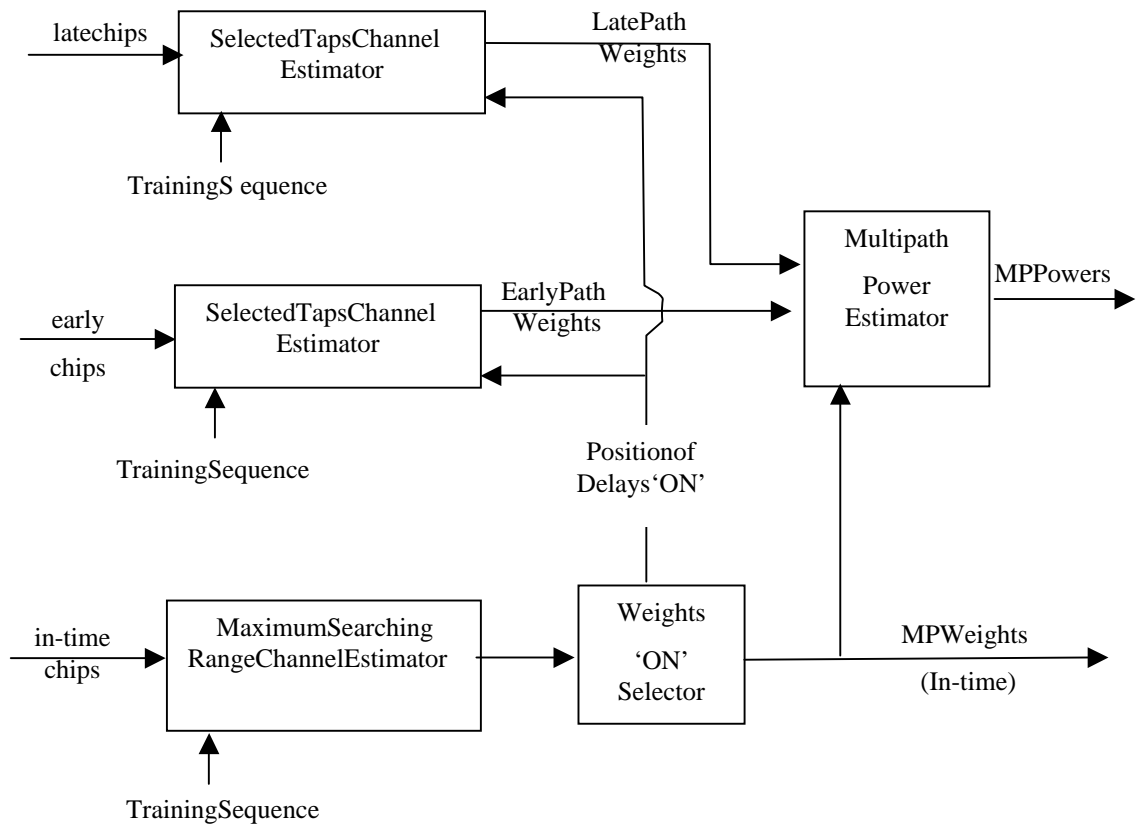


Figure 3-11: Multipath Searching

The multi-path channel is estimated for the 'in-time chips' for all delays over a maximum searching range and only the strongest paths are selected (by the 'Weights ON Selector'). Assuming an 'early-late' closed-loop time synchronization, the channel is again estimated only at the delays associated with the 'in-time' strongest paths (at 'Position of Delays ON').

The resulting power values (see Figure 3-12) are used as metrics by the 'DL Time Controller' for time tracking and the 'MPWeights' are used by the RAKE receiver to exploit the multipath diversity by 'Maximal Ratio' combining the 'in-time chips'.

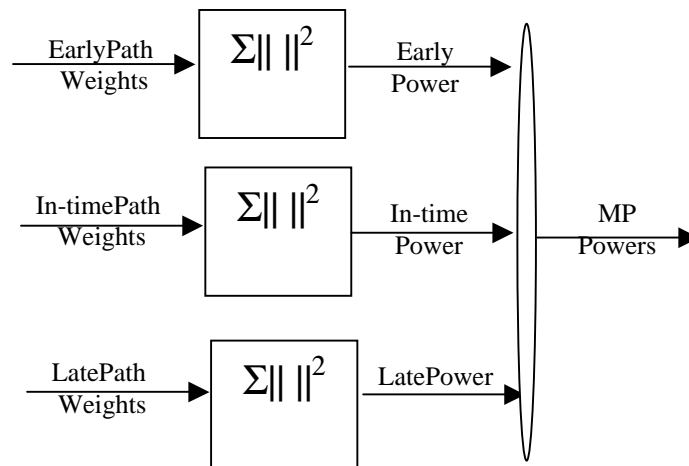


Figure 3-12: Multipath Power Estimator, Block Diagram

3.1.3.4 The RAKE Receiver

In the RAKE receiver a 'Maximal Ratio Combiner' (MRC) is used to combine the multipath signals to increase the SIR of the received signal. Figure 3-13 shows such an arrangement, where the linear 'Maximal Ratio Combiner' precedes the 'Descrambler and Despreader' block.

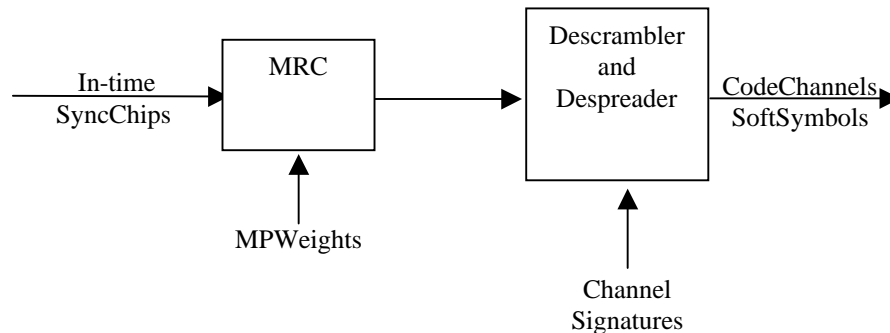
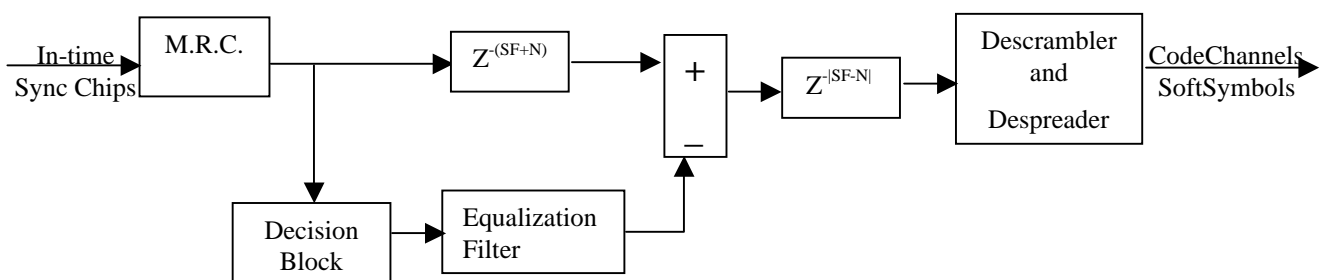


Figure 3-13: RAKE Receiver

For low spreading factors, because of the low processing gain, the amount of inter-path and inter-user interference could be considerable. Equalization and interference cancellation may be required. For example, if the 'MPWeights' convolution measured in respect to the 'In-time Gain' divided by the channel spreading factor is larger than a set threshold further equalization may be needed. If equalization is performed, a 'Pre and Post' cancellation method should be preferred over other methods such as 'Zero-Forcing' (because of the spectral nulls presence in a mobile environment).

Figure 3-14 shows an example of an MRC and chip level 'Pre and Post' decision based equalization where:

- The 'Decision Block' attempts to estimate the transmitted chips. Note that only the channel of interest could be monitored.
- 'Equalization Filter' is an odd-symmetric FIR with the coefficients given by the circular convolution of the 'MPWeights' normalized to the weights power gain (In-time Gain), but with the central coefficient (tap) set to 'zero'.
- SF: the maximum spreading factor
- N: the MRC delay



- $|SF-N|$: the absolute value of $(SF-N)$

Figure 3-14: Example of RAKE MRC and Chip Level 'Pre and Post' Decision Based Equalisation

Note that the above example performs equalization at the chip level, but could be reduced to a symbol level equalization.

3.1.3.5 Forward Symbols Frequency Synchronization

As opposed to the 'Feedback Frequency Synchronization', this block operates in forward mode and its scope is to compensate for the 'residual' carrier offset left after feedback synchronization at channel symbol level. This will tend to reduce the symbol shifting and could be thought

of as a

'refinement' of the carrier recovery. Implementation wise this process could embed a 'Digital Controlled Oscillator' and digital complex mixers for complex sine wave multiplication of the 'Code Channels Soft Symbols'.

3.1.3.6 DL Soft Bit Mapping

This process maps the received complex channel symbols to the 'Physical Channel Soft Bits'. The recommended method for QPSK constellation is the projection of channel symbols into the 'decision' boundary. For higher order modulation, reliability of each bit can be computed by averaging reliability of all the constellation symbols that have the same value for that bit.

3.1.3.7 Frequency Offset Estimation

Various methods for frequency estimation are described and compared in [Agapciuc 2002], [Hanzo 2000] and [Meyer 1998]. If a data-aided mode is chosen for frequency estimation, only the pilot symbols should be considered at the input of the 'Frequency Offset Estimator'. A method that works for both data-aided and not data-aided is the phase multiplication method, which could be combined with a 'Fitz' estimator (referred in [Meyer 1998] as D-Spaced estimator) to give the best results (see [Agapciuc 2002]). For this method all the M-PSK modulated symbols could be used (mean that 'Type 3' 16-QAM HSDPA symbols should be excluded) where the phase multiplication factor equals 'M'. The 'Feedback Frequency Offset' output is the angular frequency offset normalized to the chip rate, where the 'Ch Forward Freq Offset' is the angular frequency offset normalized to each code channel symbol rate.

3.1.3.8 Code Generation

For FFDDL (receiver) the 'Code Generation' produces the:

- FDDL Scrambling and OVSF codes
- Training sequences for 'Multipath Searching and Channel Estimation' (i.e., P-CPICH, DCH pilot chips)

For FFDUL (transmitter) the 'Code Generation' produces the:

- FFDUL Scrambling and OVSF codes
- FFDUL CPCH pilot bits

Note that same OVSF code generation could be used for both UL and DL.

3.1.4 Transmitter Transport Channel Processing

Figure 3-15 shows the processing chain of the transmitter 'Transport Channel Processing', where the 'UL Data' bits are coded, interleaved and rate matched.

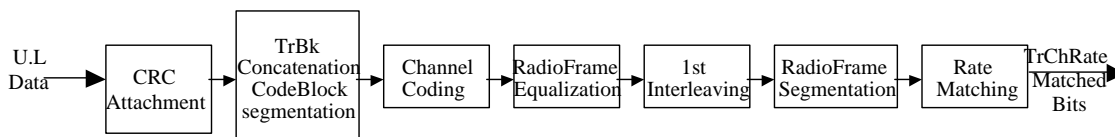


Figure 3-15: Transmitter Transport Channel Processing, Block Diagram

3.1.4.1 CRC Attachment

The CRC bit will be appended to each transport block. CRC size, which varies from 24, 16, 12, 8 to 0 will be determined by higher layer control.

3.1.4.2 Transport block concatenation/segmentation and channel coding

All transport blocks in a Transport Time Interval (TTI) are serially concatenated. If the concatenated string size is larger than the maximum allowable size for the code block, then code block segmentation will be performed. The allowable block size for turbo coding is $40 \leq X \leq 5114$ and $X \leq$

504 for convolution coding. All segmented blocks must be of the same size. If this is not possible, then filler bits will be added to the start of the 1st block. After channel coding, if there are more than 1 encoded block (i.e., more than 1 segmentation block), they will be serially concatenated.

3.1.4.3 Radio frame size equalisation and 1st interleaving

The radio frame size equalisation appends the input data with {0, 1} so that the output stream can be segmented into the same size frame for rate matching. Bits are split into column/s in the 1st interleaver depending on the TTI length. In compress mode by puncturing, radio frames are marked in positions corresponding to the starting bits of the radio frames. Bits are read into a matrix in rows, column-wise interleaving is done through permutation patterns depending on the TTI length. The outputs are read out in columns.

3.1.4.4 Radio frame segmentation and Rate matching

If the TTI is longer than 10ms, the input sequence will be segmented and mapped onto consecutive radio frames. The rate matching block repeats or punctures bits on a transport channel so that the channel bitrate can be met after the TrCH multiplexing. Bit separation is done only on turbo encoded TrCH in puncturing case. For the case of turbo encoded TrCH with repetition and convolutionally encoded TrCH, bit separation function is transparent. The decision of bit puncturing and repetition is controlled by higher level signaling and is done at the rate matching algorithm block. Puncturing bits will be removed at bit collection.

3.1.5 Transmitter Physical Channel Processing

Figure 3-16 shows the processing chain of the transmitter 'Physical Channel Processing', where the 'TrCh Rate Matched Bits' are multiplexed, interleaved and mapped to the 'Physical Channel Bits'.

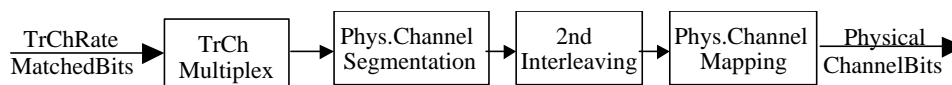


Figure 3-16: Transmitter Physical Channel Processing, Block Diagram

In TrCH multiplexing, each 10ms radio frame from individual TrCH will be serially multiplexed into a coded composite transport channel (CCTrCH). The CCTrCH are then being divided into different PhCHs during PhCH segmentation, when more than one PhCH are used. Bits that are marked before the 1st interleaver, will be removed. At the 2nd interleaver, input is read into a 30 column matrix in rowwise. Block interleaving is done here through an inter-column permutation pattern. Output is read out columnwise. During physical channel mapping, input is mapped onto the physical channel. In the uplink, each transmission frame is either completely filled or not used at all, except for compress mode where retransmission is turned off during TGL. However, there is no such restriction in the downlink.

3.1.6 Receiver Physical Channel Processing

Figure 3-17 shows the processing chain of the receiver 'Physical Channel Processing', where:

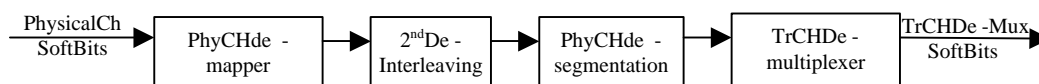


Figure 3-17 Receiver Physical Channel Processing, Block Diagram

- The demapped PhCH is input into the 2nd deinterleaving block where the inversion of the 2nd interleaver will be done using the same permutation pattern as that in the transmitter.
- With more than 1 PhCH, each PhCH will be combined to form one CCTrCH in the PhCH de-segmentation block.

- The TrCH will be demultiplexed from the coded composite transport channel (CCTrCH) in the TrCH demultiplexing block accordingly into respective 10ms radio frames.

3.1.7 Receiver Transport Channel Processing

Figure 3-18 shows the processing chain of the receiver 'Transport Channel Processing', where:

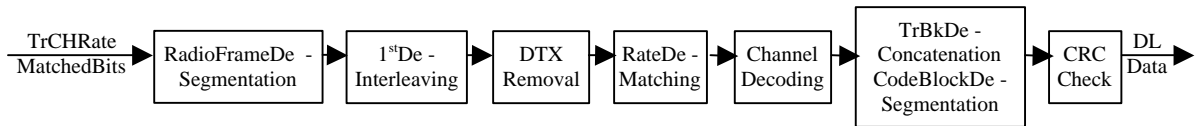


Figure 3-18 Receiver Transport Channel Processing, Block Diagram

- The radio frame is reconstructed from thesegmentation done in the transmission to fit the 1 deinterleaver block size.
- An inversion of the 1st interleaving is done using a same permutation pattern.
- 1st DTX Removal is required for fixed positions of TrCHs.
- When puncturing is done in the Node B transmitter, bits insertion will be done here. In the case of soft bits, bits with neutral weightage will be inserted. For bit repetition, the repeated bit will be removed.
- The decoding for the convolutional code will most likely be done through Viterbi decoding and turbo code will most likely be processed with iterative decoder. After channel decoding, the transport block will be reconstructed for CRC check.
- The CRC bits are rechecked and will be detached from each transport block. If error occurs in the CRC check, retransmission will be necessary. As with the transmitter, CRC size will be informed through higher layer control.

3.2 Baseband Architecture for UMTS/TDD

A general description for the link level UL/DL of UMTS/TDD will be presented here, and the functionality of the constituent blocks will be described. This section should give a clear understanding of the receiver algorithms in the UMTS/TDD mode.

3.2.1 Transmitter

A first order subdivision of the transmitter module is shown in Figure 3-19. Many modules of the transmitter are identical to those used by UMTS/FDD mode (channel coding, spreading, etc.), and have not been described in this section to avoid multiple descriptions.

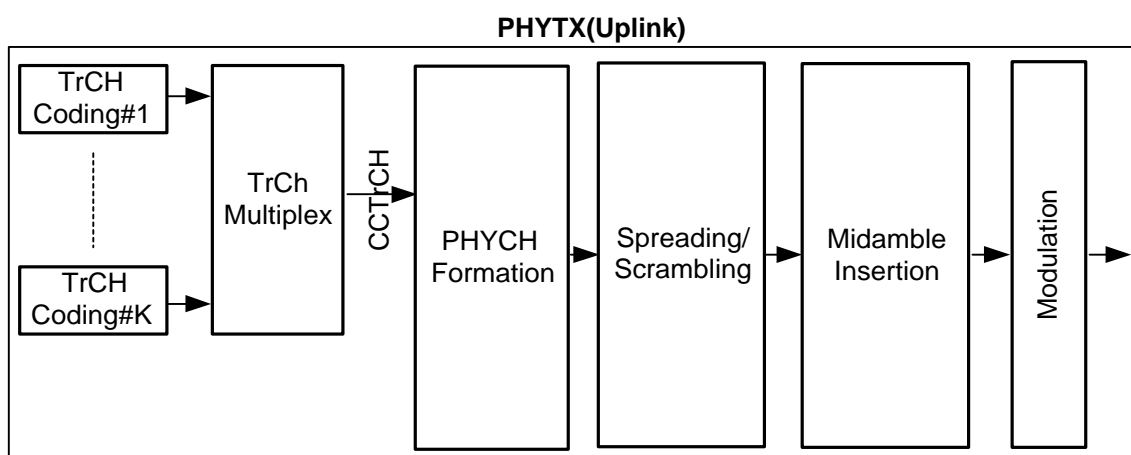


Figure 3-19: Block Diagram of the Transmitter.

3.2.1.1 TrCH Coding

Functionalities: this block receives the binary sequence generated by the data source, and performs processing to make the transmitted sequence more resistant against channel impairments. The processing operations performed within this block are:

Channel coding

Interleaving

Data block length/size management operations. These operations are intended to rearrange the data so that the blocks internally processed follow 3GPP specifications, and enable matching of the input sequence data rates with one of those specified for UMTS. A more detailed block diagram of this unit is given in Figure 3-20.

3.2.1.2 TrCH Multiplex

Functionalities: the function of this block is to multiplex data from several TrCH's.

3.2.1.3 PhyCh Formation

Functionalities: this block creates the physical channels according to 3GPP specifications. The operations included within this block are:

- Data block management, specifically , segmentation of the input data into blocks with the appropriate size.
- Second level of interleaving.

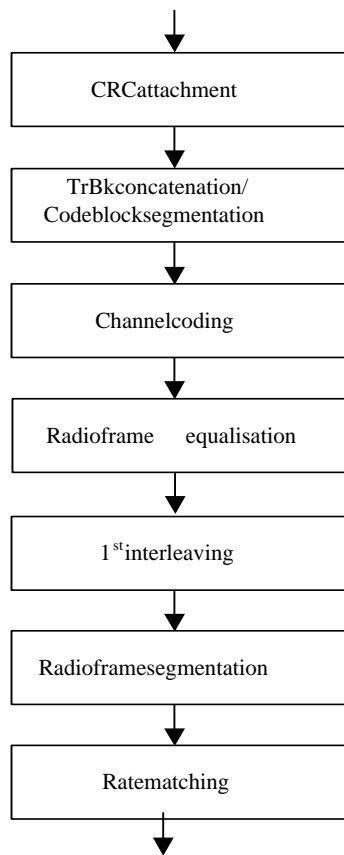


Figure 3-20:BlockDiag ramofTrCHModule.

3.2.1.4 Spreading/Scrambling

*Functionalities:*theoperationsperformedwithinthisblockare:

- MultiplicationofthecomplexalgebraicsequencesfromthePhyChFormationblockwitha Walsh-Hadamardcodeoflength Q ($Q \in 1 \dots 16$)and baudrate3.84Mchip/s.Thisoperation providesaspreadingfactorof Q .
- Multiplicationofspreadsequencesbyarandomisationcodeatthesamebaudrate.The randomisationcodesaredefinedin[3GPP25223320].

Theblockdiagramillustratingthesetwooperationsisshownin Figure 3-21.

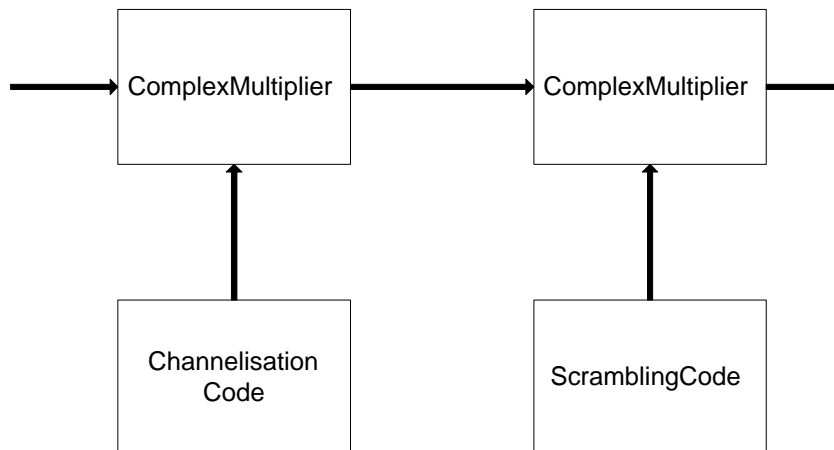


Figure 3-21:BlockDivisionofSpreading/ScramblingUnit.

3.2.1.5 Midamble Insertion

Functionalities: this block multiplexes the sequence from the spreading/scrambling unit, with a deterministic sequence known as midamble specified by 3GPP [RAN25.221]. Two different types of midambles have been defined, one with 512 chips of type 1 and another with 256 chips of type 2. Figure 3-22 and Figure 3-23 show how they are inserted in bursts 1 and 2. They are used to estimate multiple channel impulse response in the UL. In the DL, when no Tx diversity scheme is used, there is only one midamble common to all the bursts of the slot.

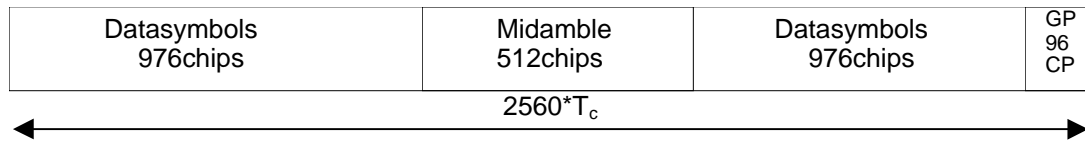


Figure 3-22: Structure of Burst Type 1.

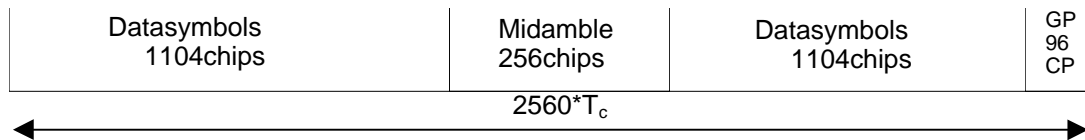


Figure 3-23: Structure of Burst Type 2.

3.2.1.6 Modulation

Functionalities: the purpose of this block is to adequately shape the signal to be transmitted over the channel. 3GPP specifies QPSK carrier modulation with root-raised cosine pulse formatting (roll-off factor = 0.22). Since 3GPP specifies coherent demodulation, the simulations are carried using the baseband complex envelopes of the real bandpass signals. Consequently no block involving specific QPSK carrier modulation is needed. The Modulation block has only to provide the RRC shape to the 4-ary unitary amplitude complex samples provided by the block Midamble Insertion block.

3.2.2 Receiver

Figure 3-24 shows the block diagram of the receiver. The sub-modules that compose the receiver are the following:

- **Pulse shaping:** square root raised cosine filter identical to the one used by FDD mode.
- **Channel estimation:** each user's channel impulse response $h_k = (h_k[0], \dots, h_k[W-1])$ is estimated with the a priori knowledge of the transmitted midamble. The algorithm exploits the midamble construction method and is therefore specific to the TDD mode.
- **Rake receiver:** depending on the channel estimation strategy, the Rake receiver for the TDD mode can have the same structure as the one used for FDD. If the channel estimation algorithm estimates the tap-delay line multipath model, the Rake receiver has the same structure as for FDD. On the other hand, if the channel estimation algorithm estimates a $T_c/2$ received channel, the rake receiver will have a FIR structure. As an option, Multi-user detection algorithm can replace or be added after the Rake receiver. A classical MUD receiver is the joint detection, which is a block multi-user equalizer.
- **RxPhyCh:** This block performs the inverse of the operations done by the block PhyCh Formation, i.e. deinterleaving and unsegmentation.
- **TrCH demultiplexing:** This block is the dual of the TrCH coding block. It performs channel decoding, deinterleaving and block management operations.
- **TrCH decoding:** This block is the dual of the TrCH coding block. It performs channel decoding, deinterleaving and block management operations.

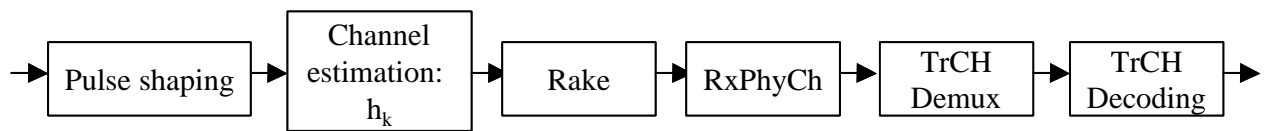


Figure 3-24: Module identification of Rx

3.2.2.1 Channel estimation

Let e be the vector corresponding to the useful part of the received midamble, and h the vector of concatenated channel impulse response of the K user:

$$h = (h_0[0], h_0[1], \dots, h_0[W-1], h_1[0], h_1[1], \dots, h_1[W-1], h_2[0], \dots, h_{K-1}[W-1])$$

The 2 vectors are linked with the midamble matrix G , according to the following linear system:

$$e = Gh + n$$

The matrix G is formed with the cyclic shift of length P sequences $s[0], \dots, s[P-1]$:

$$G = \begin{pmatrix} s[P-1] & s[P-2] & s[P-3] & \dots & \dots & s[1] & s[0] \\ s[0] & s[P-1] & & & & & s[1] \\ s[1] & s[0] & s[P-1] & & & & s[2] \\ \dots & & & \dots & & & \dots \\ \dots & & & & \dots & & \dots \\ s[P-3] & & & & & s[P-1] & s[P-2] \\ s[P-2] & s[P-3] & \dots & \dots & \dots & s[0] & s[P-1] \end{pmatrix}$$

To perform low cost channel estimation, we used the eigenvalue decomposition of properties of circulant matrix: the eigenvector of G are the column of the FFT matrix W .

$$G = W^{-1} \Lambda W$$

$$G^{-1} = W^{-1} \Lambda^{-1} W$$

$$\hat{h} = W^{-1} \Lambda^{-1} W e$$

Λ is the diagonal matrix containing the eigenvalues of G , and is computed according to the following formula:

$$\Lambda = Q g_0 = \text{diag}(DFT(g_0))$$

where g_0 is the first column of G .

3.3 Baseband Architecture for HSDPA/FDD

A general description of the link level for HSDPA/FDD will be presented here, and functionality of the constituent blocks will be described.

High-speed downlink packet access has been added to the 3GPP UMTS standards in order to increase the data throughput, reduce the delay and to achieve high peak data rates. Therefore techniques such as adaptive modulation and coding (AMC), hybrid ARQ and fast scheduling have been added to the standards.

This chapter will focus on the high-speed downlink packet access (HSDPA) enhancements of the UMTS/FDD mode. Therefore only HSDPA specific additions will be described, in order to avoid overlapping with Chapter 3.1

3.3.1 HSDPA Specific Uplink Channel Coding and Modulation

HSDPA does not use a divergent channel coding compared to UMTS. The differences are only:

- CQI (Channel Quality Indicator)
- ACK-NACK (HARQ Protocol)
- Additional timing values
- Additional 16-QAM modulation

3.3.1.1 CQI - Channel Quality Indicator Definition

The CQI specification can be found in 3GPP TS 25.214 in chapter 7.1.2 and 7.2.

The UE procedure for reporting channel quality indication (CQI) is defined in the following steps:

- 1) The UE derives the CQI value as defined in 3GPP TS 25.214 chapter 7.2.
- 2) The UE shall transmit the CQI value in each subframe that starts $n \times 256$ chips after the start of slot i on the associated uplink DPCH with i simultaneously fulfilling

$$(5 \times CFN + \lceil (n \times 256 \text{ chip} + i \times 2560 \text{ chip}) / 7680 \text{ chip} \rceil) \bmod k = 0 \quad \text{and} \quad i \bmod 3 = 0,$$
 where CFN denotes the connection frame number for the associated DPCH and being the smallest m fulfilling the requirement described in subclause 7.7 in 3GPP 25.211.
- 3) The UE shall repeat the transmission of the CQI value derived in 1) over the next $(N_{\text{cqi_transmit}} - 1)$ consecutive HS-DPCCH subframes in the slots respectively allocated to the CQI as defined in 3GPP 25.211.
- 4) The UE shall not transmit the CQI in other subframes than those described in 2) and 3).

The UE shall report the highest tabulated CQI values such that, for the current radio conditions, the transport block error probability does not exceed 0.1 for a single transmission with a TFRC corresponding to the reported, or a lower, CQI value. Depending on the UE category as defined in 3GPP 25.306, either Table 8, 9, 10, or 11 should be used. For the purpose of CQI reporting, the UE shall assume a total received HS-PDSCH power of $P_{\text{HSPDSCH}} = P_{\text{CPICH}} + \Gamma + \Delta$ in dB, where the measurement power offset Γ is signaled by higher layers and the reference power adjustment Δ is given by Table 8, 9, 10, or 11, depending on the UE category. If S-CPICH is used as a phase reference for HS-PDSCH demodulation, P_{CPICH} is the received power of the S-CPICH used by the UE, otherwise P_{CPICH} is the received power of the P-CPICH.

3.3.1.2 ACK-NACK (HARQ Protocol)

The HARQ specification can be found in 3GPP TS 25.214 in chapter 7.1.1.

If the UE did not detect control information intended for this UE on any of the HS-SCCHs in the HS-SCCH set in the previous subframe, the UE shall monitor all HS-SCCHs in the HS-SCCH set. If the UE did detect control information intended for this UE in the previous subframe, it is sufficient to only monitor the same HS-SCCH used in the previous subframe.

If a UE detects that one of the monitored HS-SCCHs carries control information intended for this UE, the UE shall start receiving the HS-PDSCHs indicated by this control information. After decoding the HS-PDSCH data, the UE shall transmit a hybrid ARQ ACK or NACK as determined by the MAC layer based on the CRC check. The UE shall repeat the transmission of the ACK/NACK information over $N_{\text{acknack_transmit}}$ consecutive HS-DPCCH subframes, in the slots allocated to the HARQ-ACK as defined in the following chapter. When $N_{\text{acknack_transmit}}$ is greater than one, the UE shall not attempt to receive nor decode transport blocks from the HS-PDSCH in HS-DSCH subframes $n + 1$ to $n + (N_{\text{acknack_transmit}} - 1)$ where n is the number of the last HS-DSCH subframe in which a

transport block has been received. If control information is not detected on any of the HS-SCCHs in the HS-SCCH set, neither ACK, nor NACK, shall be transmitted in the corresponding subframe.

Further information about the additional MAC_hsis is available in the 3GPP TS 25.321 Specification.

3.3.1.3 Additional timing values

These timing specifications can be found in 3GPP TS 25.211 in chapter 7.7.

Figure 3-25 shows the timing offset between the uplink DPCCCH, the HS-PDSCH and the HS-DPCCH at the UE. The code-multiplexed HS-DPCCH sub-frame starts $m \times 256$ chips after the start of an uplink DPCCCH slot with m selected such that the ACK/NACK transmission starts within the first 0-255 chips after 7.5 slots following the end of the received HS-PDSCH sub-frame. UE and Node B shall only update m in connection to UTRAN reconfiguration of downlink timing. Note that due to autonomous adjustments of the DPDCCH/DPCCH transmission time instant by the UE described in 3GPP 25.214, the relationships described in this section may cease to be valid. More information about the uplink timing adjustments can be found in 3GPP 25.214.

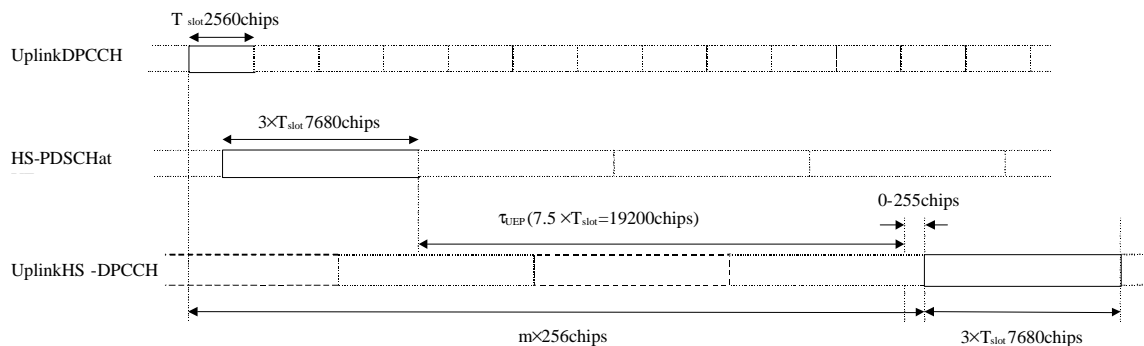


Figure 3-25: Timing structure at UE for HS-DPCCH control signalling

3.3.2 HSDPA Specific Downlink Channel Coding and Modulation

This Chapter describes the HSDPA specific in contrast to the basic UMTS algorithms. A few UMTS descriptions (e.g. Rake-MMSE) are included to describe possible improvement options for HSDPA.

In the downlink, several physical channels are multiplexed synchronously to the transmission channel by using orthogonal spreading codes. In a multipath channel, inter-path interferences destroy the orthogonality and cause multiple-access interferences (MAI). Along scrambling code of length 38400 chips is superimposed on the spreading codes in order to reduce the impact of the multi-paths and the MAI.

The part of the receiver described in this section basically has to perform five tasks. The first task consists of the timing synchronization with respect to the received scrambling code. As a second task, the frequency error of the local clock oscillator relative to the clock oscillator of the transmitter is estimated and corrected. The third task is to suppress the MAI of the multipath channel. A first option is a simple Rake combiner. The proposed more powerful second option is a MMSE chip-level equalizer. In the fourth step the data of the I and Q components are detected by means of despreading and descrambling. HSDPA data that are 16-QAM modulated in order to achieve highest data rates are reconstructed by a 16-QAM demapper in a fifth step.

Figure 3-26 gives an overview of this part of the receiver that is divided into synchronization, MAI suppression and demodulation. A more detailed description is given in the following subsections.

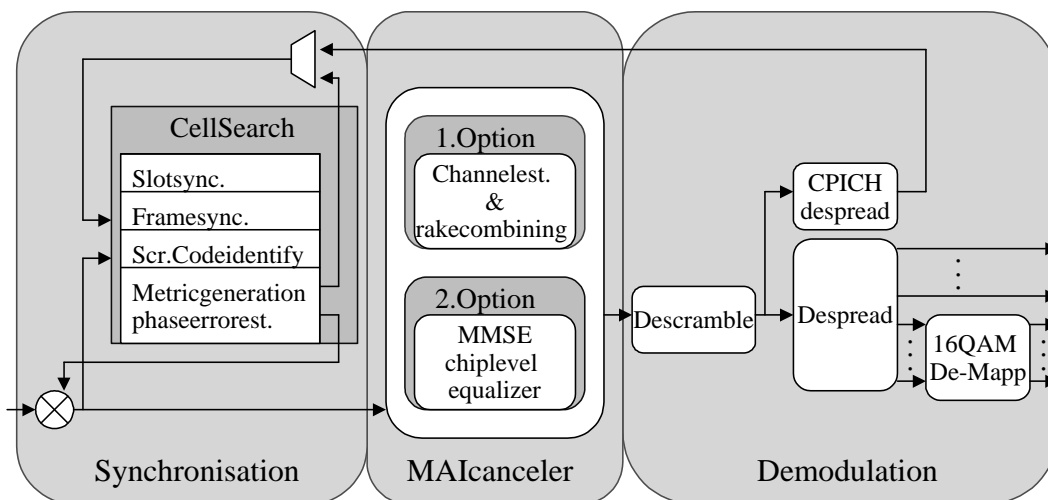


Figure 3-26: Synchronization and Demodulation

3.3.2.1 Synchronization

This part in HSDPA is identical to UMTS synchronization. Thus no additions have to be reported here.

3.3.2.2 MAI suppression

For 3GPP one important distinction from previous standards is the requirement of high and variable data rate. It is possible to increase the data rate without bandwidth expansion by reducing the spreading factor. Alternatively, the spreading factor may remain fixed and allocating several parallel spreading codes for the same service increases the data rate. The standard supports both techniques.

The physical layer has been defined in such a way that a conventional RAKE receiver, forming the simplest multi-path diversity receiver that can be used, would give sufficient performance in most cases.

Therefore, as a first option a rake combiner can be used. This receiver type suffers from multi-user interference caused by other channels. Thus, a rake combiner would require very powerful channel coding to guarantee sufficient low BERs. Advanced receiver algorithms capable of suppressing or cancelling interference can significantly improve system capacity with less channel coding needed. The target requirement of 10 Mbit/s could be fulfilled with a rake combiner by a large amount of puncturing. In order to be able to handle this challenging requirement in a more hostile environment, an MMSE chip level equalizer can replace the rake combiner in the more powerful option.

Rake combiner

The rake combiner contains a channel estimator that consists of two parts. The 4 strongest delays are determined by a full search with respect to the CPICH. Those paths out of the four strongest ones that exceed a certain threshold (20% of the power in the strongest path) are tracked in separate fingers in the second part. The tracking in a distinct finger is performed using an early-late loop with a timing resolution of 8 samples per chip. Each finger is able to estimate Doppler shifts of up to 800 Hz. A fast estimation and correction of the phase errors caused by the Doppler shifts allow correlating over 4 bits on the CPICH corresponding to 1024 chips. The estimates of the respective coefficients of the channel impulse response, build from the active fingers, are maximum ratio combined.

MMSE chip level equalizer

The purpose of the MMSE equalizer is to approximate the superposed multi-user synchronous signal at the output of the downlink transmitter by means of a linear operation. The approximation is done by minimizing the mean square error between the multi-user synchronous signal and the estimate at the output of the equalizer. This minimization problem can be formulated as follows:

$$\min E\{|s(n + \tau) - g^H \cdot r|^2\},$$

where $s(n + \tau)$ denotes the transmitted and time shifted multi-user chip-sequence, g^H the transposed and complex conjugated version of a vector containing the taps of the equalizer and a vector of consecutive received data. The length of r corresponds to the length of the equalizer.

Under the following statistical assumptions:

- these sequence values for the multi-user signal are i.i.d. random variables of variance σ_s with uncorrelated constellation points in order to avoid that the covariance matrix of s becomes a complicated expression involving the OVSF codes
- $r = H \cdot s + \eta$, where H is the channel convolution matrix and the additive noise η is an i.i.d. complex random variable with zero mean and variance σ_N
- s and η belong to uncorrelated processes

The minimization problem is solved by :

$$g = (HH^H + \sigma_N^2 / \sigma_s^2 \cdot I)^{-1} H \cdot e_\tau.$$

Those set of coefficients g out of the possible solutions, given by this equation, belonging to a delay τ that lead to the minimum mean square error have to be chosen for the taps of the chip level equalizer.

Several efficient algorithms for solving the given equations system exist that exploit the pilots on the CPICH in order to adaptively update the equalizer coefficients at the symbol rate instead of the chip rate. For these algorithms no knowledge is required about the active channel codes as well as the transmitted symbols. In addition to that the variances of signal and noise must not explicitly be determined.

3.3.2.3 Demodulation

After the scrambling, the soft bits in the I- and Q-branches of up to 15 HS-PDSCH and one or more DPCH can be demodulated configuring a spreader building block accordingly. For QPSK modulated data the soft bits are fed directly to the channel decoder part. For HS-DPSCH data that is 16-QAM modulated the soft bits at first have to be demapped.

3.3.3 Physical Channel Decoding

Figure 3-27 shows the Physical channel decoding chain for UMTS (DCH)/HSDPA (HS-DSCH). Both of these chains exist in parallel and their channel decoding is conceptually similar with notable differences being the use of 16-QAM along with QPSK and shorter frame size. Therefore the HSDPA consists of the same functional blocks as UMTS (in fact most of them could be reused), and the only noticeable differences being the HARQ (replacing the Rate Matching in UMTS), an adaptive symbol to bit mapper and a retransmitted frame combiner. The chains are described below.

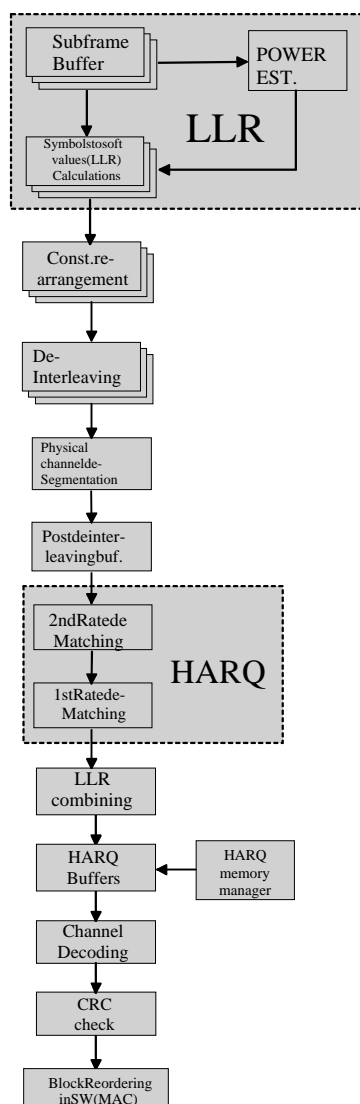


Figure 3-27: Channel Decoding chain HSDPA/HS -DSCH

3.3.3.1 HSDPA (HS -DSCH)

The HS-DSCH consists of the following blocks

- Subframe buffer (16 -QAM only)**
 This buffer stores the part of the subframe of HS -DSCH. The buffering is needed in order to perform the power estimation for the 16 -QAM LLR calculations. The size of the buffer depends on the reliability of estimates.
- Power Estimation (16 -QAM only)**
 Used to find the decision values to be used in 16 -QAM LLR calculations. In a way it provides the bias for mapping from symbol to bits.
- LLR Calculations**
 Symbols are mapped to bits based on the outputs from the power estimation block.
- Constellation Rearrangement**
 Specification reference: TS25.212 subclause 4.5.7.
 It changes the mapping from bits to constellation points to achieve better performance during retransmissions.
- DeInterleaving**

Specification reference 25.212 subclause 4.5.6.

For QPSK the interleaving is performed in the same way as in Rel99. For 16 Interleavers are reused.

-QAM2

- **Physical channel DeSegmentation**

Specification Reference: 25.212 Subclause 4.5.5

The bits from physical channels are put together (concatenated) to form a single HS block.

-DSCH

- **Post DeInterleaving Buffer**

The necessity of this buffer depends on the constraints in doing inverse HARQ. It is needed for the bit separation.

- **Bit Separation**

Specification reference 25.212 Subclause 4.5.5. The incoming bit stream is divided into three streams, the systematic bits, the first parity and the second parity. It's the inverse of the transmitter Bit Collection function.

- **2nd Rate Dematching**

Specification reference 25.212 Subclause 4.5.4.3.

The Second Rate dematching matches the incoming bit stream to receiver's soft buffering capacity. The Second Rate Matching also makes different redundancy versions for Incremental redundancy.

- **LLR combining**

Specification reference: NA.

The LLR combining combines different (re)transmissions of HS DSCH blocks to form one soft bit value for use in turbo decoder. For the first transmission the HARQ buffer needs to be nulled out or made transparent.

- **HARQ buffers**

Specification reference: NA.

HARQ buffers are divided into a set of 8 sub-buffers (to be investigated) one for each HARQ process that is active. The actual size of these buffers is signaled by higher layers.

- **1st Rate De-matching**

Specification reference 25.212 Subclause 4.5.4.2

Works in the same way as the Rate Matching in Rel99 with $\Delta N_{il}^{TTI} = N_{IR} - N^{TTI}$ where N_{IR} is the UE's soft buffering capacity. This block basically rearranges the soft bits into their respective correct positions before sending.

- **Channel Decoder**

Specification reference 25.212 Subclause 4.5.3

This block consists of the code block segmentation and Turbo decoder. A HS DSCH block can contain up to 4 code blocks each of (5114+tail) bits, which are separately decoded by the turbo decoder.

- **CRC decoder**

Specification reference 25.212 Subclause 4.5.1

24 bit CRC is performed to check the integrity of the received HS DSCH block. It's the same block as used in Rel99.

3.3.3.2 HS-SCCH Decoding

The HS-SCCH carries the control signaling for the HS-DSCH and has to be decoded before the HS-DSCH can be decoded. The HS-SCCH carries the following information

- The channelization code set $X_{CCS,1}, X_{CCS,2}, \dots$ (7 bits)

- ModulationschemeInformation X_{ms} (1bit)
- HybridARQprocessinformation(3bits)
- Redundancyandconstellationversion(3bits)
- Newdataindicator(1bit)
- UEidentity(16bits).TheUEid isnotexplicitlytransmittedonHS-SCCH, butitsusedinthe calculationofNE-specificmaskandCRC.

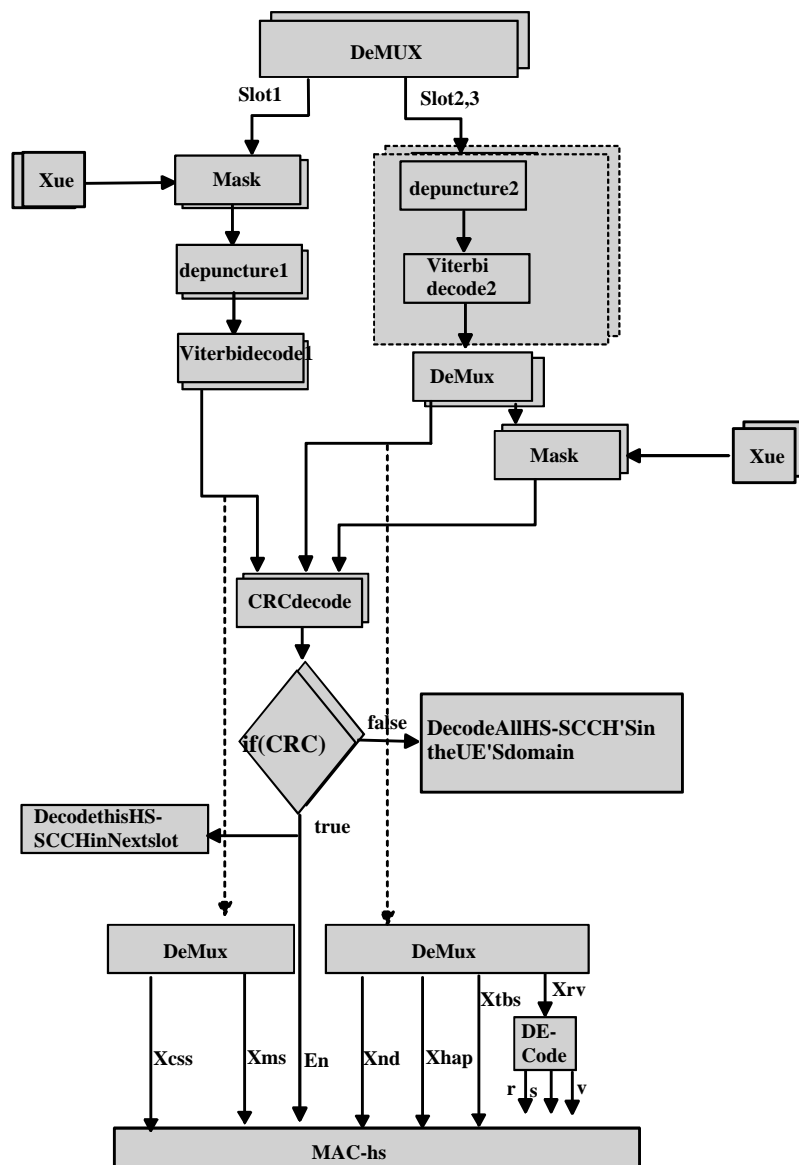


Figure 3-28:HS-SCCHDecoding

The decoding process involves the steps as explained in TS 25.211 chapter 4.6.4...4.6.7. The timing specification can be found in 3GPP TS 25.211 chapter 7.7.

3.3.3.3 HS-SCCH/HS-PDSCH timing

Figure 3-29 shows the relative timing between the HS-SCCH and the associated HS-PDSCH for one HS-DSCH sub-frame. The HS-PDSCH starts $\tau_{HS-PDSCH} = 2 \times T_{slot} = 5120$ chips after the start of the HS-SCCH.

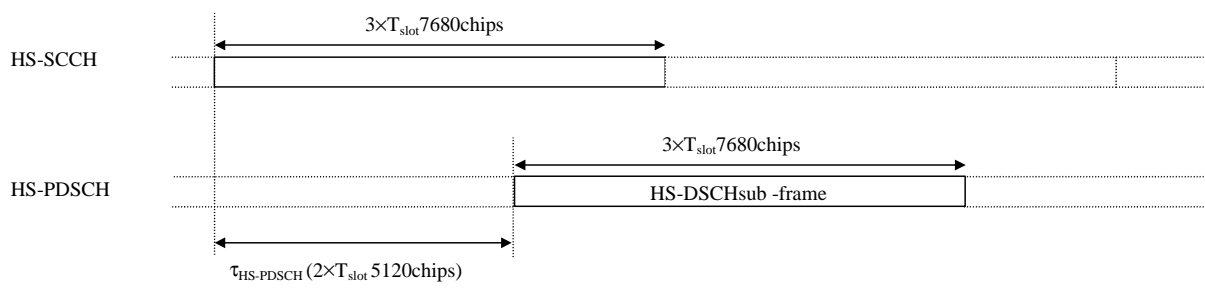


Figure 3-29: Timing relation between the HS -SCCH and the associated HS -PDSCH

4 Multi-Mode System Architecture

A general high-level description of the multi-mode system architecture will be presented here. It will be in a form of a matrix-like block diagram, with rows representative of different modes, and columns containing a functional group across modes. A matrix-like block diagram is provided for each sublayer in the Uplink Tx and Downlink Rx. Possible re-configurability in each column will be discussed in the aspect of whether the constituting functions are identical or they need further inspection for identifying their re-configurability level (SW re-configurable, HW re-configurable, and non-re-configurable).

4.1 Functionality Matrix for Uplink Transmitter

4.1.1 Sample Processing

The functional blocks of the 'Uplink Transmitter - Sample Processing' are virtually functional identical for all modes.

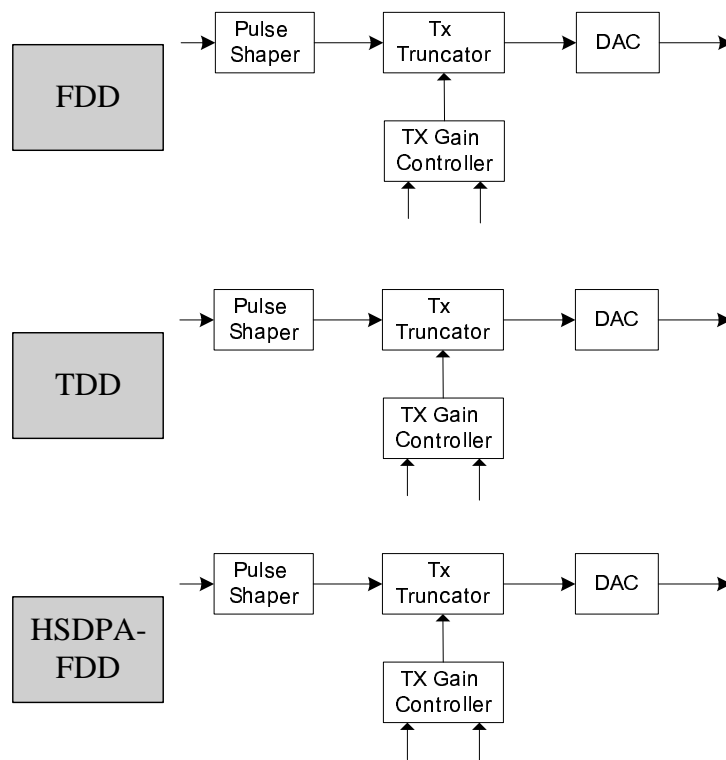


Figure 4-1: Block Matrix Uplink Transmitter - Sample Processing

4.1.2 Chip Processing

The transmitter 'Chip Processing' top level descriptions shown in Figure 4-2 is similar for both FDD and TDD. Only one block, the 'Midamble Insertion' is unique to TDD.

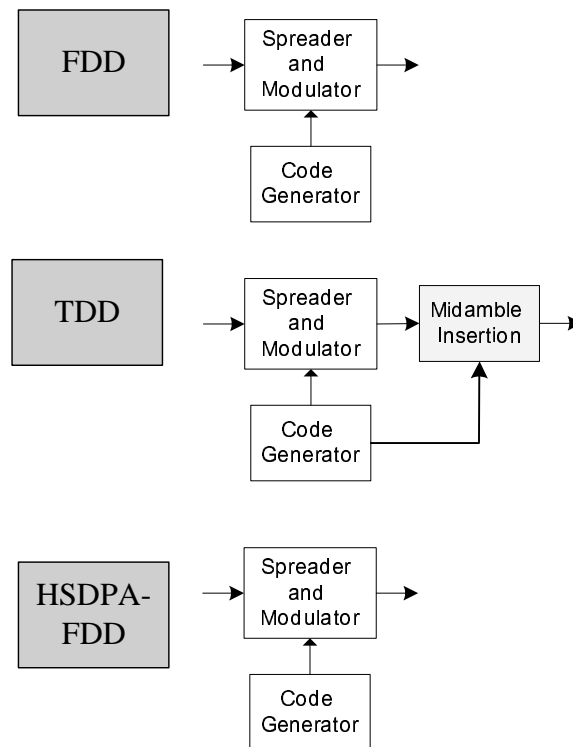


Figure 4-2: Block Matrix Uplink Transmitter – Chip Processing

Another difference between the FDD and TDD mode is the generation of scrambling code and the midamble for TDD as opposed to DCPCH pilot bits for FDD.

4.1.3 Transport Channel Processing

The functionality matrix for the uplink transmitter, which provides the transport channel processing, is shown in Figure 4-3. Most blocks for FDD and TDD are very similar if not equal. The channel coding, Transport Block Concatenation/Code Block segmentation and the CRC generation are the same for both modes. TDD has an additional option of no channel coding, which results in a larger parameter set for TrBI Concatenation /Code Block segmentation. HSDPA needs only simple channel coding in uplink. The following coding chain from Radio frame equalization has some differences between FDD and TDD. Especially Rate matching, which has to be further examined in respect to configurability.

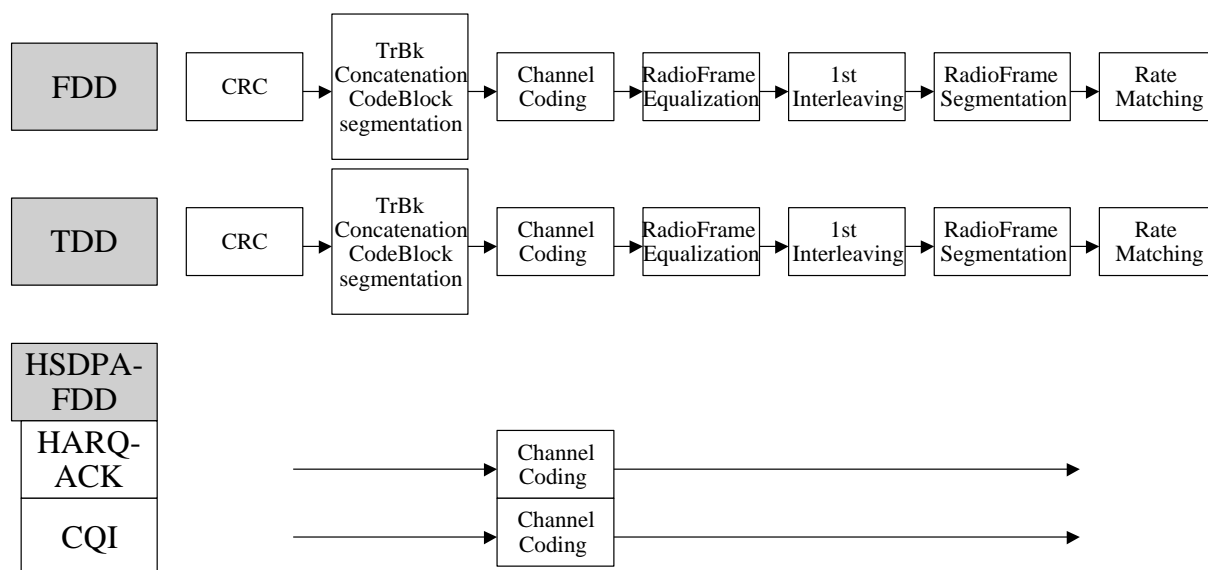


Figure 4-3: Block Matrix Uplink Transmitter –Transport Channel Processing

4.1.4 Physical Channel Processing

The functionalities shown in Figure 4-4 are also quite similar between FDD and TDD. One of the blocks, which is the Bits scrambling, is unique to TDD and will therefore not be reusable. Transport channel Multiplexer and Physical Channel Segmentation are more or less the same for FDD and TDD. The TDD 2nd interleaver is more complex, as it has two options, frame and time slot based, for interleaving. The interleaver itself is the same as in the FDD mode. Physical channel mapping has to be further inspected for its re-configurability.

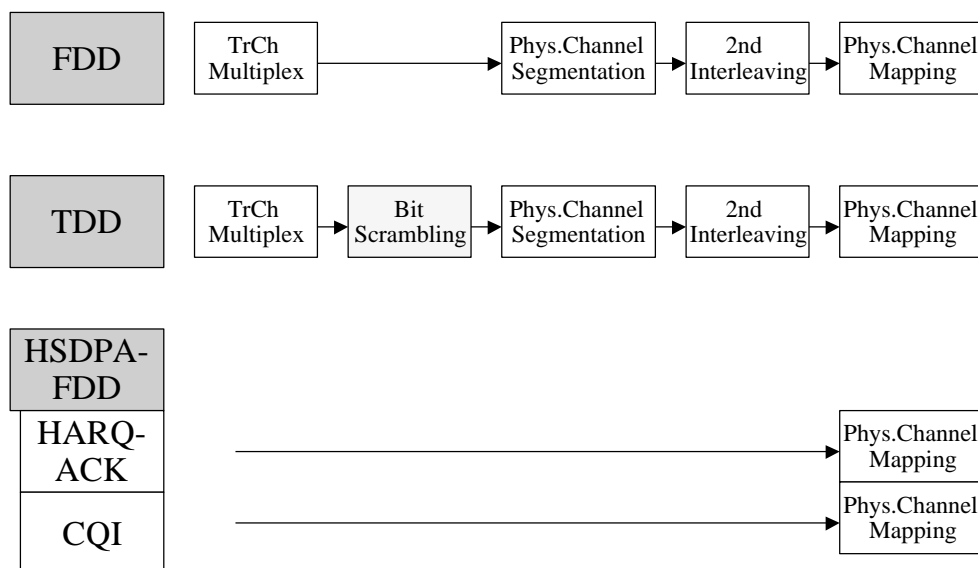


Figure 4-4: Block Matrix Uplink Transmitter –Physical Channel Processing

4.2 Functionality Matrix for Downlink Receiver

The whole DL Rx diagram for physical processing is shown below.

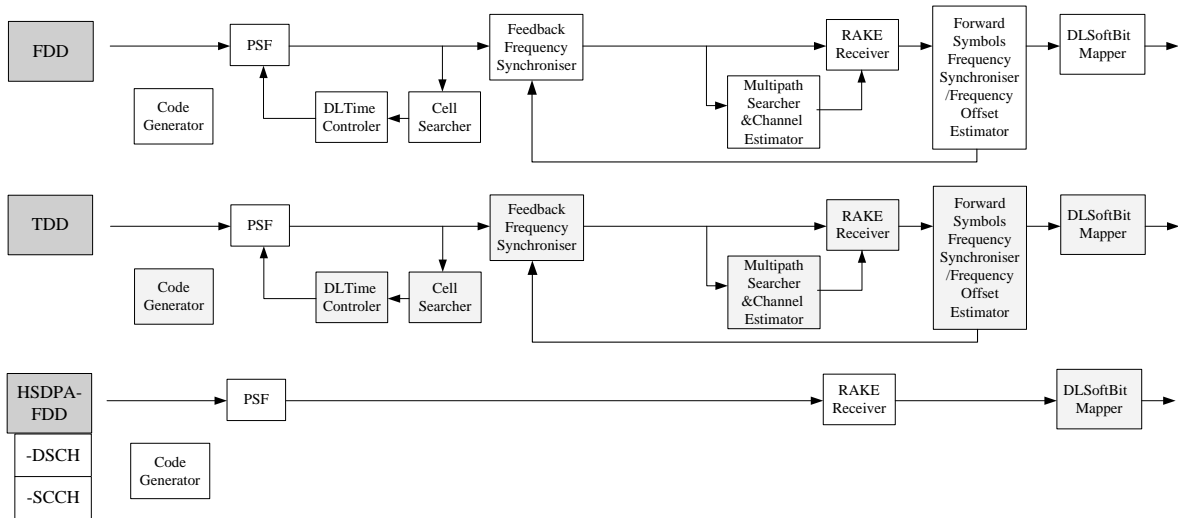


Figure 4-5: Block Matrix Downlink Receiver

4.2.1 Sample Processing

The block embedded within the 'Sample Processing' with the exception of 'Cell Searcher' are functional identical for all modes.

Therefore, the 'ADC', 'Pulse Shaper', 'Feedback Frequency Synchronizer', 'Rx Gain Controller' and 'DL Time Controller' do not need re-configuring.

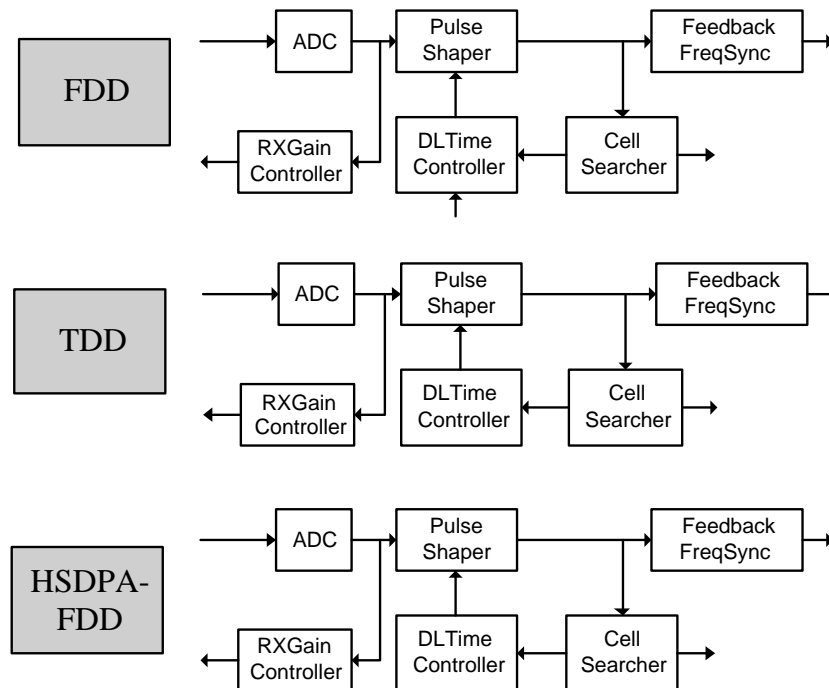


Figure 4-6: Block Matrix Downlink Receiver - Sample Processing

The functional matrix for 'Cell Searching', which is identical for FDD and HSDPA-FDD, but differs for TDD is described in the following subsection.

4.2.1.1 Cell Search

The functionality block matrix for cell search is depicted in Figure 4-7.

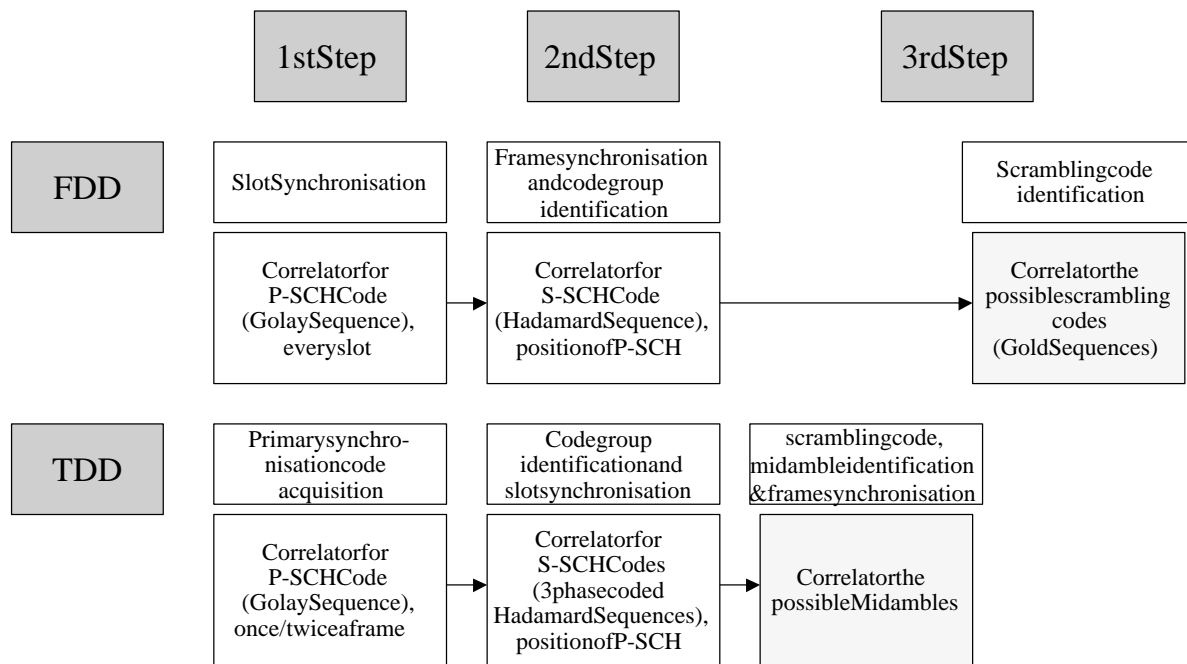


Figure 4-7: Block Matrix Downlink Receiver – Cell Search

The code sequences for the first two steps are the same in FDD and in TDD mode; although, control and evaluation results of these two steps are different. These sequences for FDD are received every slot while the TDD sequences are only received once or twice a frame. While in FDD mode slot synchronisation is achieved after the 1st step, in the TDD mode it is achieved after the 2nd step. The demand for coherence is higher for the 2nd step of TDD, as the S-SCH is phase coded. The codes in the 3rd step are different in both the two modes. In FDD mode the cell specific scrambling code is derived through correlating with the CPICH. In TDD mode it is deduced from the correlation with the midamble of the P-CCPCH.

4.2.2 Chip Processing

The receiver 'Chip Processing' top level descriptions shown in Figure 4-8 is similar for both FDD and TDD.

The functional similarities or differences between these constituent blocks are as follows:

- ❑ The code generation for FDD and HSDPA is the same, but differs for TDD mode. For training sequences, pilot chip patterns are used for FDD and HSDPA, whereas midambles are used for TDD. The scrambling and synchronization code generators for TDD are also different, but the OVSF codes are all the same.
- ❑ The 'Multipath Searcher and Channel Estimation' are identical for both FDD and HSDPA -FDD, but the configurability for TDD will depend on the algorithm chosen for the channel estimation.
- ❑ The 'RAKE Receiver' presents a slight discrepancy in the management of the signal between the UMTS/TDD and the UMTS/FDD. However, it should be noted that there are many similarities between these modes and reduction of configuration complexity will be possible.
- ❑ The only parameter for 'Forward Symbols Frequency Synchronization' that needs to be configured is the 'number of channels', which is independent of the FDD/TDD mode of operation.

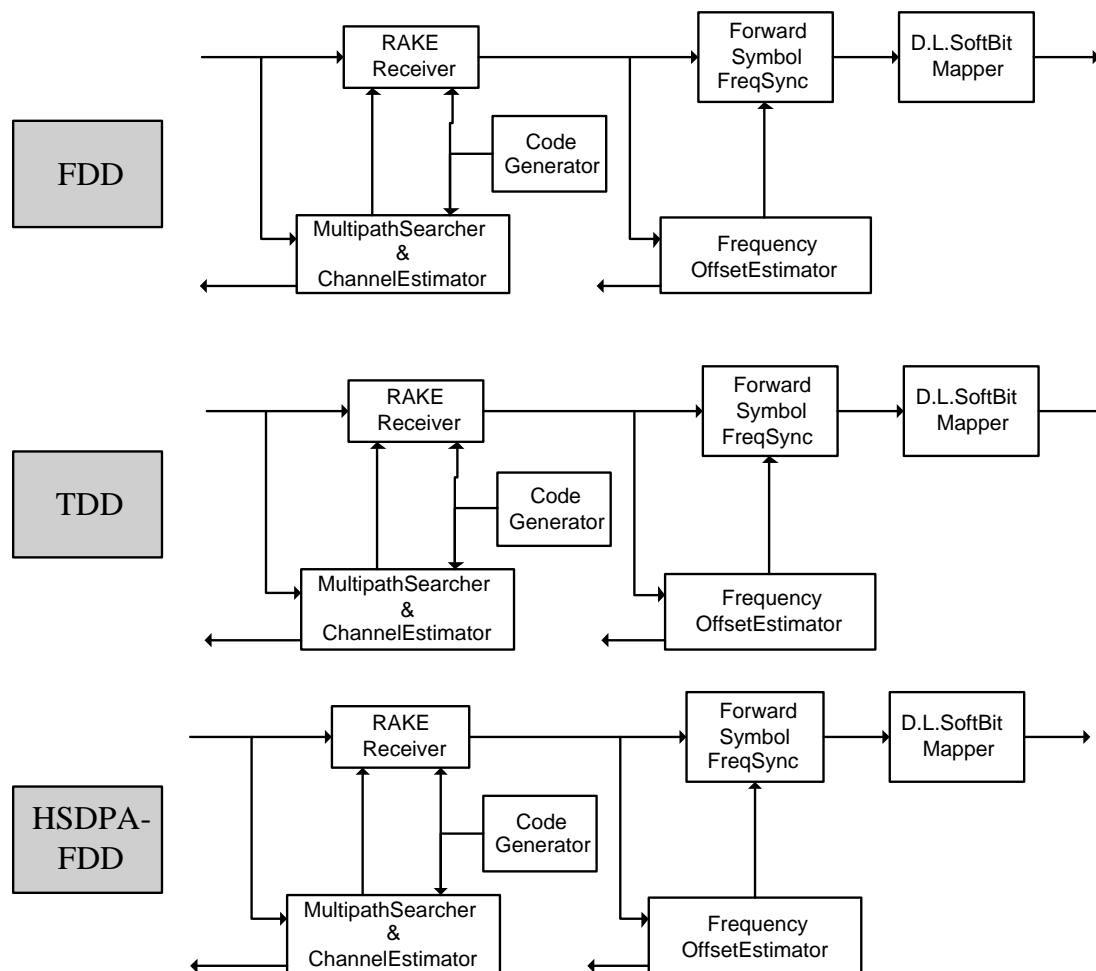


Figure 4-8: Block Matrix Downlink Receiver – Chip Processing

- The configurability (both intra and inter mode) of the 'Frequency Offset Estimation block' depends mainly on the algorithm choice (see section 3.1.3.7). Further inspection and algorithm study is required.
- In UMTS/TDD and UMTS/FDD, QPSK and $\pi/4$ offset QPSK modulation are used respectively. The discrepancy between the different QPSK schemes used in UMTS/FDD and UMTS/TDD will be further inspected. In HSDPA/FDD, where 16-QAM can be applied, 'DL Softbit mapper' needs special care to extract reliably the constituent bits from the soft value of the received symbol.

4.2.3 Physical Channel Processing

As for the uplink transmitter, the functionalities shown in Figure 4-9 are also quite similar between FDD and TDD. Again, the Bits scrambling is unique for TDD and will therefore not be reusable. Transport channel de-multiplexer and Physical channel de-segmentation are more or less the same for FDD and TDD. Again, the TDD 2nd de-interleaver is more complex, as it has to cope with frame and time slot based interleaving. The de-interleaver itself is the same as in the FDD mode. Physical channel de-mapping has to be further inspected for its re-configurability. HSDPA needs no Transport channel de-multiplexer. There re-configurability for the DSCH de-interleaver has to be further inspected. A new functionality is the constellation re-arrangement for 16-QAM, which is unique to HSDPA.

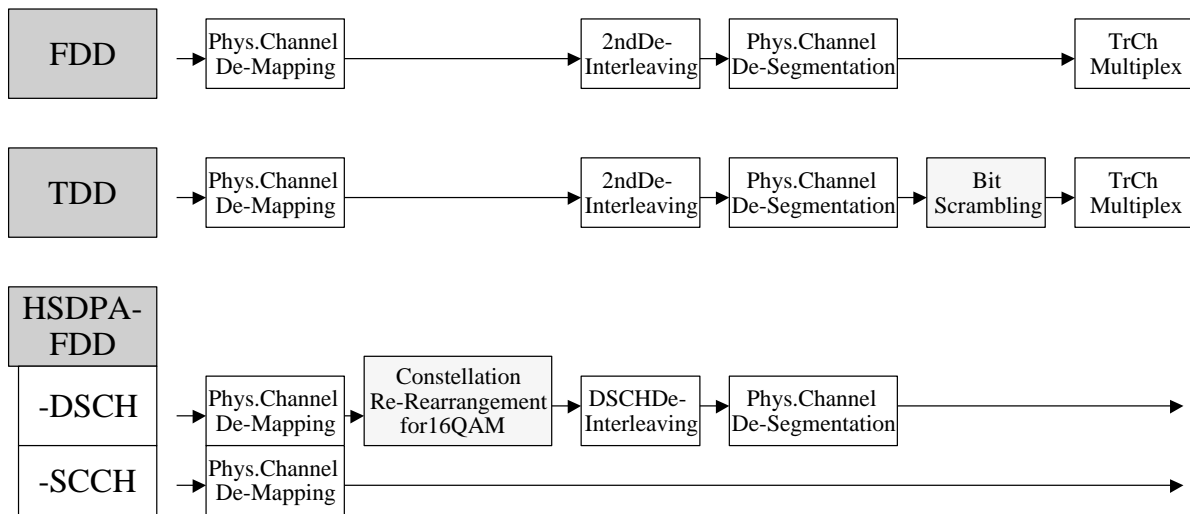


Figure 4-9: Block Matrix Downlink Receiver – Physical Channel Processing

4.2.4 Transport Channel Processing

The functionality block matrix for the downlink receiver providing the transport channel processing is shown in Figure 4-10. Channel decoding, Transport Block de- concatenation/Code Block de- segmentation and the CRC check are the same for FDD and TDD. HSDPA uses the same functionalities but with a subset of parameters only.

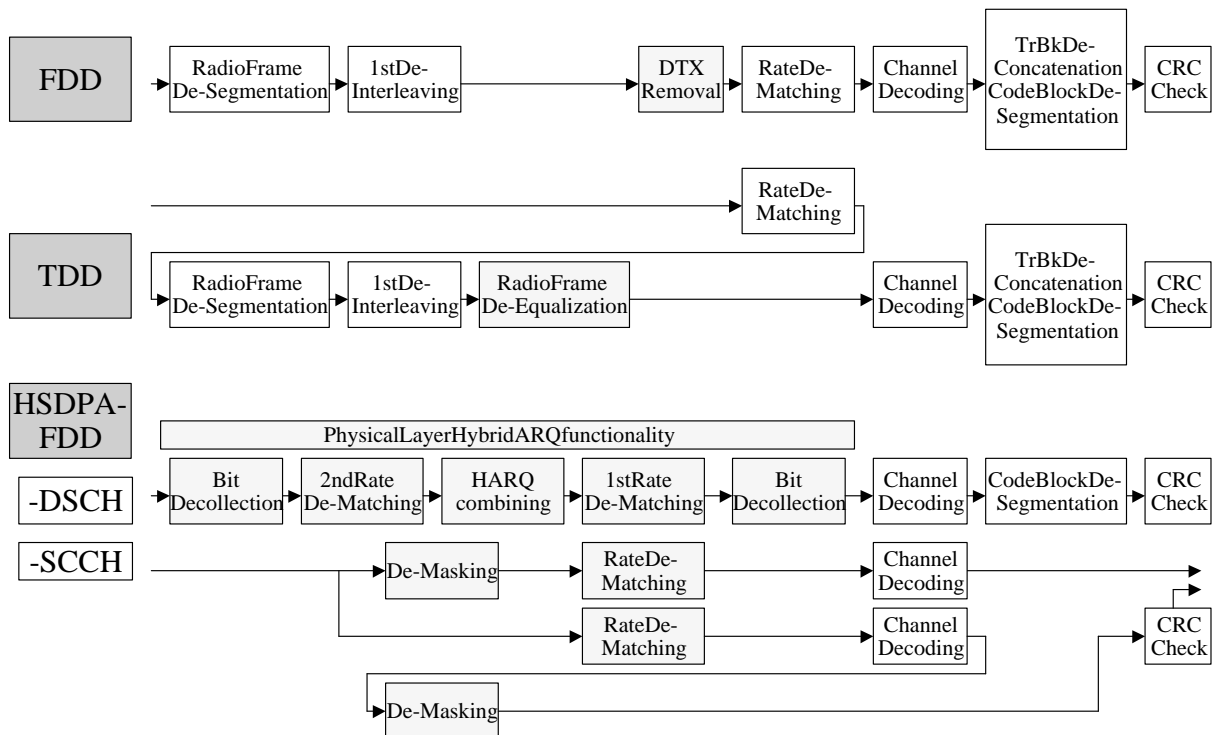


Figure 4-10: Block Matrix Downlink Receiver – Transport Channel Processing

As in Uplink the rate matching has to be further inspected. Radio frame equalization is not utilized in FDD and is therefore needed in TDD only. Radio frame de- segmentation and the 1st De- interleaver have to be further inspected, although there are not many differences. Special for HSDPA is the whole HARQ functionality. The 1st rate matcher is similar to the FDD rate matcher, there- configurability has to be examined. The channel decoder, code block de- segmentation and the CRC check are the

same as for FDD and TDD. Transport block de -concatenation is not needed. Further in the HSDPA -
 SCCH the unique functionality of UE specific masking is necessary.

4.3 System Partitioning

When it comes to the realization of communications systems the system designer or architect has to decide, which part of the system is mapped to which part of the available resources. Furthermore the question arises, which part of the system should be implemented in hardware and which part could be managed by a software implementation. It becomes obvious that throughout the partitioning process section boundaries will be inherently defined.

These boundaries, e.g., refer to the separation between analog front -end and digital baseband (which we can refer to as horizontal partitioning) or to the separation between software, re -configurable hardware and dedicated hardware (which can be referred to as vertical partitioning -see Figure 4-11).

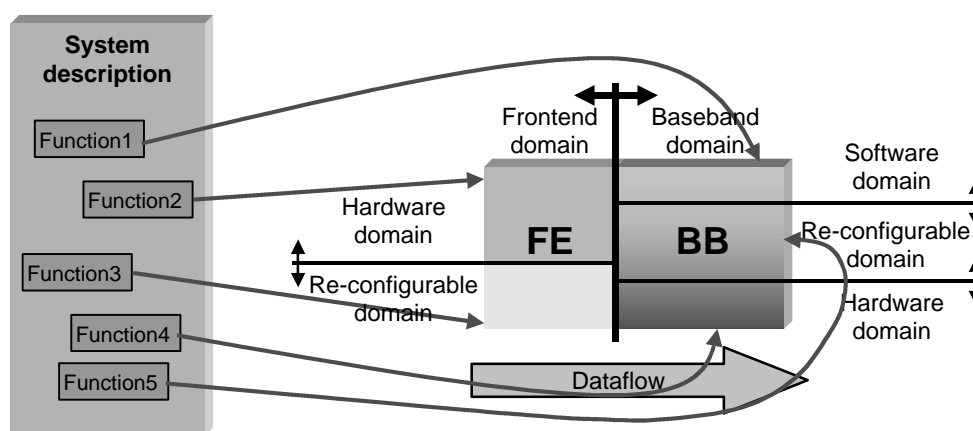


Figure 4-11: FE/BB partitioning degrees of freedom

Horizontal partitioning is mainly defined by technological constraints. The border between the analog world and the digital world can be slightly moved but remains a natural barrier that cannot be shifted out of the system completely. Vertical partitioning offers much more degrees of freedom, especially when using not only microprocessors and dedicated hardware but also re -configurable hardware.

Today, systems for real -time applications are usually implemented by using a mixture of software and hardware based subsystems utilizing microprocessors, digital signal processors and dedicated or re -configurable hardware. Generally, software is used for features and flexibility, while hardware is necessary to achieve the required performance. Introducing re -configurable hardware could be an option to increase flexibility on a higher performance level compared to general -purpose processors.

4.3.1 Digital baseband HW/SW partitioning

Important for the successful application of hardware/software co -design in a re -configurable digital baseband architecture is that the intended behaviour of the overall system is allowed to influence the selection of the hardware architecture to a greater extent than it does in current practice. This does even more apply in the case of re -configurable software -defined architectures. The hardware architecture selection includes

- Characterise the functions of the system and the operations they require.
- Selection of suitable microprocessor and/or DSP
- Development of suitable re -configurable technologies
- Definition of characteristics of the application -specific circuit to be designed (if any)

To decide on different features of the hardware architecture, it is important to have ways of assessing the consequence of a certain architectural choice. Therefore models are needed estimating the impact

of decisions on selected criteria (e.g. timing, area). Unified description language for the microprocessor (i.e. the software world) and the ASIC (i.e. the hardware world) domain are needed.

Currently System C (<http://www.systemc.org>) is seen as a promising description language throughout the whole design process, starting from algorithm design and evaluation down to HW and SW implementation. System C is a standard design and verification language built in C++ that spans from concept to implementation in hardware and software.

A simplified typical system on chip architecture, which can be used for a re-configurable digital baseband design inside a multi-mode radio, is shown in Figure 4-12.

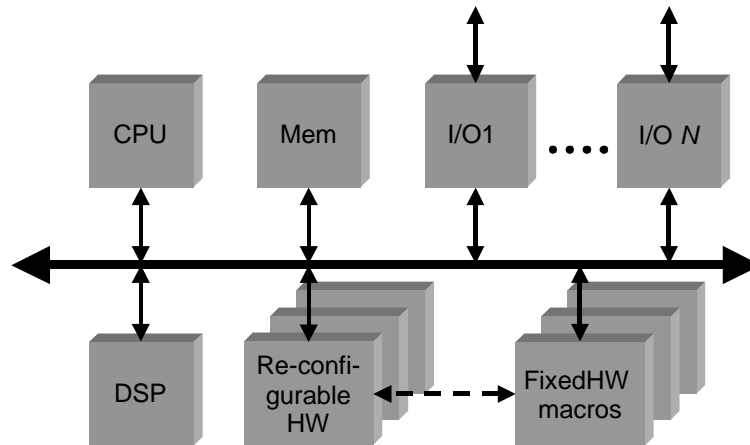


Figure 4-12: Typical SoC design

The architecture contains the processors, memory and interfaces. Additionally there are fixed functionality HW macros (e.g. for Viterbi decoding) and re-configurable HW macros, intending to reach DSP flexibility with ASIC processing performance.

4.3.2 Component Interaction

Embedded systems, like multi-mode systems, typically have many activities (or tasks) occurring in parallel (concurrent). Concurrent tasks are the natural mode for e.g. many real-time applications. It results in a separation of concerns of *what* each task does from *when* it does it. Concurrent tasks allow a greater scheduling flexibility since time-critical tasks may be given higher priority. However, concurrent multi-tasking introduces complexity into the system, since these tasks have to interact with each other, especially if the different tasks execute asynchronously, i.e. at different speeds. There are three types of interactions between concurrent tasks possible:

1. Communication to transfer data between tasks
2. Synchronization to coordinate tasks
3. Mutual exclusion to control access to shared resources

This task interaction leads to three types of behaviour:

1. Independent tasks have no interaction with each other
2. Co-operating tasks communicate and synchronize to perform some common operation
3. Competing tasks communicate and synchronize to obtain access to shared resources

During the functional partitioning process dedicated resources, which may be an application specific circuit or a microprocessor/DSP, are allocated for a dedicated task. When this allocation is done on a shared resource (e.g. processor, memory or even a shared HW accelerator component), the system designer has to take care about what mechanisms are provided to enable the resource to execute one task and to change its activity to another task. Additional topics that must be paid attention to are

timing and priority issues, to fulfil performance requirements and to avoid deadlock situations respectively.

4.3.3 Partitioning process

The system-level partitioning problem refers to the assignment of operations to hardware or software. A hardware/software partitioning map, linking the system behaviour functions to hardware resources is shown in Figure 4-13.

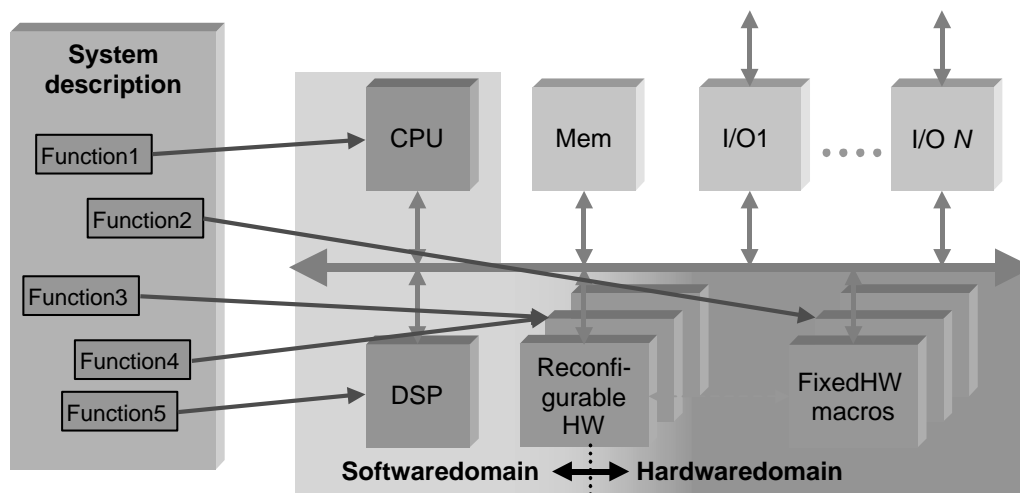


Figure 4-13: HW/SW Partitioning Map

The overall system performance is determined by the effect of hardware-
software partition on utilization of the processor and the bandwidth of the intercommunication architecture (i.e. the bus system) between the processor and the application specific hardware. An efficient way to do this would be to define a partition cost function that captures these properties and use it to direct the partitioning algorithm towards a desired solution (i.e. the minimum value of the partition cost function).

5 Interface to Front -End

In this chapter the interface of the digital multi-mode baseband to RF front-end will be explained. Only the interface will be described, not the front-end functionality. The uplink channel and front-end is assumed to be ideal. Thus the downlink (UE) receiver will be dealt with. The front-end interface can be separated into three different types of functionality – data interface, control interface and configuration interface – as given in Table 5.1.

Data interface	Interface describing the source (user) data flow between the digital baseband and analog front-end
Control interface	Interface describing the control data flow to define the behavior of front-end. The control data is coming from higher protocol layers (L2, L3) or can be generated inside the physical layer (L1) itself.
Configuration interface	Interface describing the control data flow in order to define the configuration of the analog front-end. The configuration data is generated by L1 itself, based on L2/L3 control signals.

Table 5.1: Front -end Interface Functionality

In addition to the data path the digital baseband will configure the front-end according to the required mode and also has to fine-tune some front-end blocks during operation. The digital baseband will provide status information on the quality of the received downlink data stream. The properties of the digital baseband signals are influenced from the analog front-end receiver functions. The front-end can use the control information in order to improve the quality of the received signals.

In Figure 5-1 an example of this digital baseband to analog front-end feedback control information is shown for the frequency synchronization. Two loops may operate in parallel, one slow analog correction loop, adjusting the VCO only in steps, and one fast digital frequency correction loop doing the final frequency synchronization.

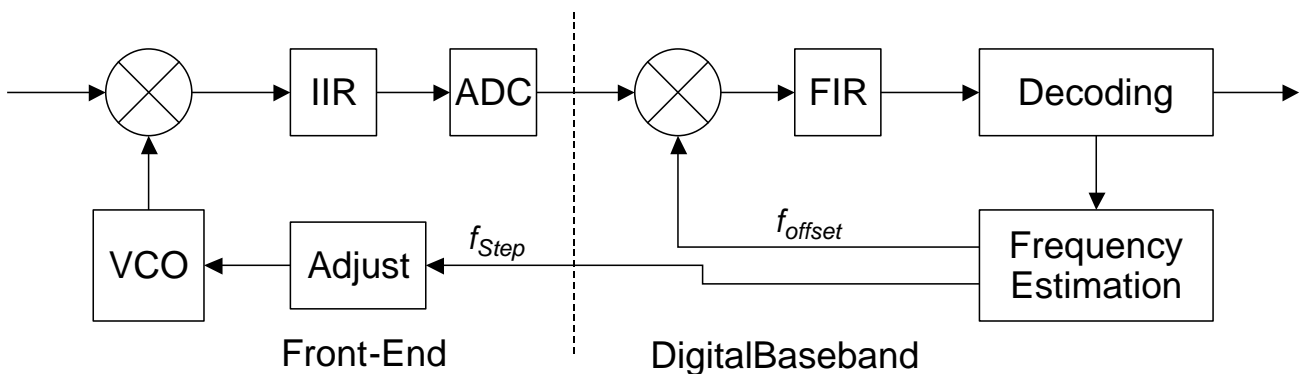


Figure 5-1: Front -End Interface Functionality –Example

This figure is just one example about the possibilities of the digital baseband feedback to the analog front-end. The detailed capabilities and functionalities will be developed throughout WP2 and WP3 in a close co-operation.

There are two possibilities for the implementation of the control and configuration interfaces:

- *Analog interface*

This would require separate DACs and ADCs in the digital baseband part for each status and control signal. Therefore the implementation requires some process requirements for the

ADC/DAC implementation. Additional to this the analog interface is vulnerable to signal distortions.

- *Digital interface*

This would allow the implementation of a digital bus system down into the analog front part. This enables a standardized interface for all control information, which can be easily extended to the needed control information space. -end

This second solution will be used for the MuMoR system. A single master digital bus system driven by a digital baseband block and terminated in the front -end will be used. Each target address means a different parameter to be set and will be recognized by the respective block(s). This seems to be the most promising approach because it is very flexible according to interface requirements, which are not yet obvious. The following table shows exemplary configuration parameters, which may be configured (once) or (continuously/repeatedly) set via the bus.

Parameter	Description	Normal Mode	Multi Mode
SetGainfactors	The power amplifier gain factor(s), per I & Q or together	<input type="checkbox"/>	<input type="checkbox"/>
ConfigSynthesizer	Frequency set	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
ConfigBiascurrent	For each analogue block shall the Bias current be optimised for low power, a nd rise for bad conditions.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Loopfrequencydrift	Temperature and component variability correction	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
ModeSwitch	Multiple reconfiguration	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Fieldstrength	Measurement output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Table 5.2: Exemplary front -end configuration parameters

The detailed configuration capabilities of the analog front -end and the required digital baseband control and status parameter will be defined jointly throughout the project work in WP2 and WP3.

The interface to the analog front -end will then have the following definition:

Interface Signal	Direction	Length
<i>Data Interface</i>		
I-phased downlink data signal	In	ADC ¹
Q-phased downlink data signal	In	ADC
I-phase uplink data signal	Out	DAC ²
Q-phase uplink data signal	Out	DAC
<i>Control Interface</i>		
Control Address	Out	8 ³

¹The required resolution of the ADC will be evaluated in a later stage of the project in cooperation with working package 2.

²The required resolution of the DAC will be evaluated in a later stage of the project in cooperation with working package 2.

InterfaceSignal	Direction	Length
Writedatabus	Out	8
Enable	Out	1
ReadnotWrite	Out	1
Acknowledgement	In	1
Readdatabus	In	8
<i>ConfigurationInterface</i>		
UMTSnotHSDPA	Out	1
FDDnotTDD	Out	1
GSMsupport ⁴	Out	1

Table 5.3: TheselectedFDDHS -DSCHphysicallayercategory

Thecontrolinterfacewillimplementadigitalbussystemwithasimpleasynchronousprotocolbased onhandshakesignals(Enable –Acknowledgement).Mappingthefront -endcontroland status parametertoaregistermap,accessibleviaadigitalbussystem,providesamodularandscalable configurationrange.

Thefunctionalityofthesignalsisdefinedasfollows:

- *ControlAddress*
This8 -bitaddressdefinesthetargetbyteaddressforthe currentdatatransfer.Itisvalidas longastheenablesignalhasbeenasserted.
- *Writedatabus*
This8 -bitdatabuscontainsthedatatobetransferredduringawritetransfer.Itisvalidas longastheenablesignalhasbeenasserted.
- *Readdatabus*
This8 -bitdatabuscontainsthereceiveddataduringareadtransfer.Itisvalidaslongasthe acknowledgmentsignalhasbeenasserted.
- *Enable*
Thissignalsinitiatesanewdatatransfer.Anewdatatransfercanonlybeinitializedif acknowledgementhas beende -asserted.
- *ReadnotWrite*
Thissignalsindicates,whethercurrentdatatransferisread('1')orwrite('0')transfer.It isvalidaslongastheenablesignalhasbeenasserted.
- *Acknowledgement*

³Thiswillallowaccessing256one -bytereisters.Thiscouldbeincreased,byextendingthebitwidthofthe addresssignal,accord ingtotheneededconfigurationspace.

⁴GSMisnotinthefocusoftheMuMoRprojectforthedigitalbaseband,butwillbeconsideredtosomeextend intheanalogfront -end.

This signal indicates the master that the data has been stored at the receiver during a write transfer, or the data has been placed on the read data bus during a read transfer. The acknowledgement signal has to be de-asserted on the de-assertion of the enable signal.

The protocol timing is shown in an example write transfer, followed by a read transfer as shown in the following Figure 5-2.

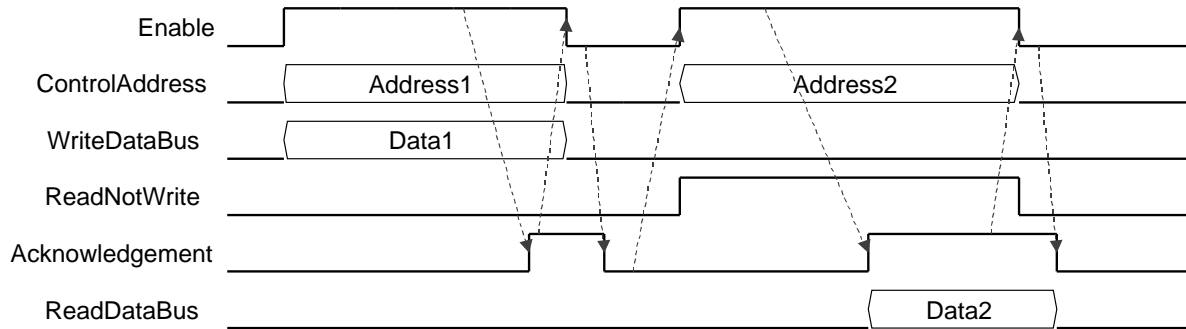


Figure 5-2: Control Interface Protocol

6 Verification channel Model and Propagation conditions

These set of channel models and propagation conditions specified by 3GPP will be described here. These models are needed for the evaluation of the three possible modes (UMTS FDD/TDD, and HSDPA FDD).

This chapter provides an overview over Propagation conditions according to TS25.101 especially Chapter A.7 and TS25.102, and Channel model(s) according to TS25.101 and TS25.102. Additionally the restriction of the implemented first channel will be documented.

6.1 UMTS-Spec Values: (B.2) Propagation Conditions

6.1.1 Propagation Conditions

6.1.1.1 Static propagation condition

The propagation for the static performance measurement is an Additive White Gaussian Noise (AWGN) environment. No fading and multipath exist for this propagation model.

6.1.1.2 Multi-path fading propagation conditions

Table 6.1 shows propagation conditions that are used for the performance measurements in multipath fading environment. All taps have classical Dopplers spectrum.

Case1, speed3km/h		Case2, speed3km/h		Case3, speed120 km/h		Case4, speed3km/h		*Case5, speed50km/h		Case6, speed250km/h	
Relative Delay [ns]	Relative mean Power [dB]	Relative Delay [ns]	Relative mean Power [dB]	Relative Delay [ns]	Relative mean Power [dB]	Relative Delay [ns]	Relative mean Power [dB]	Relative Delay [ns]	Relative mean Power [dB]	Relative Delay [ns]	Relative mean Power [dB]
0	0	0	0	0	0	0	0	0	0	0	0
976	-10	976	0	260	-3	976	0	976	-10	260	-3
		20000	0	521	-6					521	-6
				781	-9					781	-9

NOTE*: Case5 is only used in TS25.133.

Table 6.1: Propagation Conditions for Multipath Fading Environments

6.1.1.3 Moving propagation conditions

The dynamic propagation conditions for the test of the baseband performance are non-fading channel models with two taps. The moving propagation condition has two taps, one static, Path 0, and one moving, Path 1. The time difference between the two paths is according Equation

$$\Delta \tau = B + \frac{A}{2} (1 + \sin(\Delta \omega \cdot t))$$

The taps have equal strengths and equal phases.

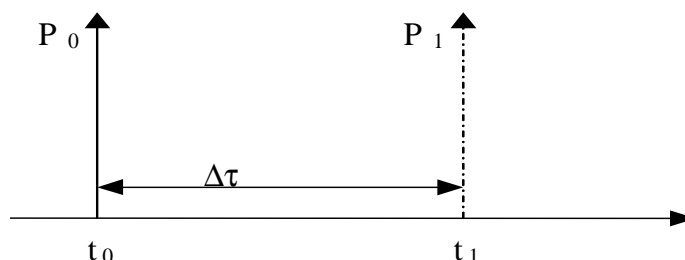


Figure 6-1: The moving propagation conditions

The parameters in the equation are shown in the following **Table 6.2.**

Parameter	Value
A	5 μs
B	1 μs
$\Delta\omega$	$40 \cdot 10^{-3} \text{s}^{-1}$

Table 6.2: Parameters of the Moving Propagation Conditions

6.1.1.4 Birth-Death propagation conditions

The dynamic propagation conditions for the test of the baseband performance are a non-fading propagation channel with two taps. The moving propagation condition has two taps, Path 1 and Path 2, which alternate between 'birth' and 'death'. The positions the paths appear are randomly selected with an equal probability rate and are shown in Figure 6-2.

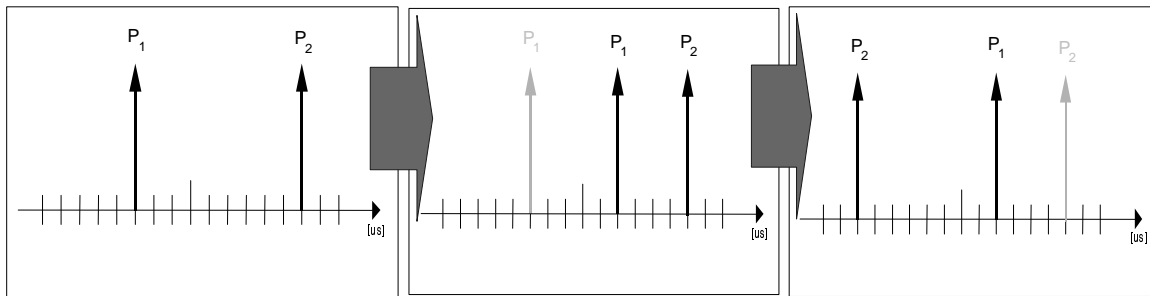


Figure 6-2: Propagation Conditions for Multipath Fading Environments

Birth-death propagation sequence

- Two paths, Path 1 and Path 2 are randomly selected from the group $[-5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5]$ μs . The paths have equal magnitudes and equal phases.
- After 191 ms, Path 1 vanishes and reappears immediately at a new location randomly selected from the group $[-5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5]$ μs but excluding the point Path 2. The magnitudes and the phases of the tap coefficients of Path 1 and Path 2 shall remain unaltered.
- After an additional 191 ms, Path 2 vanishes and reappears immediately at a new location randomly selected from the group $[-5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5]$ μs but excluding the point Path 1. The magnitudes and the phases of the tap coefficients of Path 1 and Path 2 shall remain unaltered.

This sequence in 2) and 3) is repeated.

6.1.2 Channel Model: Spurious Emissions

The spurious emissions requirements apply to all out-of-band frequencies that are not covered by the definition of limits in the emission mask section. Additional requirements are established for the GSM and PCS frequency operating bands. The limits for these frequency bands are valid for integer multiples of 200 kHz.

Frequency Bandwidth	Minimum Requirement in dBm	Measurement Bandwidth
9 – 150 (kHz)	-36	1 kHz
150 – 30000 (kHz)	-36	10 kHz

30 –1000 (MHz)	-36	100kHz
1 –12.75(GHz)	-30	1MHz

Table 6.3: Requirements For Spurious Emissions (FDD)

Frequency Bandwidth	Minimum Requirement in dBm	Measurement Bandwidth
925 –935 (MHz)	-67	100kHz
935 –960 (MHz)	-79	100kHz
1805 –1880 (MHz)	-71	100kHz
1893.5 –1919.6 (MHz)	-41	300kHz

Table 6.4: Additional Requirements For Spurious Emissions (FDD)

Sources for spurious emissions are the harmonic generation of the oscillator and mixer as well as nonlinearities of the power amplifier. Especially spurious emissions in the receive band are critical since the duplex switch has to provide a sufficient attenuation of the spurious emissions in order not to degrade the performance of the receiver in terms of dynamic range and intermodulation problems.

6.2 Rayleigh Channel Model with simplified Front -End

The following Model is developed in collaboration with WP2. This channel model to be applied has to support at least the following physical effects:

- Multiple paths (at least 4)
- Different delays for each path.
- Different gains for each path.
- An additional Gaussian distributed noise.
- A Rayleigh distributed gain for the paths.
- Neighbour channels modelled as high pass filtered white gaussian noise

Besides the channel model also front -end properties affecting the quality of the received signal in the decoding process of the digital baseband are considered. The considered front -end properties are:

- Frequency and phase offset between transmitting and receiving frequency oscillator
- DC offset due to self mixing
- IQ imbalance of the direct conversion receiver
- Quadrature error of the direct conversion receiver
- Adjustable amplifier
- FIR filtering
- Analog-to-digital converter (ADC)

The targeted channel and front -end model is shown in Figure 6-3.

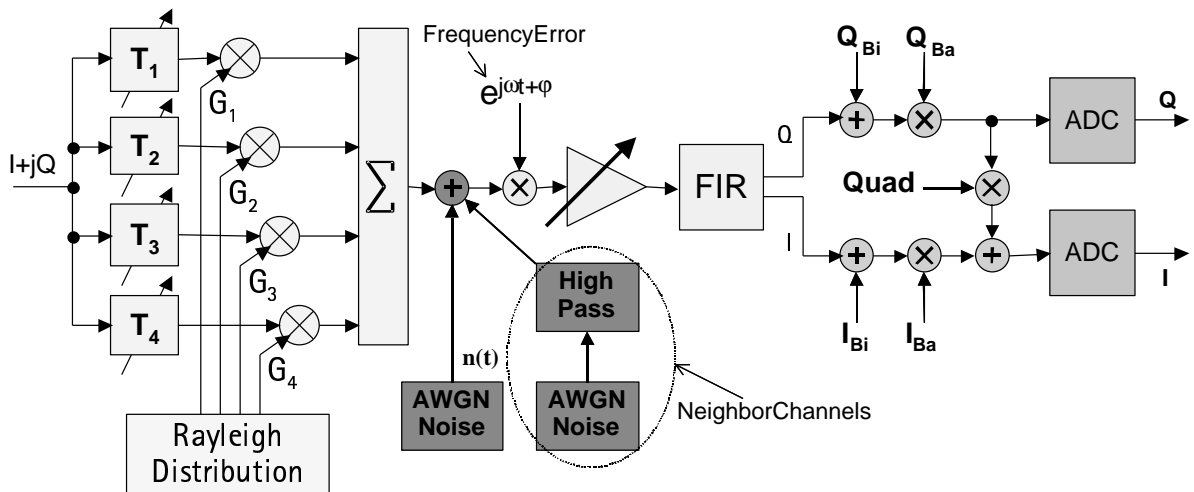


Figure 6-3: ChannelModelwithabstractFront -EndModel

The parameters of these models are listed in Table 6.5. Especially the front -end model will be developed and defined in closeco -operation with the working package 2.

Physicaleffect	Properties	Adjust.
Numberofpaths	4paths	Fix
Pathdelay's.	Staticdelays	Parameter
	Dynamicdelays	Parameter
Pathgain's.	Staticgains	Parameter
	DynamicRaleighdistributed	Parameter
Additivenoise	Gaussiandistributed	Parameter
Frequencyandphaseerror	Staticerror	Parameter
Biaserror	Staticerror	Parameter
Balanceerror	Staticerror	Parameter
Quadratureerror	Staticerror	Parameter
FIR-Filtertoemulatetheanal.Distortion	Bandpass	Parameter
Neighborchanneldistortion	Bandlimitednoise	Parameter
DopplerEffect	FrequencyShift	Parameter

Table 6.5: ChannelModelParameters

7 Conclusion

In this document an overall multi-mode architecture of the mobile terminal covering three modes, i.e. UMTS/FDD, UMTS/TDD, and HSDPA/FDD, was proposed. The first step in proposing the multi-mode architecture was to develop a matrix-like block diagram through each single mode architectural description. By further inspections in the subsequent tasks, other considerations such as algorithmic structures and implementation measures (required processing speed, memory, data size) will be taken into account for further column-wise partitioning.

Because of the complexity of the system, the detailed interface operation of the Front-End and Baseband has to be defined. This will enable a smooth multi-mode operation of a complete mobile terminal.

8 References

The 3GPP standard documents listed in Table 2.1 and Table 3.1 of the MuMoR deliverable D1.1 – Standard Requirements – can be understood as references. In these tables the full name and version number of the documents referenced in the text can be found.

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