


University of Aberdeen

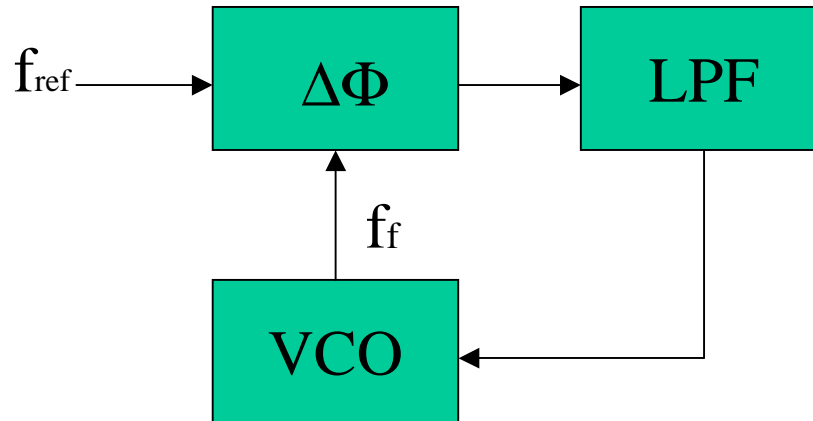


A Programmable
Frequency Synthesiser

Introduction

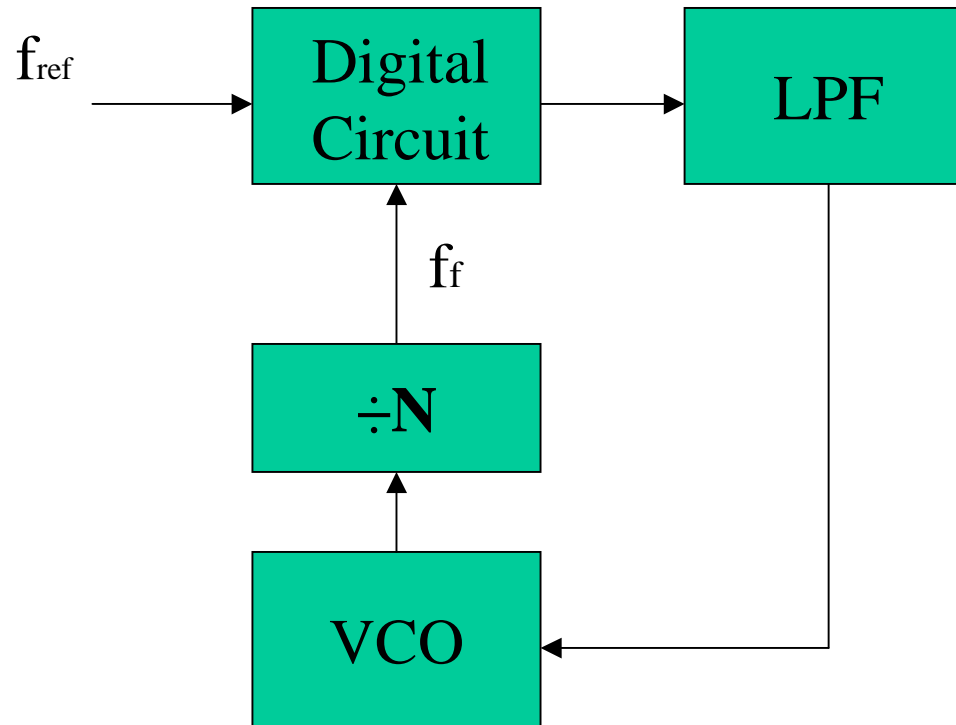
- Conventional PLL \Rightarrow 1975 Patent
Hybrid Wide-band Re-configurable Synthesiser 
- ADS Behavioural Model
- VHDL Simulation (Using Test Bench)
- Mixed Signal Simulation (Verilog AMS)
- Mathematical Analysis of Loop Operation
- Hardware Tests (Open Loop and Closed Loop)

Conventional PLL



- At lock f_f is equal to f_{ref}
- When f_{ref} changes to a new value, the PLL tracks f_{ref} adjusting the phase difference between f_{ref} and f_f
- The phase transfer function characterises the loop, with the VCO contributing a single pole to the transfer function

US Patent 3913028 (1975)



At lock, $f_{ref} \neq f_f$

R.J. Bosselaers proposes a frequency synthesiser using both digital and analogue circuitry

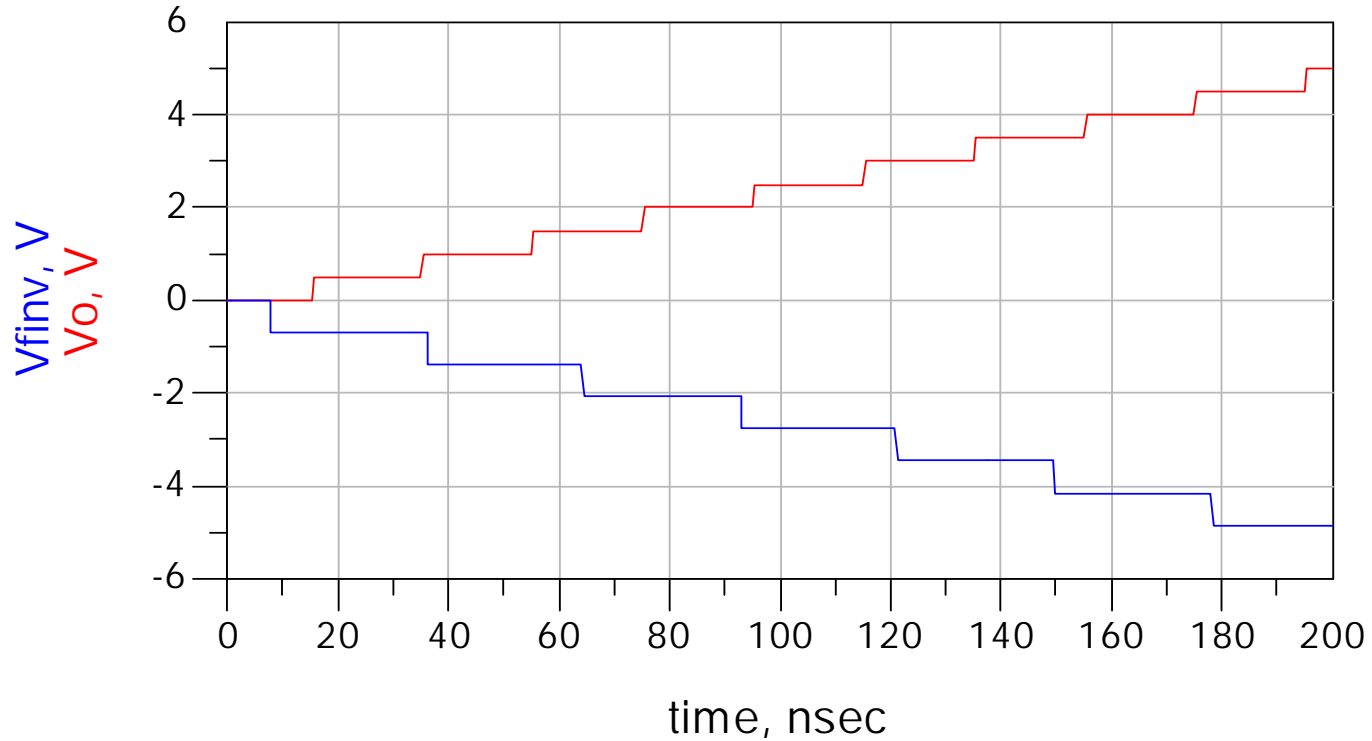
Features of the 1975 design

- Digital circuitry used 2 ALUs
- One ALU clocked by f_{ref}
- Other clocked by f_f
- Problem: 2 ALUs waste power
- Problem: Clock contention

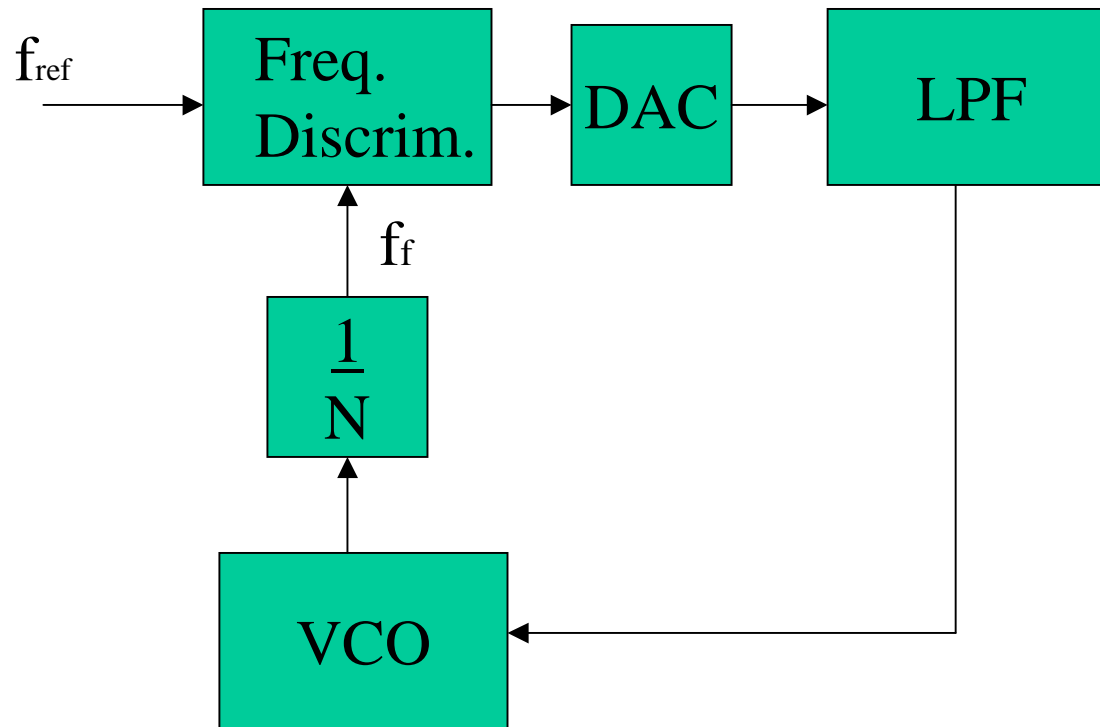


For the water level in the lake to remain constant the loss of water caused by evaporation must be compensated by the gain due to periods of rainfall.

Accumulation of Voltages Due to f_{ref} and f_f

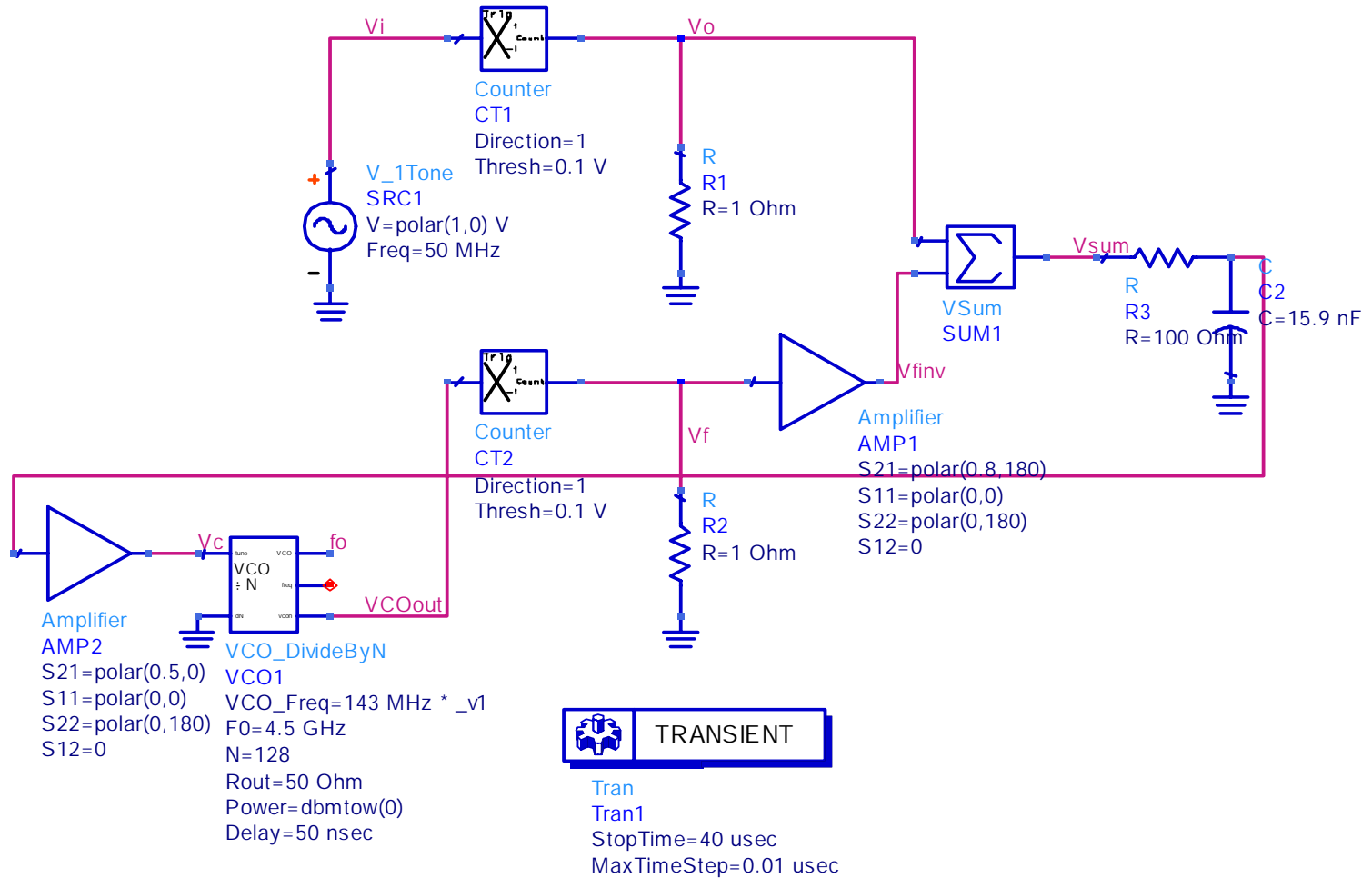


Hybrid Synthesiser

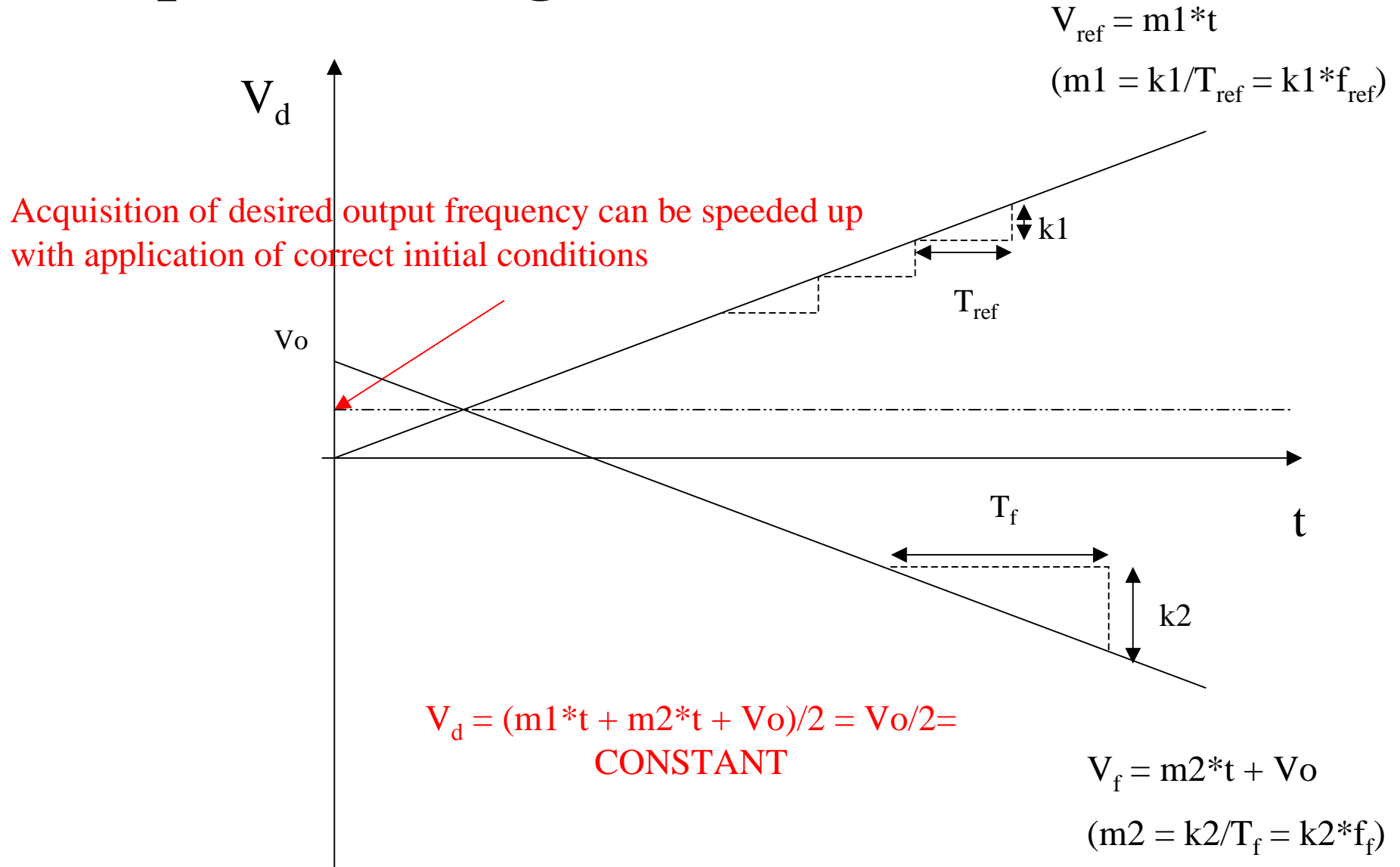


Elements of Verilog-AMS Model

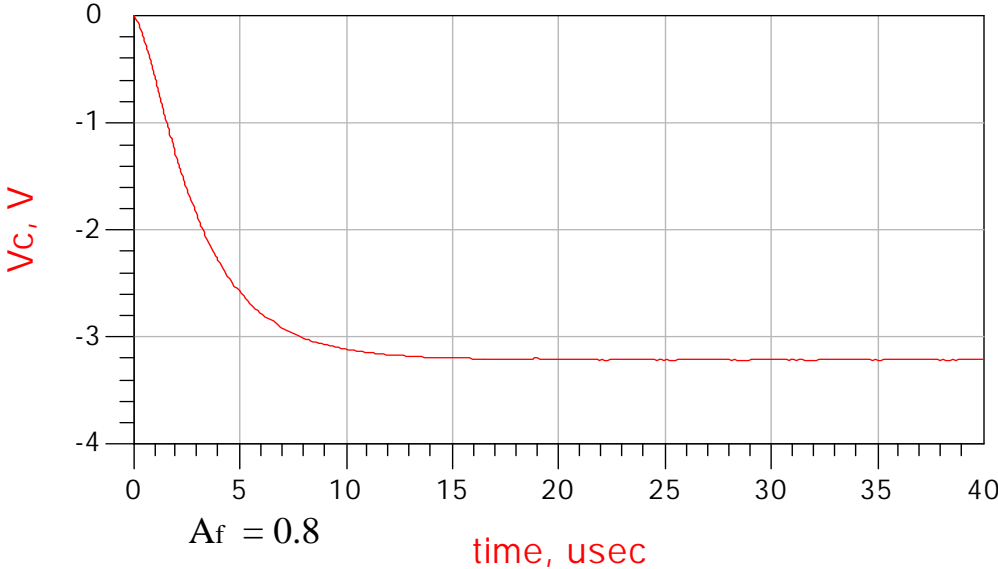
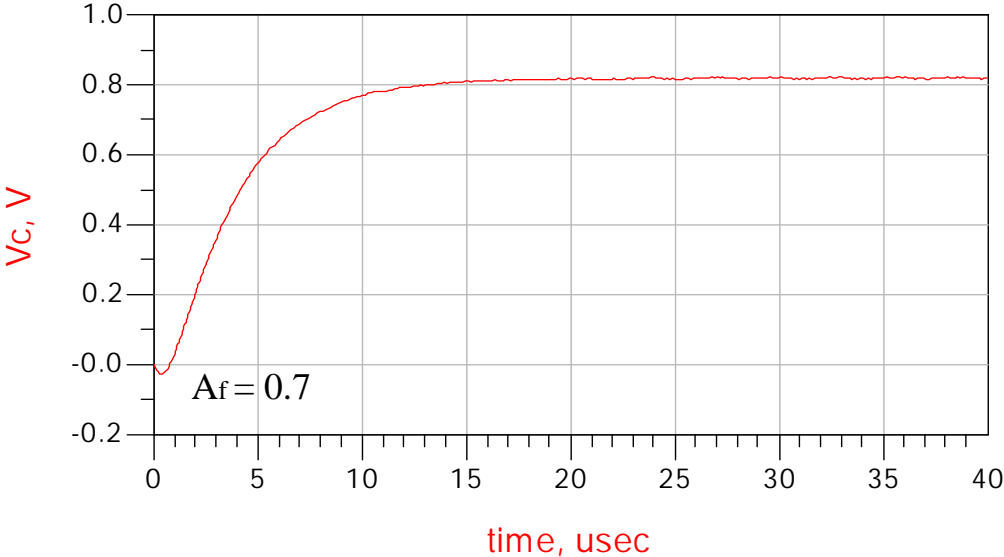
ADS Behavioural Model



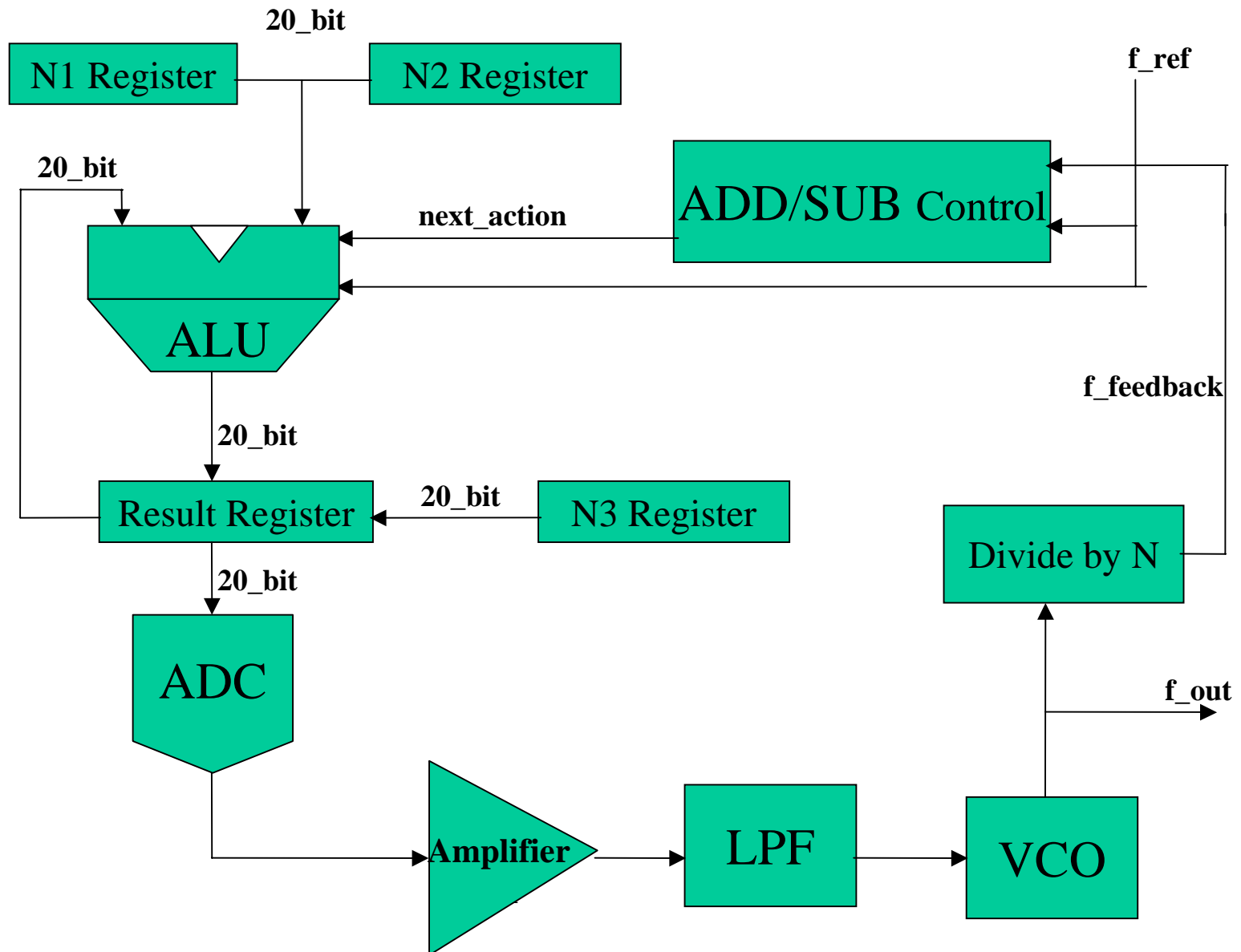
Output of the Digital Circuit



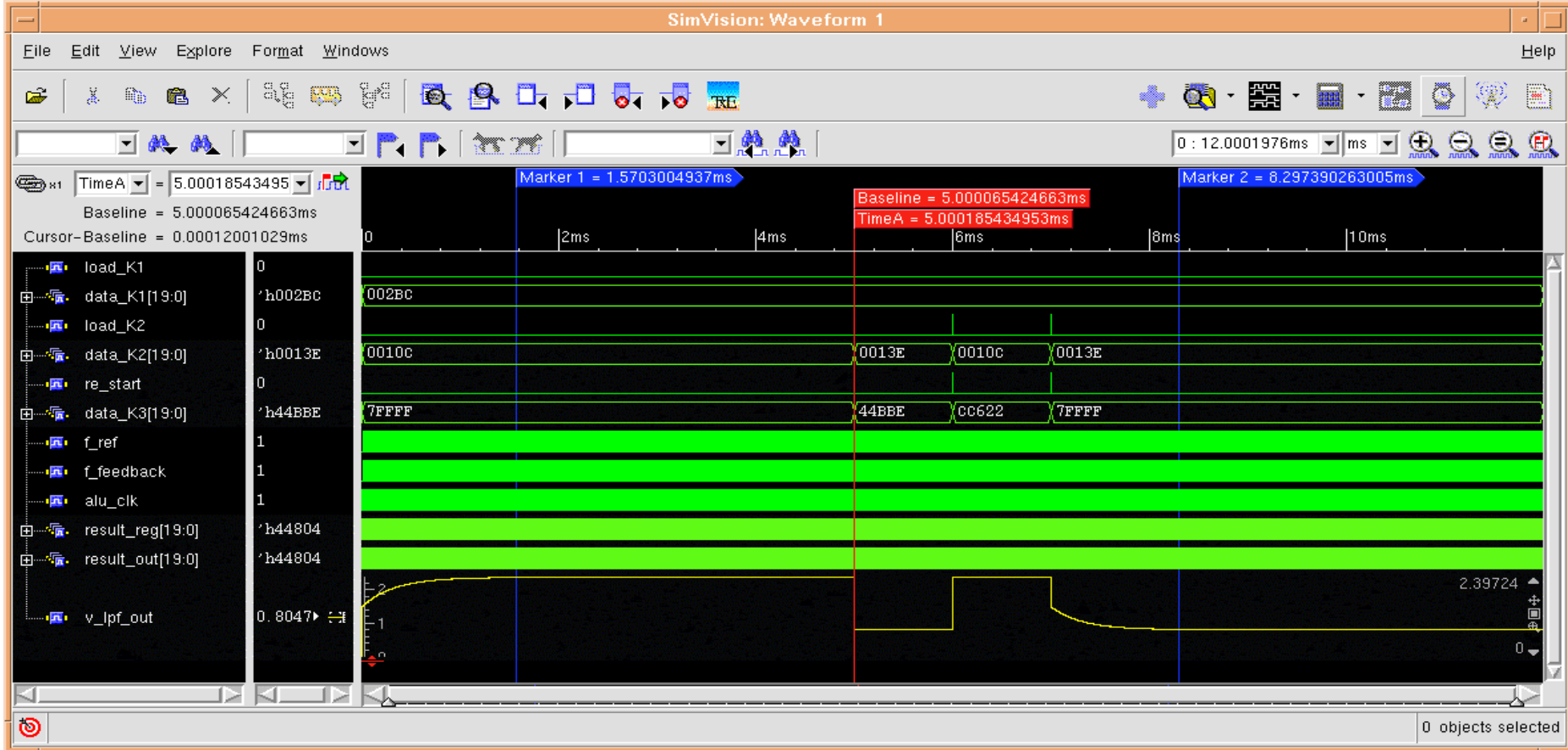
VCO Input Voltages with Differing Frequency Ratios



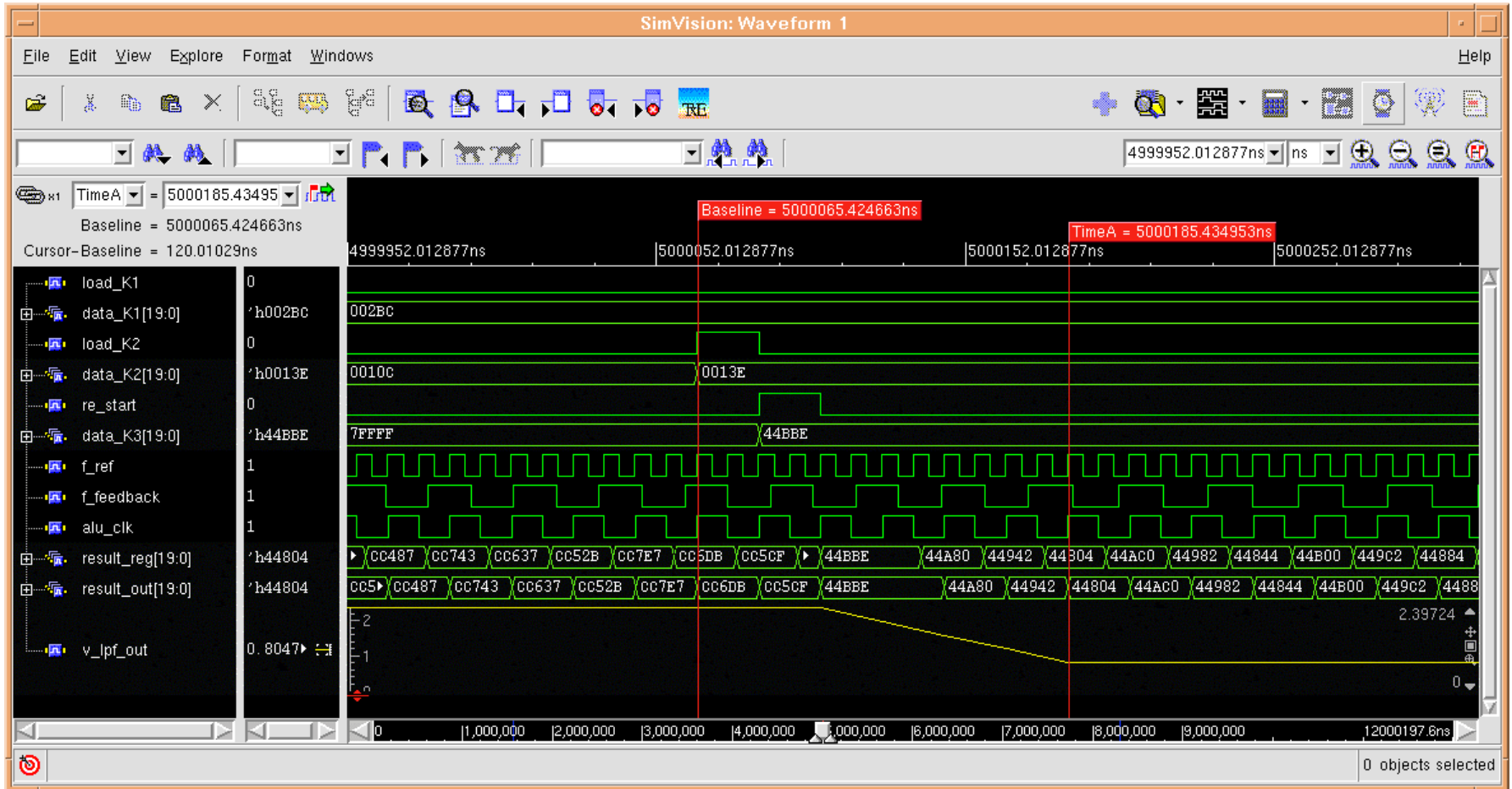
Block Diagram of the VHDL Design Developed at Aberdeen



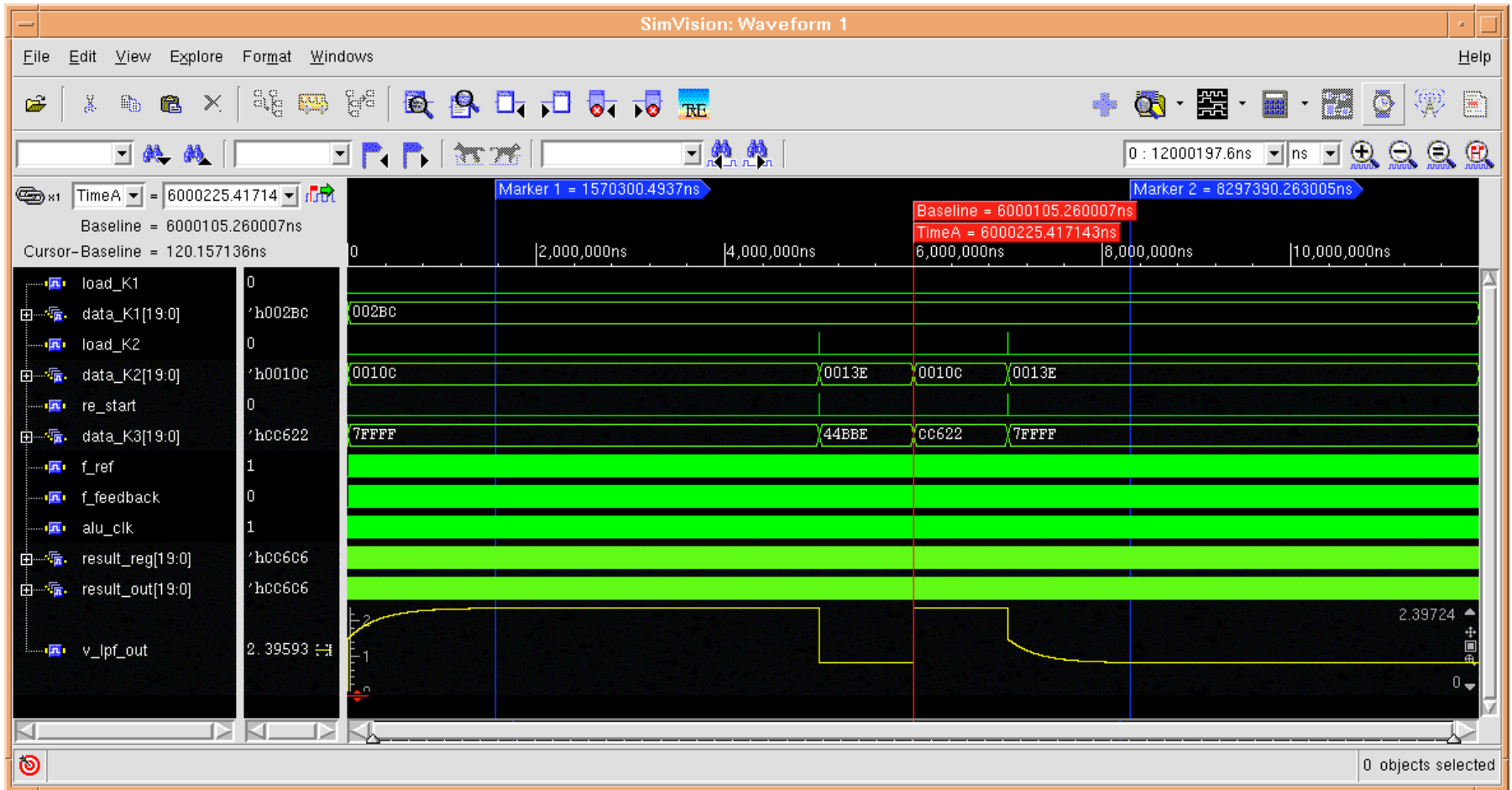
VHDL Simulation at 50 MHz Logic Clock



Expanded View of the Falling Edge of the LPF Output



VHDL Simulation at 50 MHz Logic Clock



Expanded View of the Rising Edge of the LPF Output

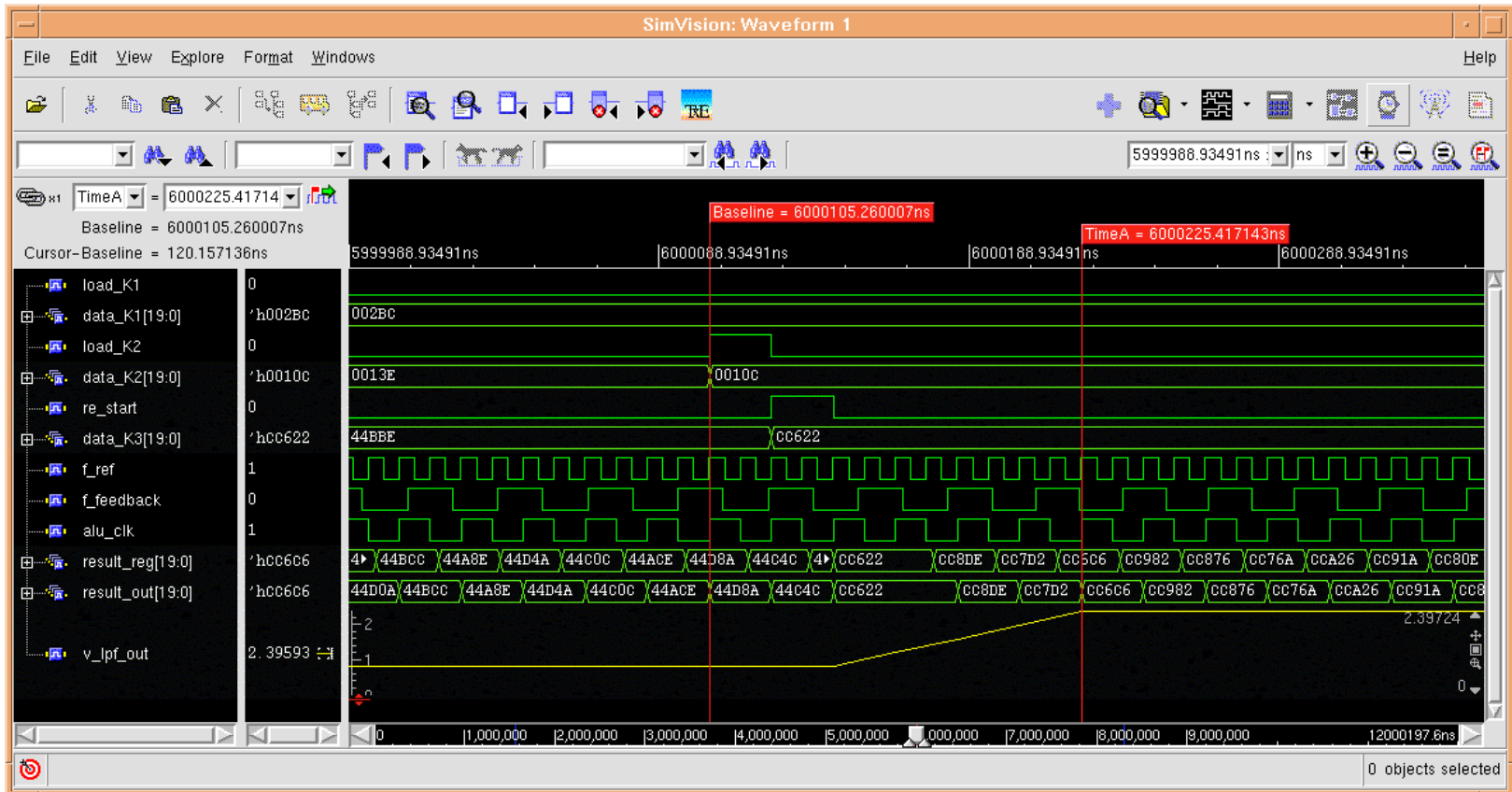
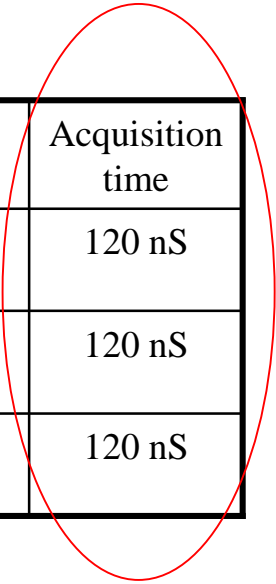


Table 1: Acquisition Time for the Frequency Ratio 7:5

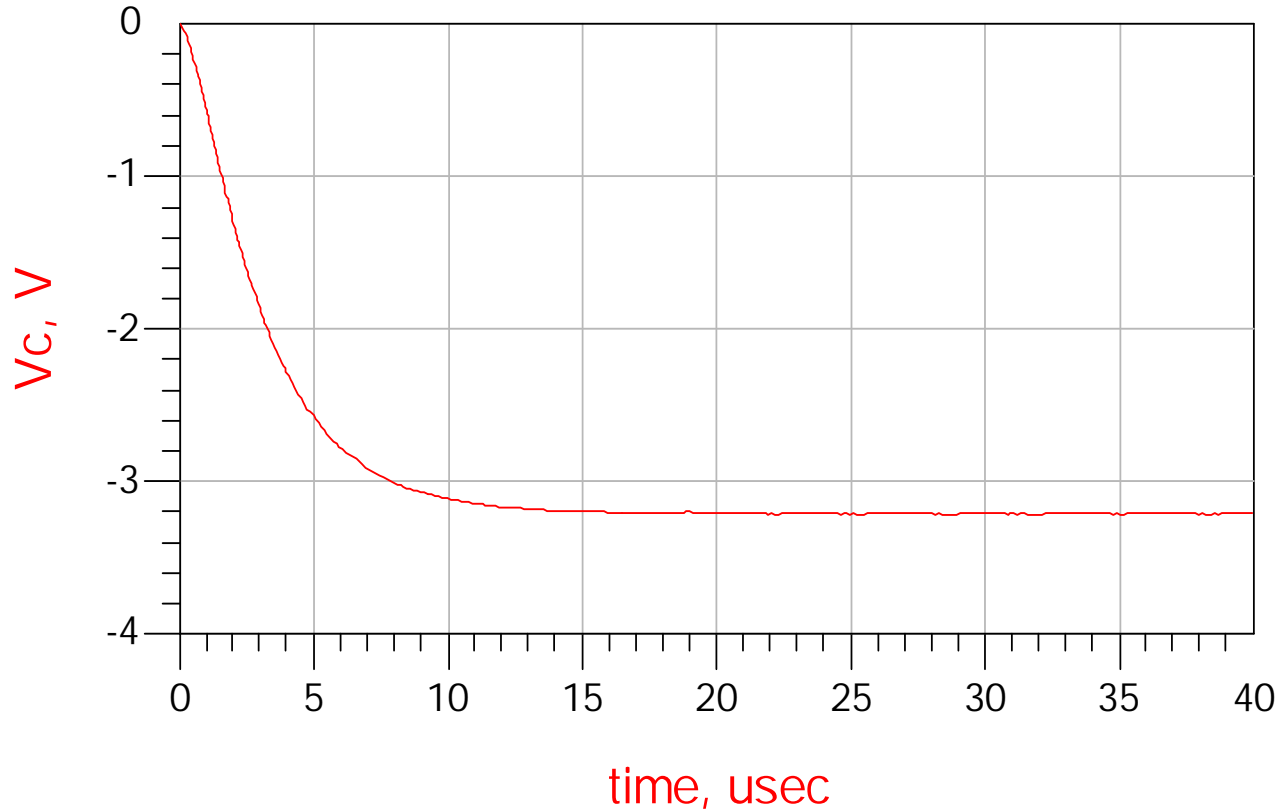
N1	N2	N3	Acquisition time
50	70	MAX/2	> 10 mS
500	700	MAX/2	3.03 mS
5,000	7,000	MAX/2	202 uS
50,000	70,000	MAX/2	21 μ S

Table 2: Acquisition Time with the Predicted Value of N3 at Switching

N1	N2	N3	Acquisition time
5	7	698638	120 nS
50	70	698638	120 nS
500	700	698638	120 nS

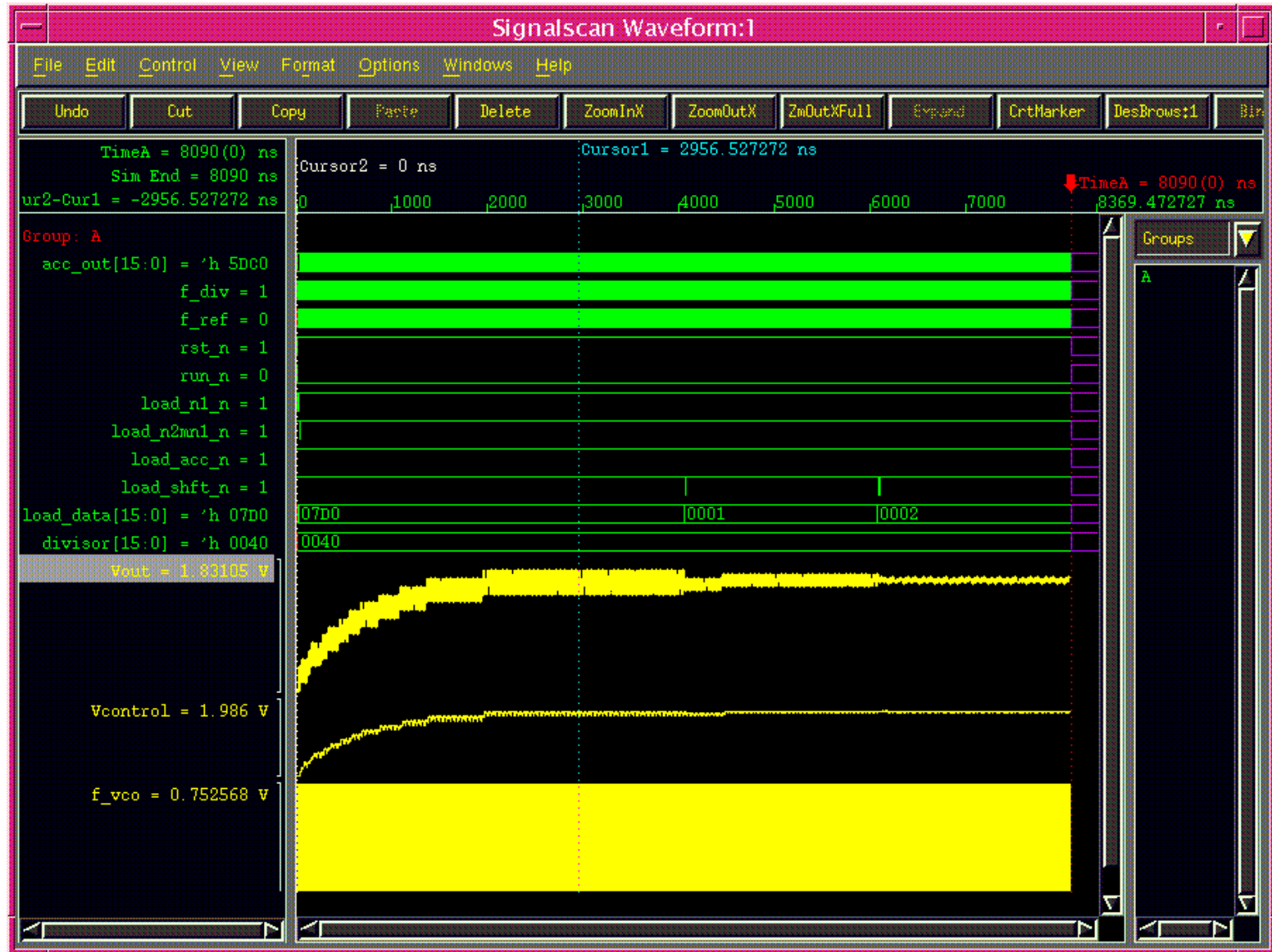


ADS Behavioural Model

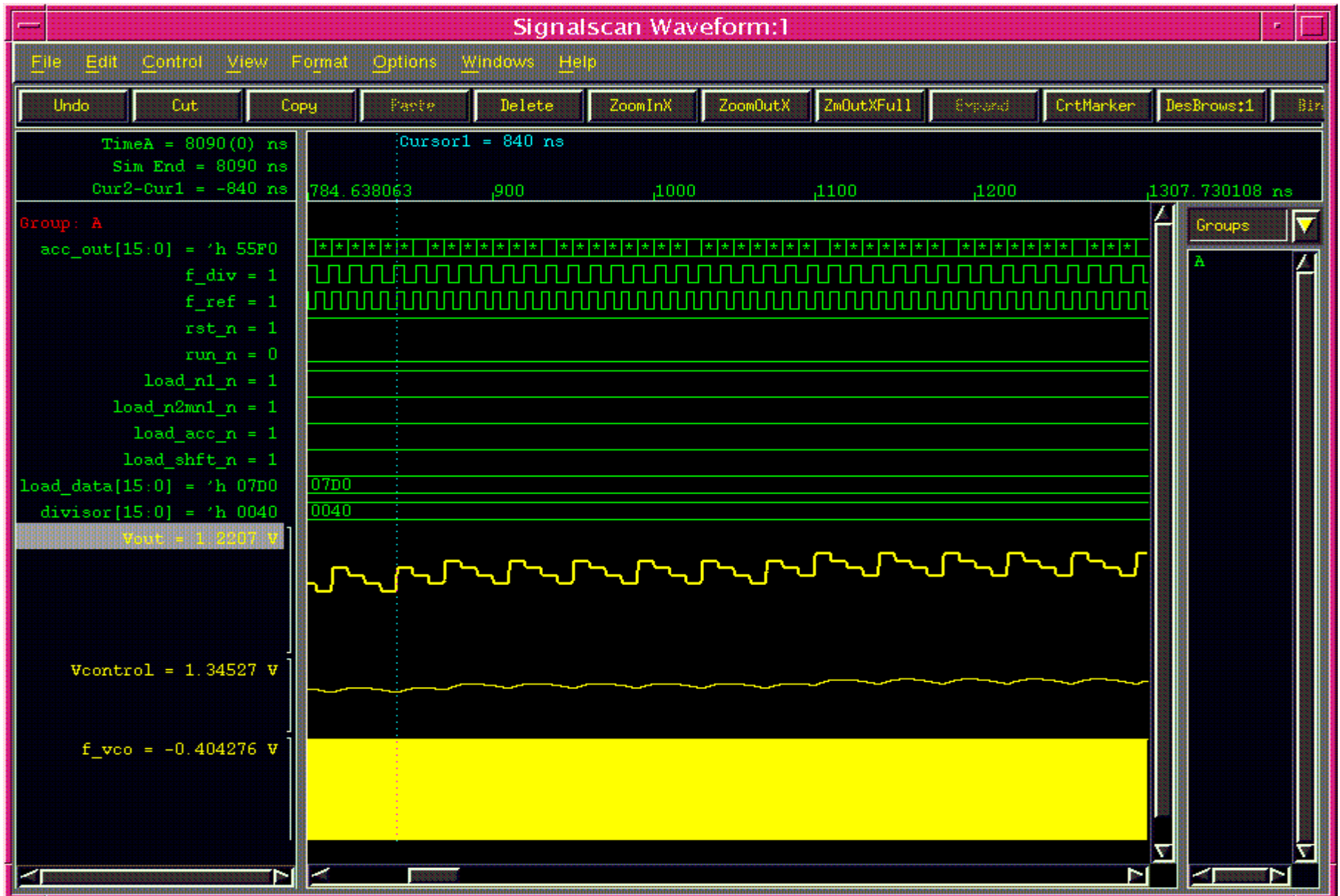


V_c =input voltage of the VCO

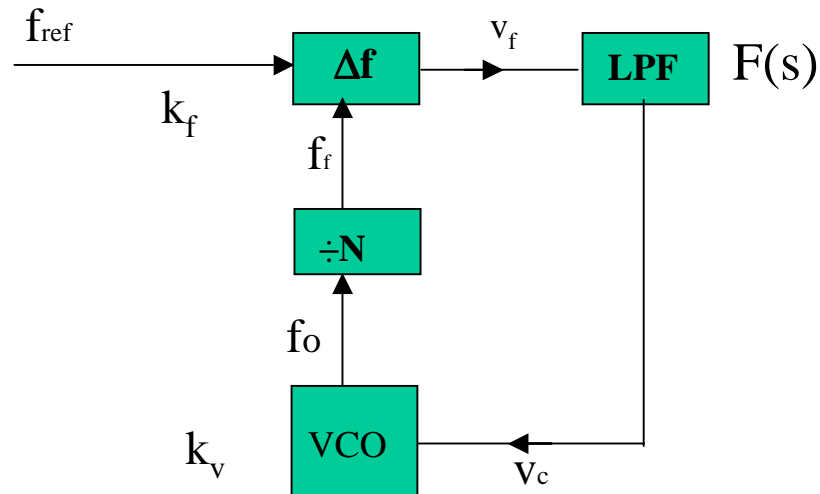
Verilog-AMS Simulation with Frequency Ratio 4:3 and $f_{VCO}=4.8\text{GHz}$



Expanded View



Loop Transfer Function



$$f_0 = k_v v_c$$

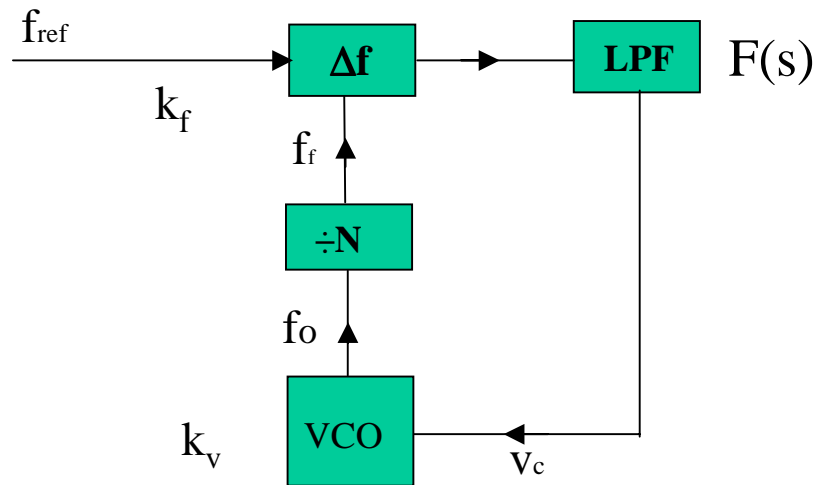
$$F_0(s) = k_v V_c(s) = k_v V_f(s) F(s)$$

$$F_0(s) = k_v k_f (F_{ref}(s) - F_0(s)) F(s)$$

$$F_0(s)(1 + kF(s)) = kF_{ref}(s) F(s)$$

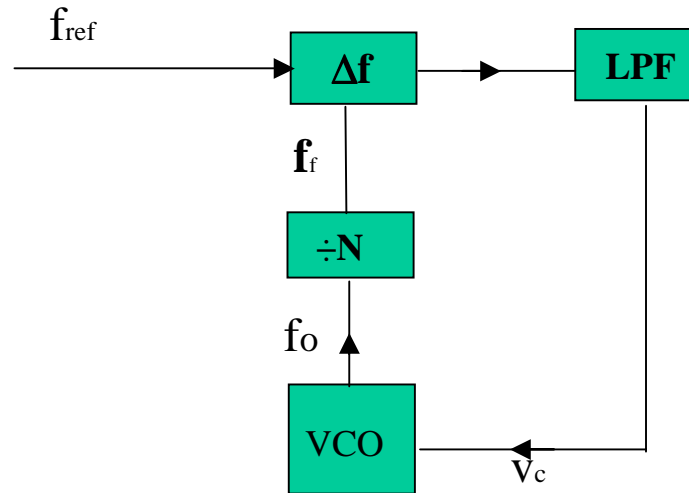
$$k = k_v k_f$$

Loop Transfer Function



$$H(s) = \frac{F_0(s)}{F_{ref}(s)} = \frac{kF(s)}{1 + kF(s)} = \frac{\frac{k}{1 + sT}}{1 + \frac{k}{1 + sT}} = \frac{k}{1 + k + sT}$$

Loop Transfer Function



$$k_1 = 1 + k$$

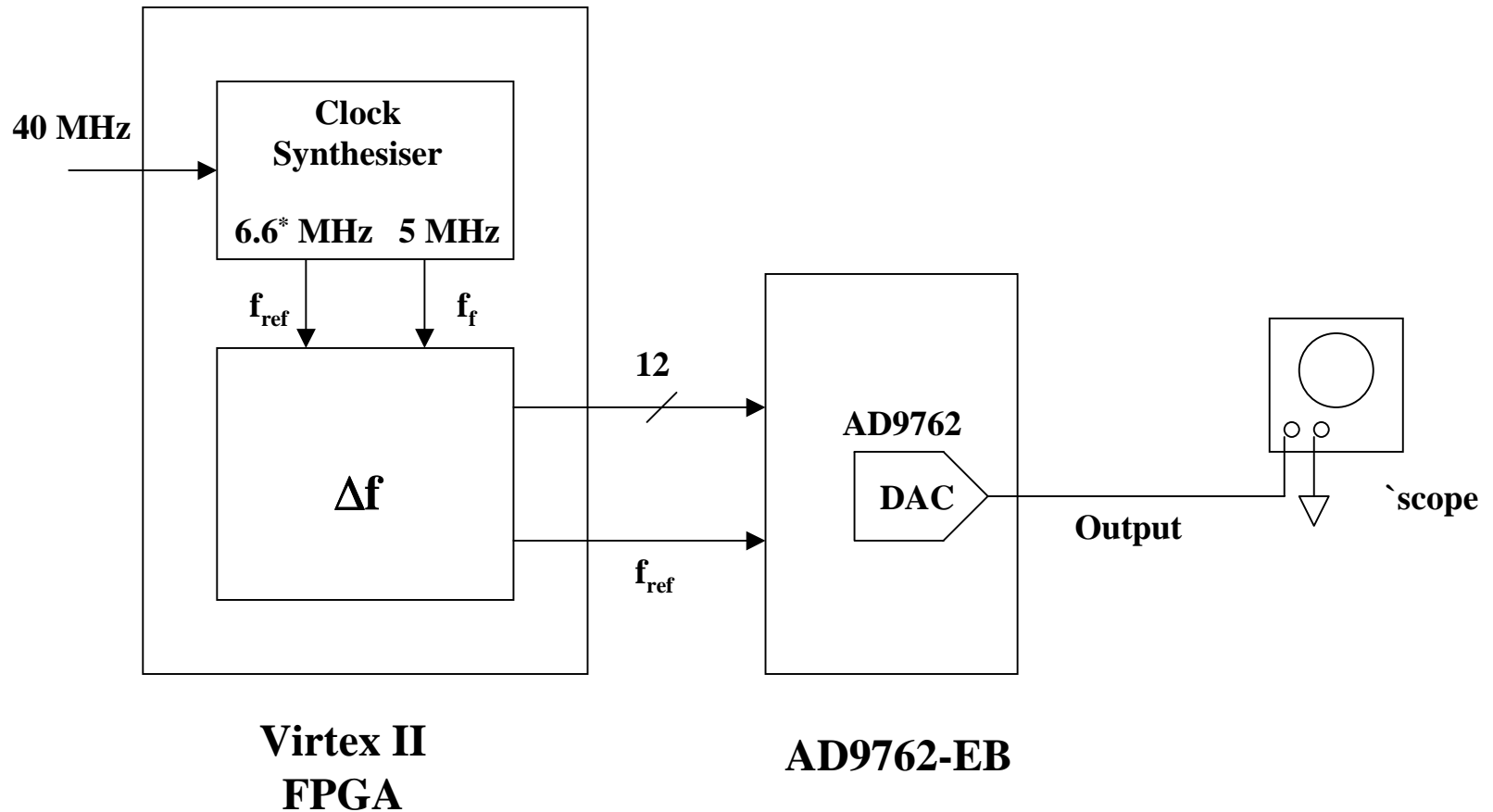
$$k_2 = \frac{k}{T}$$

$$k_3 = \frac{k_1}{T}$$

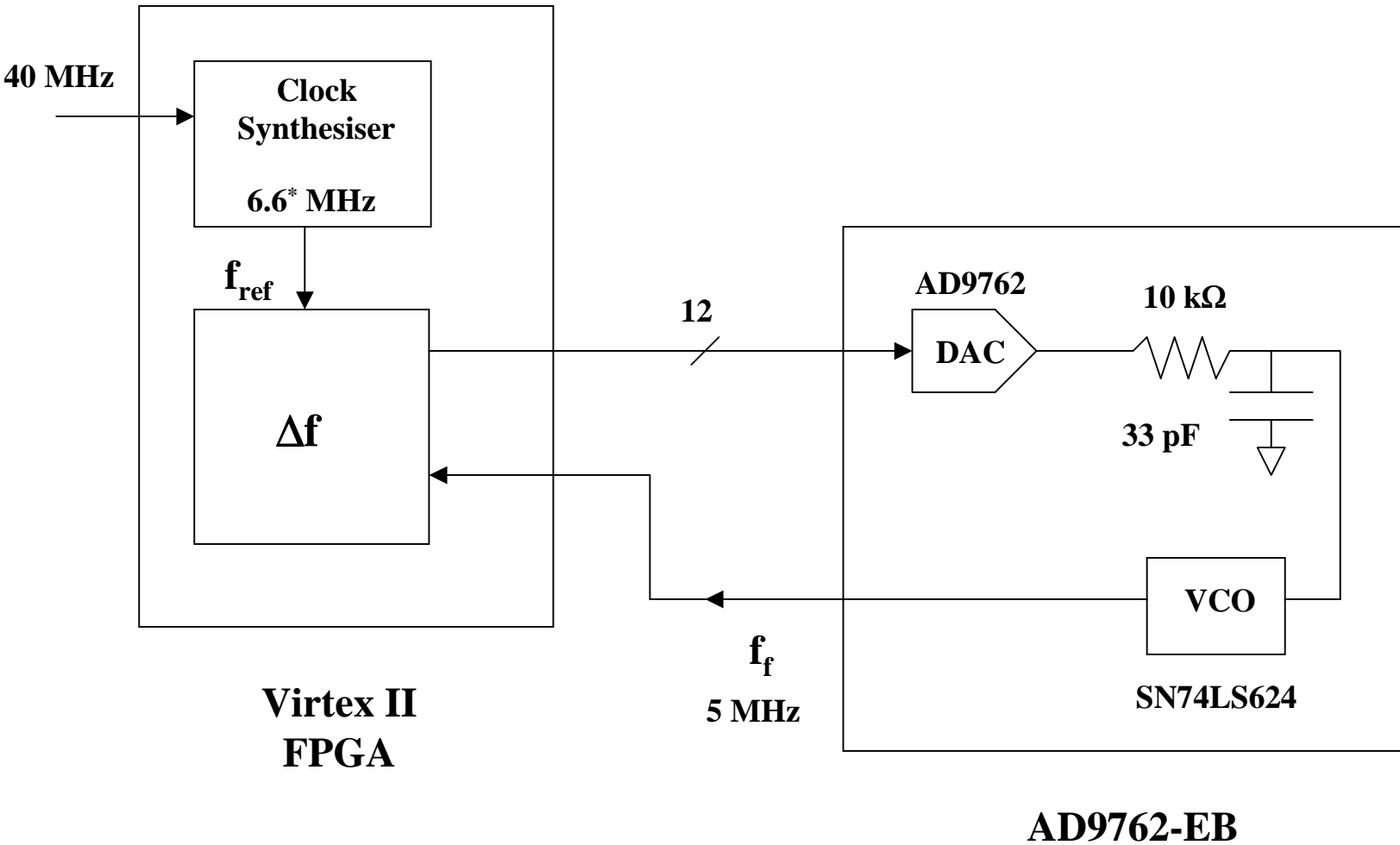
$$H(s) = \frac{k}{k_1 + sT} = \frac{k_2}{s + k_3}$$

$$\hookrightarrow h(t) = k_2 e^{-k_3 t} = \frac{k}{T} e^{-\frac{1+k}{T} t}$$

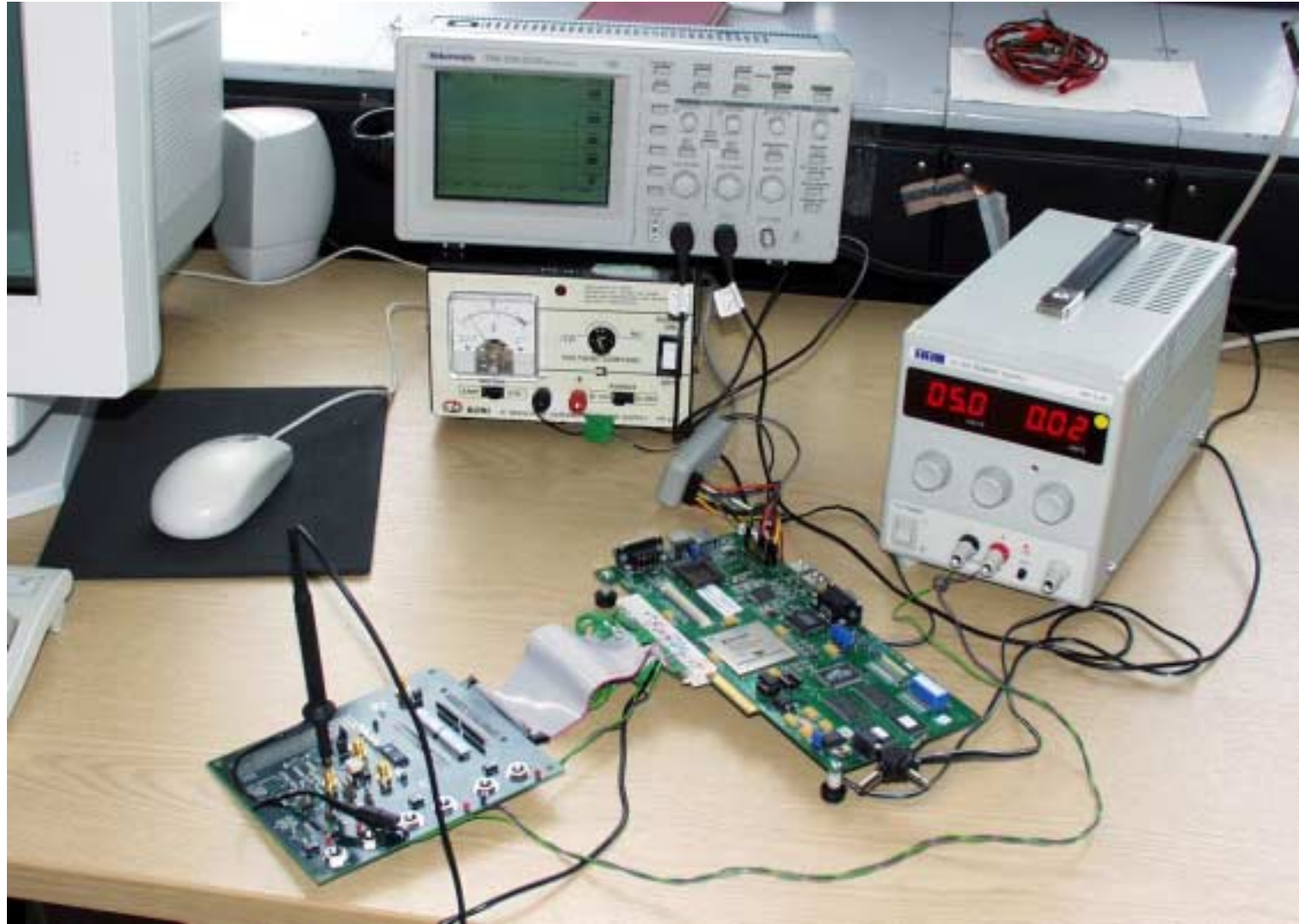
Hardware: Open Loop Test Set-up



Hardware: Closed Loop Test Set-up

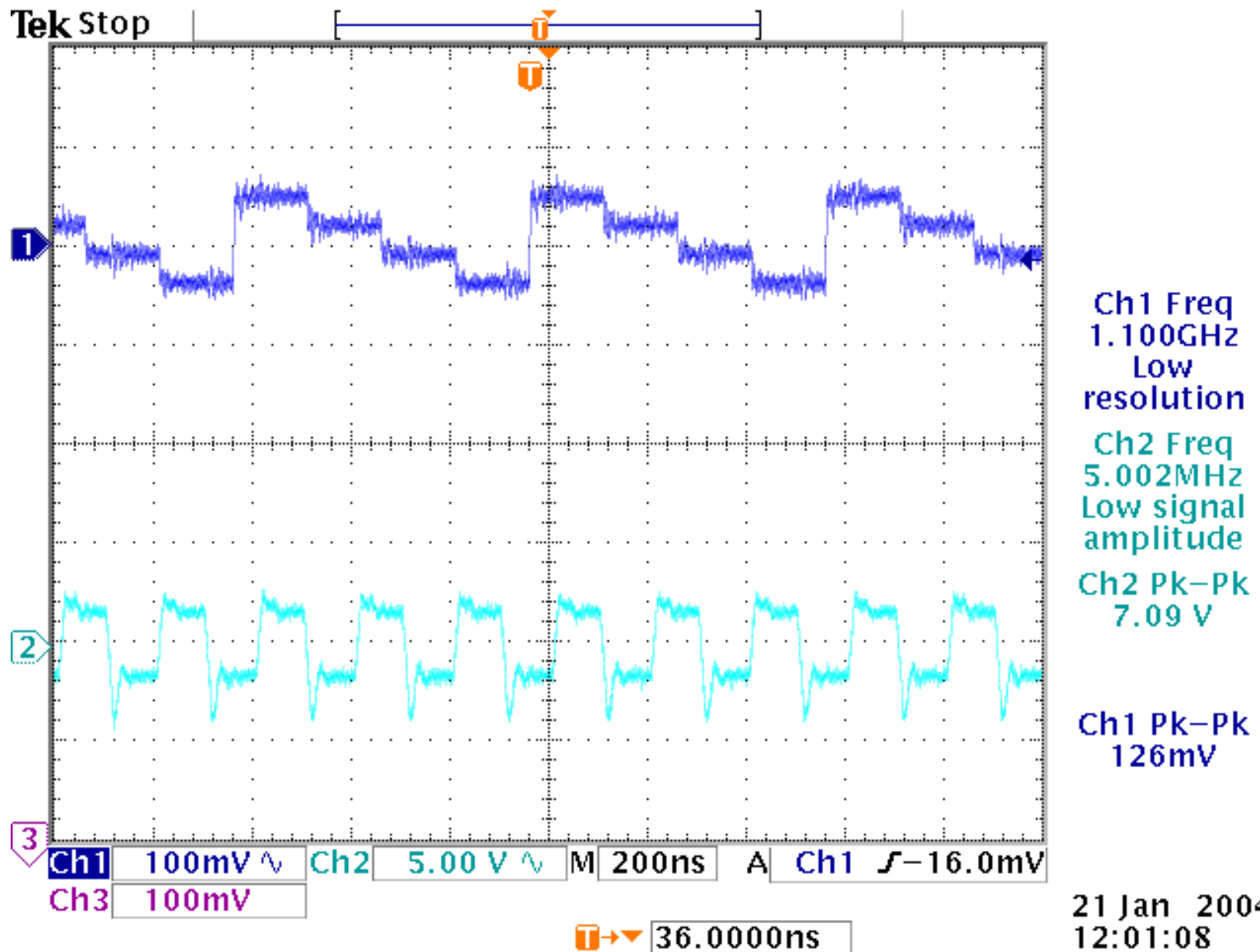


Interim Hardware Set-Up



12-bit DAC development board donated by Analog Devices

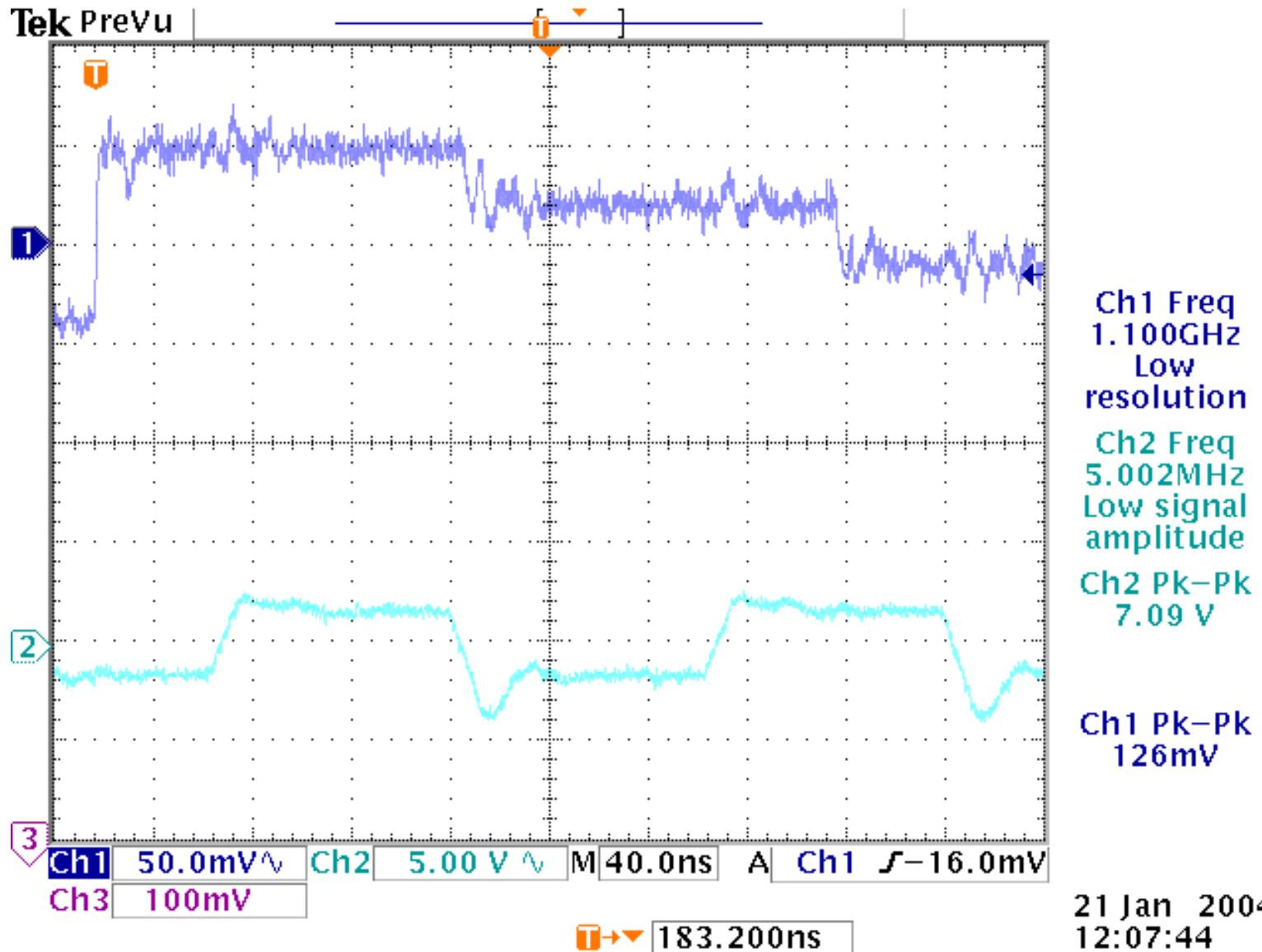
DAC Output for 4:3 Ratio



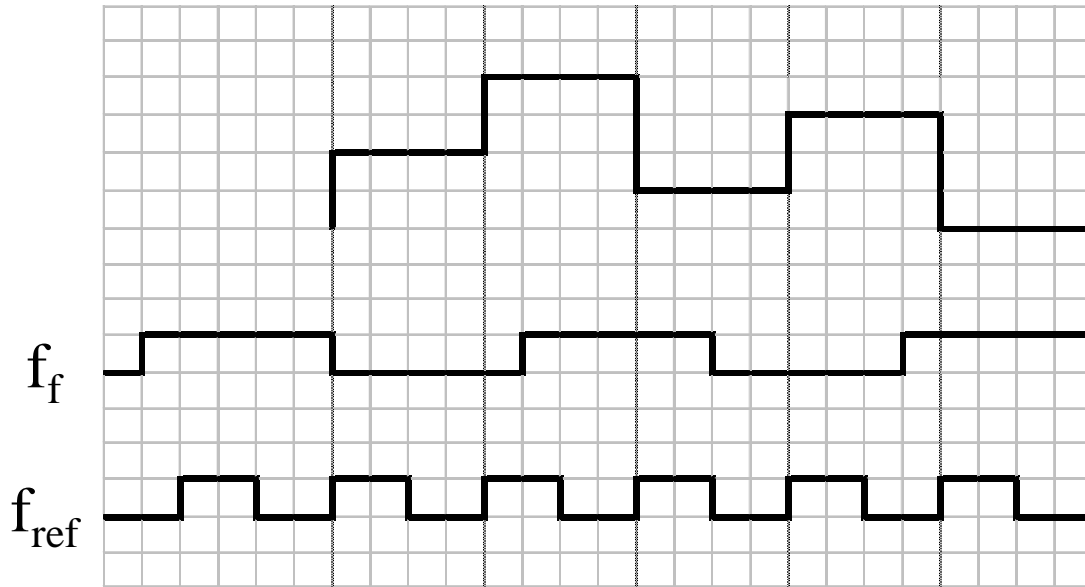
Selected Parameters of the SN74LS624 VCO

Output Frequency (f_o) Range	20MHz
Control Voltage (V_C) Range	5V
Estimated Conversion Gain (K_o)	2MHz/V
Output Signal Voltage	TTL

DAC Output for 4:3 Ratio (Detailed View)



Spurious Waveform for Ratio 2:5



BASE 2	BASE 5	Y/N
0	1	
1	2	Y
0	3	
1	4	N
0	0	
1	1	Y
0	2	
1	3	N
0	4	
1	0	N
0	1	
1	2	Y
0	3	
1	4	N
0	0	
1	1	Y
0	2	
1	3	N
0	4	
1	0	N

Summary

- Hybrid Synthesiser
- Mathematical theory for loop transfer function
- Mathematical analysis to be further developed
- Spurious noise signals analysis
- Simulation under further development
- Hardware open loop and closed loop tests completed
- Work under progress: RF board design