LABORATOIRE D'ELECTRONIQUE GENERALE - LEG

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Ecole Polytechnique Fédérale Lausanne (EPFL)

- one of the two Swiss federal engineering schools
- more than 6’000 students, more than 2’000 staff, more than 200 professors
- excellence in education and research in many engineering fields with traditional collaborations with world wide industry
- annual budget > 500M CHF
- for more info: www.epfl.ch

INSTITUT OF MICROELECTRONICS AND MICROSYSTEMS

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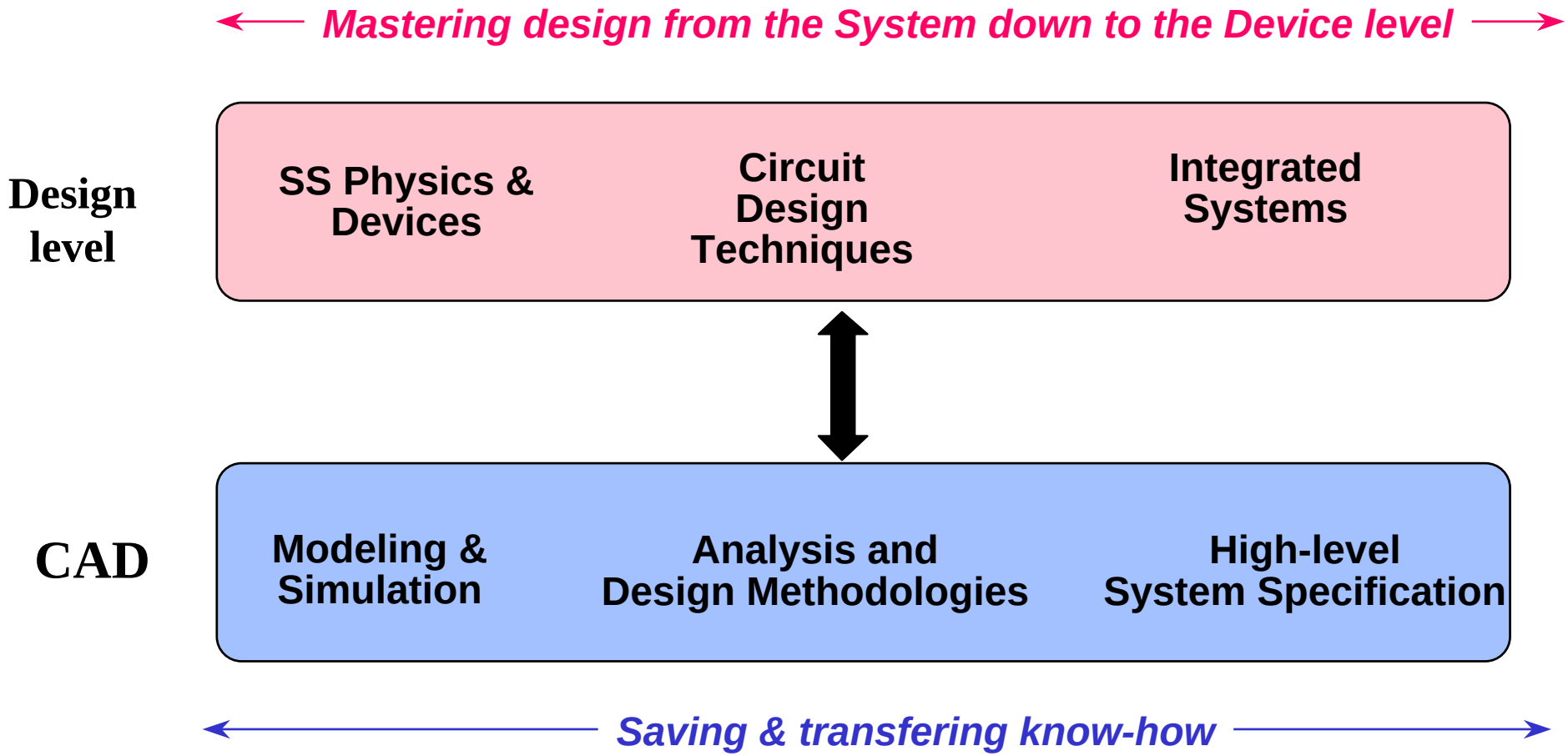
LEG RESEARCH : Overall Strategy



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RESEARCH : Overview

Analog and mixed-signal circuit design techniques

Device-level engineering:
physics and technology – basic design techniques

Advanced silicon technology

CAD and device modeling

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RESEARCH

DOMAIN 1: Analog and mixed-signal circuit design techniques

Low-power low-voltage & high-performance CMOS for signal processing

- A/D converters
- Power management
- Gm-C and Log-domain continuous-time filters

RF circuit design for telecom applications

- Short-range wireless UHF data transmission (super-regenerative, Direct-conversion, active or passive back-scattering techniques)
- Linear PA with improved power efficiency

High-voltage and high-temperature circuit design

- HV and HT SOI

Integrated microsystems (IC + MEMS)

- Integrated interfaces for Hall-effect sensors
- RF MEMS for telecom applications
- Integrated opto-electronic signal processing systems

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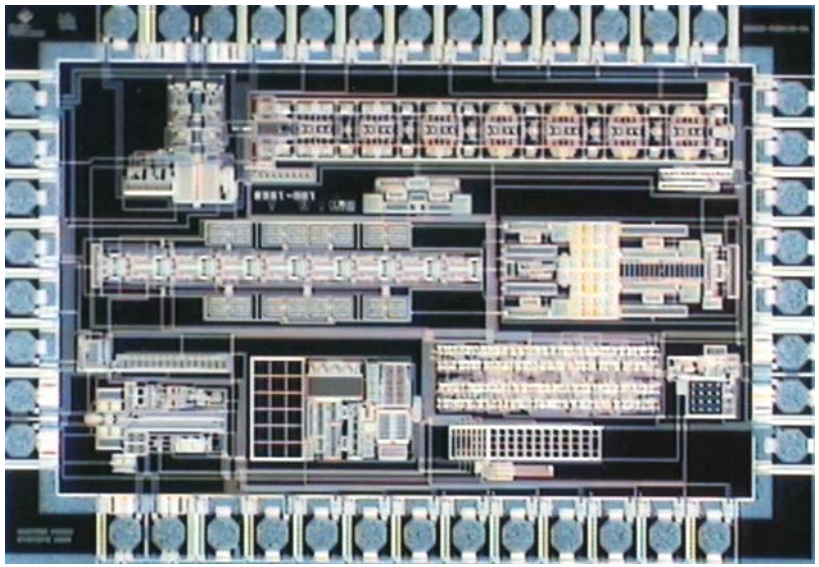
A Low-Power 1 GHz BiCMOS Super-Regenerative Transceiver for short range wireless applications

LEG: Coordinator of the European IST project SUPREGE
Partners: LEG, Logitech SA, MEAD SA, Transval SA

AMS BiCMOS 0.8um, Area = 5mm2
Minimum operating voltage: 2.4 V
Supply current in RX mode: 1.5 mA
Supply current in TX mode: 6 mA
Operating freq.: 300 to 1500 MHz
Sensitivity: - 105 dBm
(at 200 kHz quench, 10 kbit/s, 1/1000 BER)
Selectivity: 150 kHz
(At – 5 dB, 200 kHz quench)
Maximum data rate: 150 kbit/s
(At 500 kHz quench)
Ouput power of the transmitter: 0 dBm



Ref: JSSCC, July 2001, pp. 1025-1031

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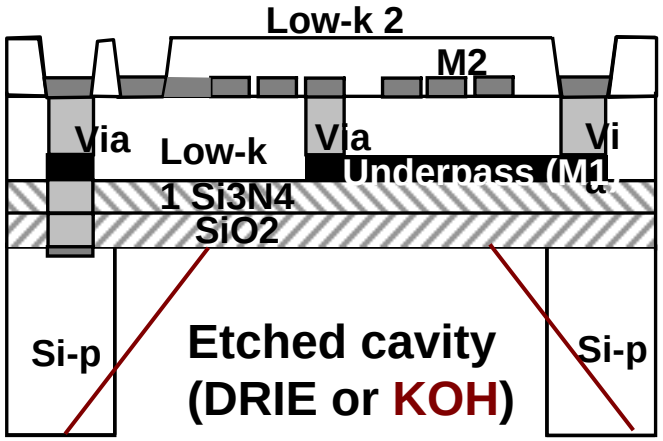
Integrated microsystems (IC + MEMS)

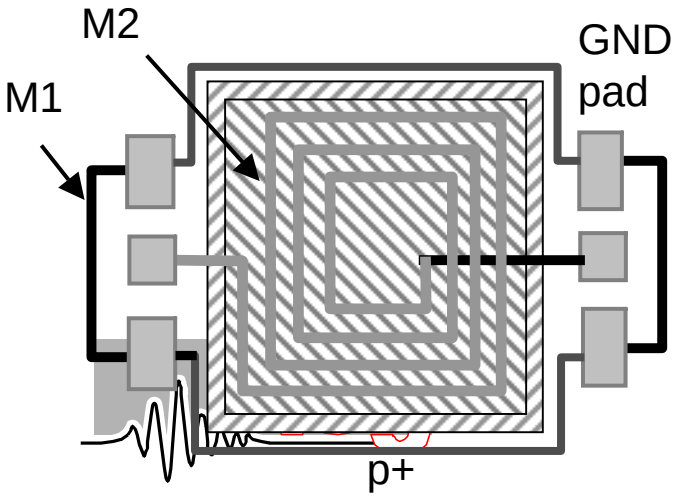
RF MEMS for telecom and airborne applications

Horizontal plane **High-Q inductors**



European IST project WIDE RF

Suspended inductor:
reduction of substrate loss



RESEARCH

Device-level engineering:
physics and technology + related design techniques

Fully-depleted CMOS-SOI Technology and related circuit design techniques

High-Voltage CMOS devices and circuits in standard CMOS technologies

Ultra-deep submicron and quantum devices

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RESEARCH

CAD and device modeling

MOS transistor modeling

Substrate noise analysis and modeling

HV MOS transistor modeling

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Noise coupling mechanisms in Mixed-Signal ICs

Strategies:

- Use of multiple pins assignment for power supplies/ground.
- Splitting supply lines and terminals of noisy and sensitive blocks.
- Installing guard ring with dedicated on-chip ground.
- Increasing the distances between noisy and sensitive circuits.
- Using special package like flip-chip.
- Adopting differential topology for analog design.
- Using silicon-on-insulator or triple-well technology.

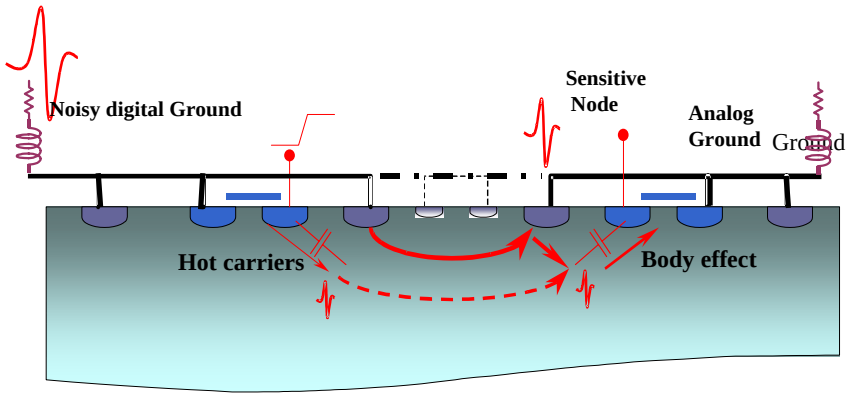

Fig .1 Noise coupling mechanisms in Mixed-Signal ICs

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HSpeedEx: A High-Speed Extractor for Substrate Noise Analysis

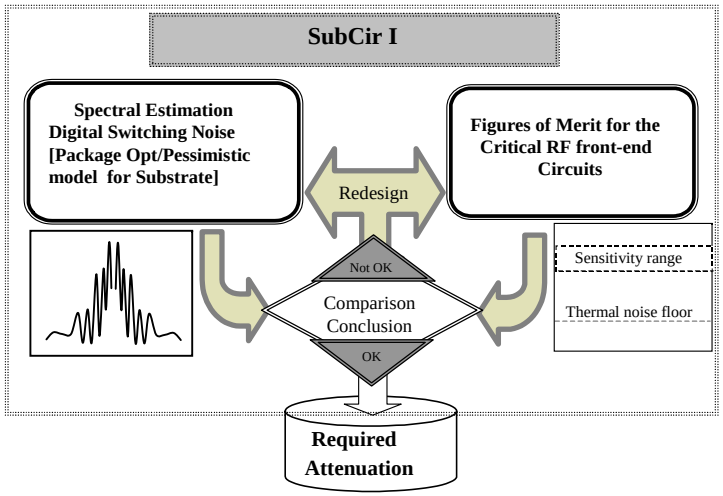

Fig.2 Flow diagram of SubCirI methodology

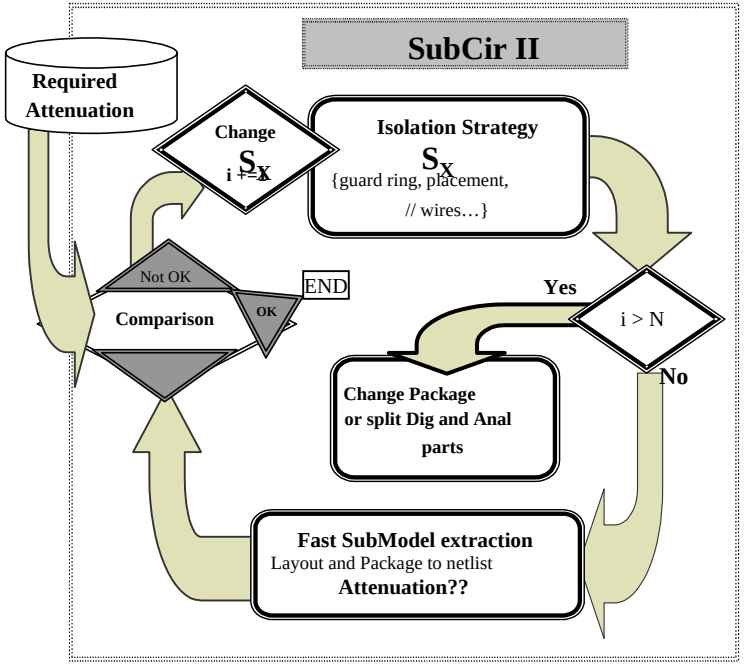

Fig.3 Flow diagram of SubCirII methodology

Individual performances
of the sensitive parts of the IC

Determination of the best isolation strategy

IEEE/ACM Int. Conference On Computer-Aided Design, 2002, pp. 309-316
Design Automation Conference, 2002, pp. 767 –770.

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RESEARCH CONTRACTS

EUROPEAN PROJECTS CURRENTLY RUNNING

IST-MUMOR
IST-WIDE RF
IST-MIMOSA
IST-NANOTIMER
IST-ROBUSPIC
IST-AMICOM

SWISS-GOVERNMENT PROJECTS CURRENTLY RUNNING

3 CTI Projects
1 National Science Foundation project

INDUSTRY-FUNDED PROJECTS

5 PROJECTS RUNNING

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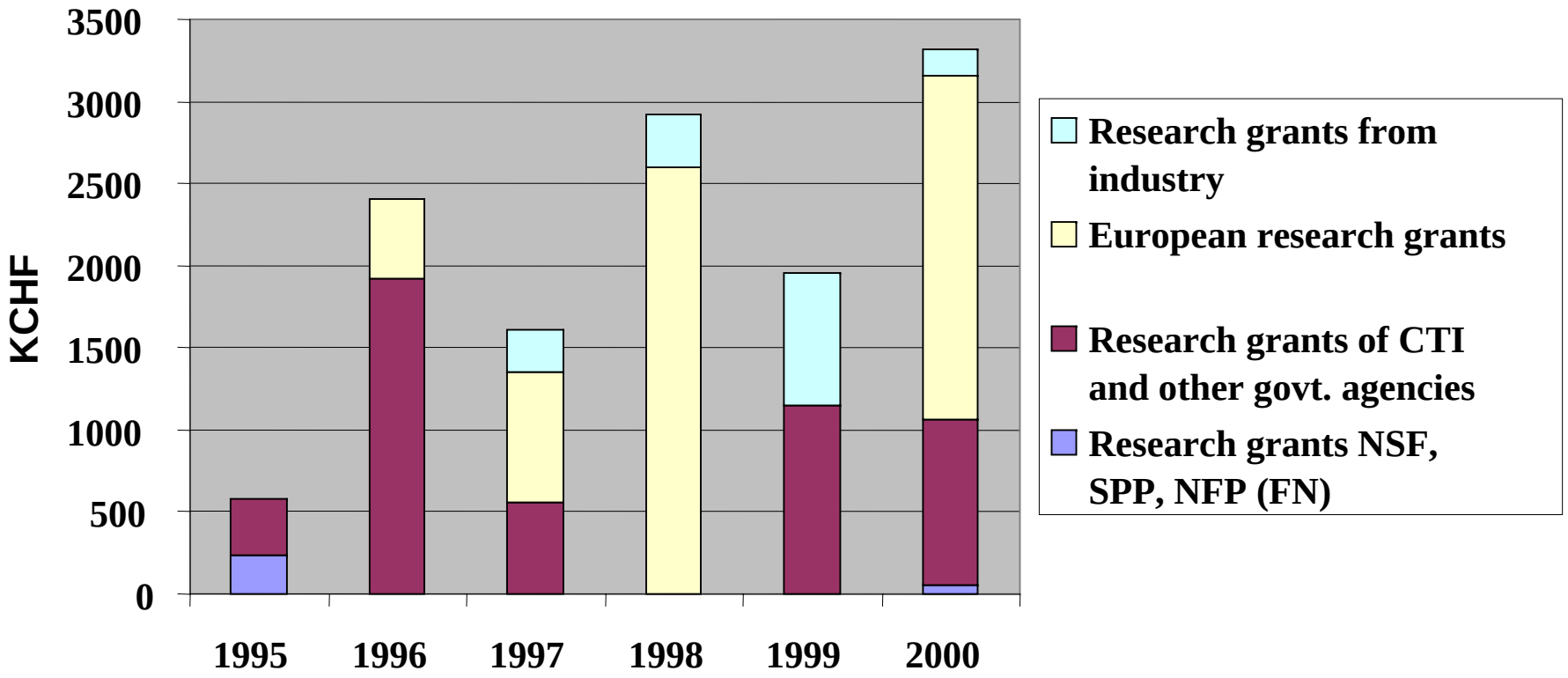
RESEARCH CONTRACTS

FUNDING FROM EXTERNAL SOURCES



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START-UP COMPANIES

MEAD S.A. (now Microchip)

Snaketech (now bought by Cadence)

Smart Silicon Systems (S3)

Wavemind

POSTGRADUATE COURSES IN IC DESIGN

Target audience

Engineers from industry (in R&D)

Strategy

Quality

- **international experts**
- **very-high level**
- **written support**

Intensive training in a short time (1 to 3 weeks)
Professional organization
Self-supported

Results

20% Switzerland - 80% Foreigners
>4'000 participants in 14 years
49 countries
>90% industry
Worldwide visibility and reputation

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POSTGRADUATE COURSES IN IC DESIGN

Courses	Number of Participants per year						
	00	**99**	**98**	**97**	**96**	**95**	**Total**
RF IC Design for Wireless Communications	78	86	71	67	73	90	387
Low-Voltage, Low-Power Analog (CMOS) IC Design	56	88	92	52	59	77	368
PLLs, Oscillators and Frequency Synthesizers	57	47	72				119
CMOS On-Chip Analog Filters		16					16
High-Speed Data Converters		49	54				103
Transistor-Level Analog IC Design		66					66
Oversampled Delta-Sigma Data Converters	65		39	57			96
Deep Submicron: Modeling and Simulation			30				30
Modeling and Simulation of MOS Analog Ics				46			46
Special Techniques for High-Performance Op-Amp IC Design				36			36
Advanced CMOS & BiCMOS IC Design		188	181	180	114	134	797
Totals	565	540	539	438	246	301	2064

PERSPECTIVES

Advanced/new devices : physics, technology, modeling

- HV-submicron
- SOI
- Quantum devices
- Substrate coupling
- Advanced Si technology

Circuit design techniques

"Pushing the limits"

- Ultra-deep submicron analog design techniques
- Interface circuits for quantum devices (SET, etc.)
- GHz-range low-power RF
- RF-MEMS

Trans-disciplinary applications (bio-medical and others)

Postgraduate courses ("summer courses")

International cooperation

Shortage of skilled designers : a major problem

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