ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

VCO for reconfigurable multi-mode Systems (GSM, UMTS, HSDPA TDD and FDD)

Adil Koukab

Swiss Federal Institute of Technology (EPFL) / LEG

Outline

- General requirements
- VCO specifications and topology
- Design Methodology
- Characterization of passive components
- VCO: Architecture and Design Optimization
- VCO: Layout and integration
- Substrate noise analysis
- Conclusion

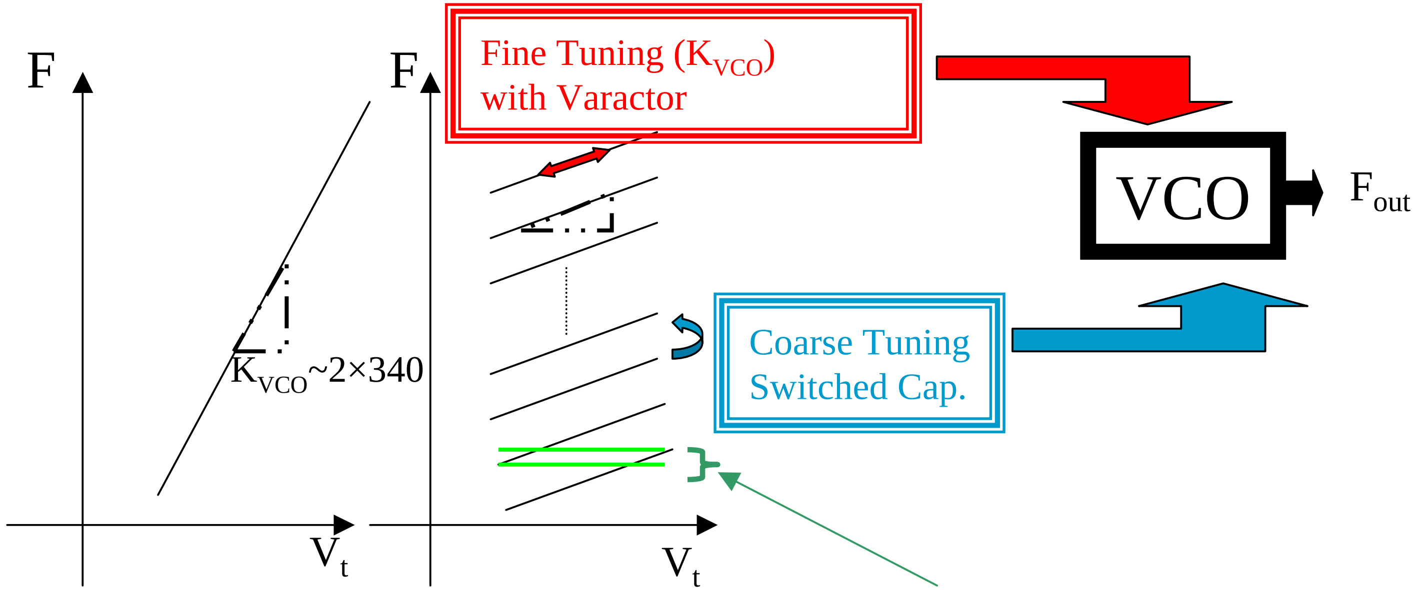
General requirements

- Design oscillator for low phase noise, low power dissipation, and low sensitivity to noise coupling
- Apply a frequency variation technique such that:
  - A wide tuning range is achieved;
  - Loop gain remains relatively constant;
  - Voltage swing remain relatively constant;
  - Frequency control path is immune to noise;
  - Sensitivity to noise in Frequency control path is low;

VCO Specifications and Topology

- multi-mode [3800-4340MHz] :
- Process and Temperature : variation~ 10-20%
- Tuning Voltage [0.5-2.1V]
  - **K_{VCO} ~ 2 x 340 MHz/V**

- Low sensitivity to DeltaV$_t$
  - K_{VCOMax} = 200 MHz/V if 0.8V<Vt<2.2 and Dig.Ctr: 4bit



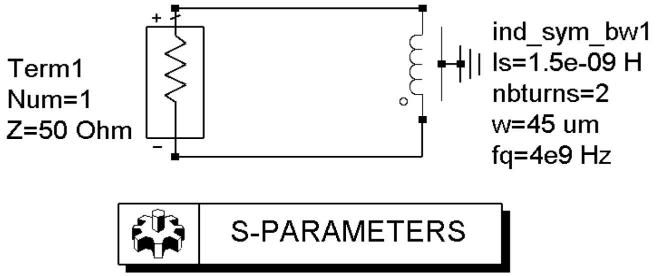
Overlap ~ statistic variation of each SC

Design Methodology

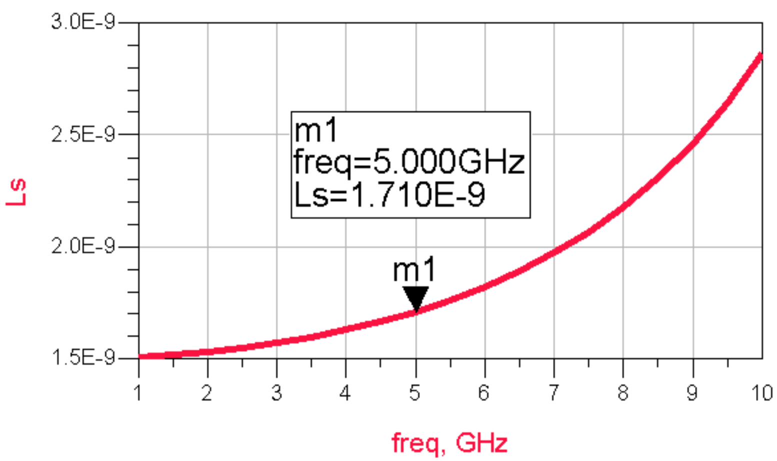
- All available passive components were characterized:
  - Objective: Design of a tank with optimal Q and low parasitic capacitance
- Various VCO architectures were designed (without SCA).
  - A comparative study (phase noise/ power dissipation/ tuning range capabilities).
- Optimization of the selected architecture without SCA
  - to meet TX and RX specifications
- Various SCA were designed
- Optimization of the VCO with SCA

Characterization of passive Components

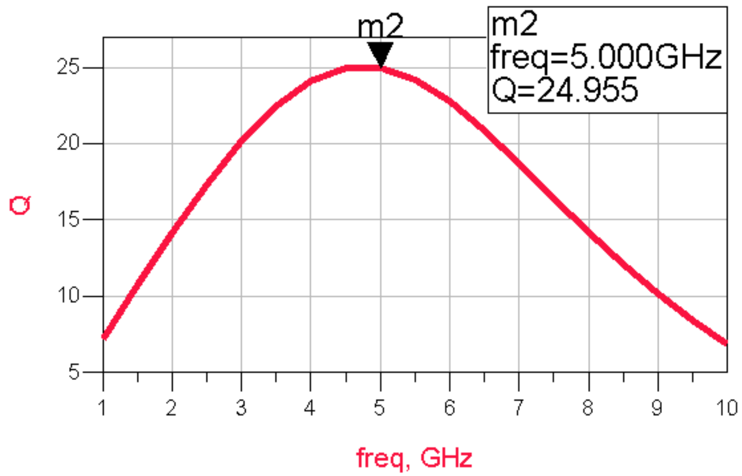
Inductors



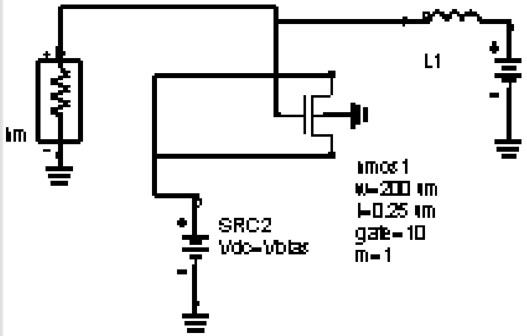
Eqn Ls=imag(Z(1,1))/(2*pi*freq)



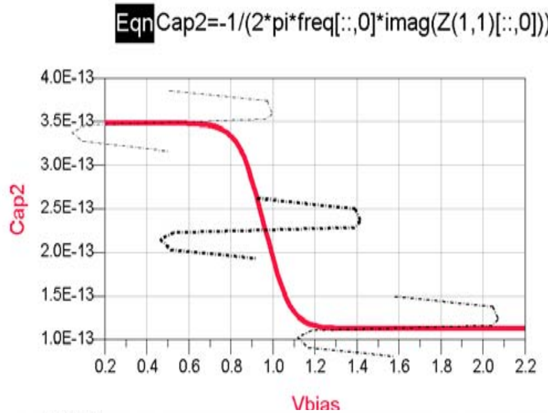
Eqn Q=imag(Z(1,1))/real(Z(1,1))



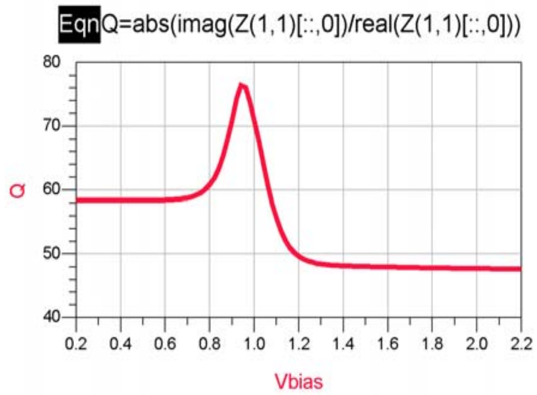
Varactors



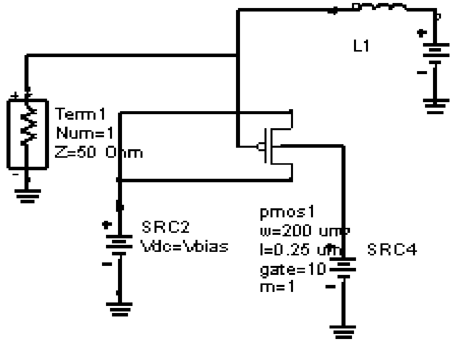
L1
nmos1
w=200 um
l=0.25 um
gate=10
m=1
SRC2
Vdc=Vbias



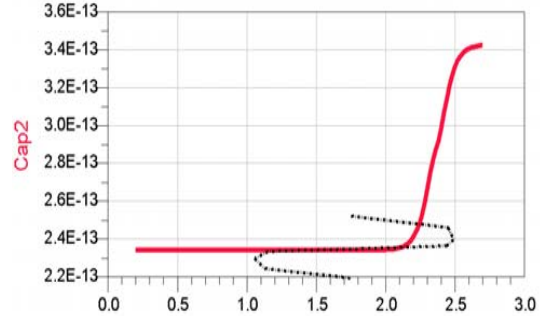
Eqn Cap2=-1/(2*pi*freq[::,0]*imag(Z(1,1)[::,0]))
Cap2
Vbias



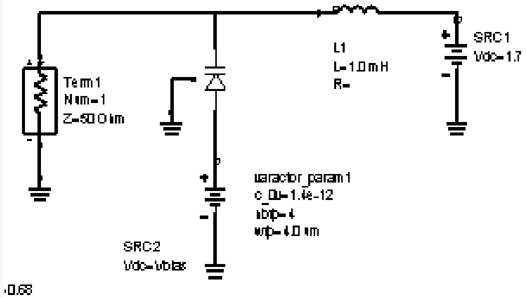
Eqn Q=abs(imag(Z(1,1)[::,0])/real(Z(1,1)[::,0]))
Q
Vbias



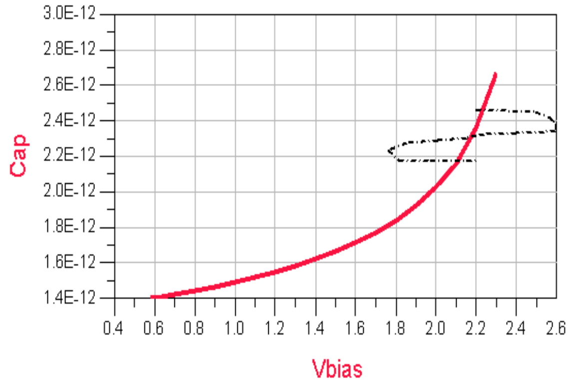
L1
Term1
Num=1
Z=50 Ohm
SRC2
Vdc=Vbias
pmos1
w=200 um
l=0.25 um
gate=10
m=1
SRC4



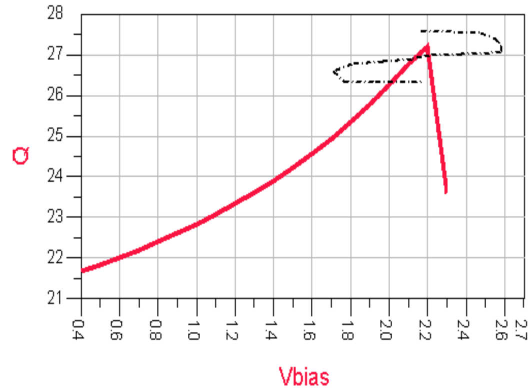
Cap2



SRC1
Vdc=1.7
L1
Term1
SRC2

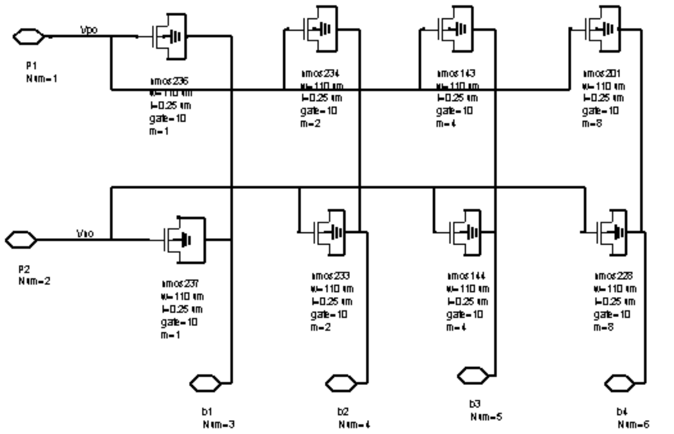


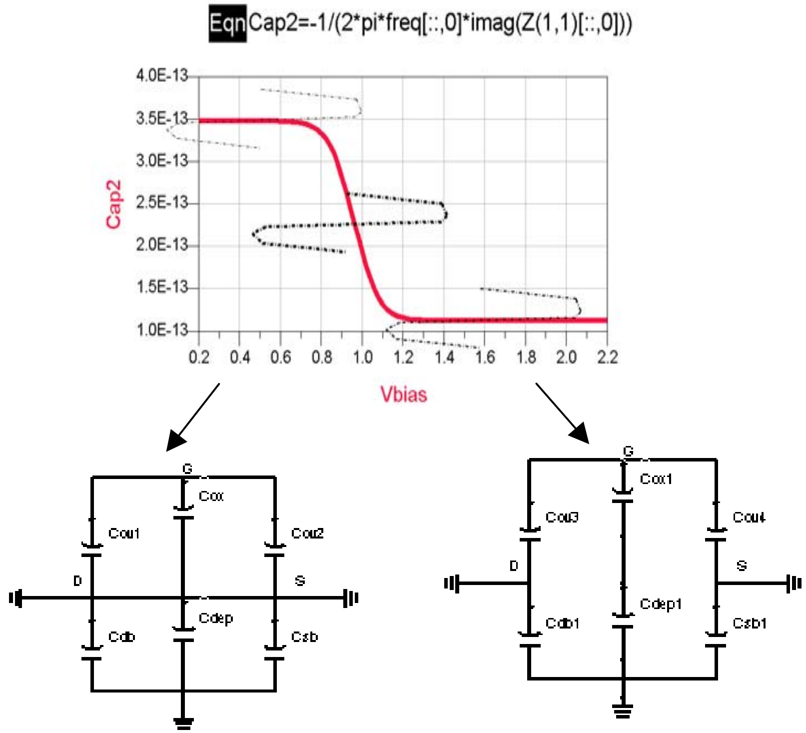
Cap
Vbias



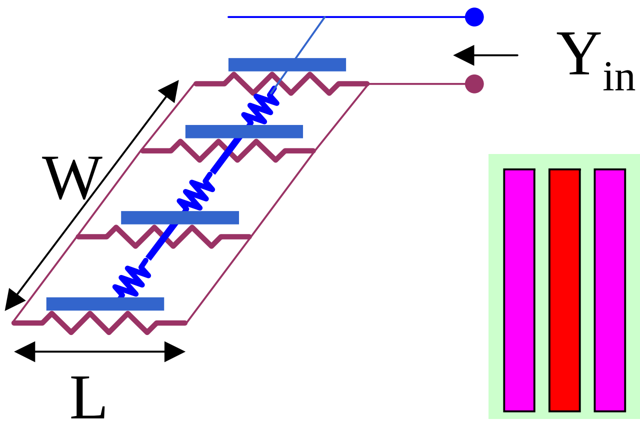
Q
Vbias

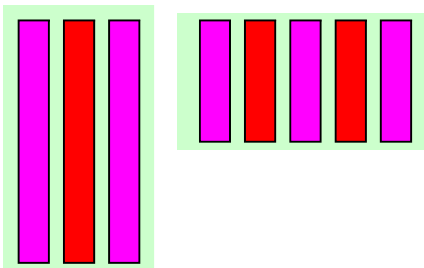
Switchable -capacitor-array (SCA)

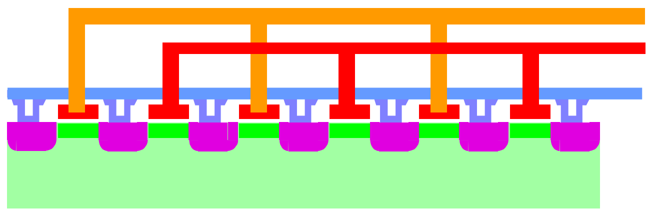




$$Q \approx \frac{12}{\omega C'_{ox}\left(R_{sh}L^2 + R_{poly}W^2\right)}$$



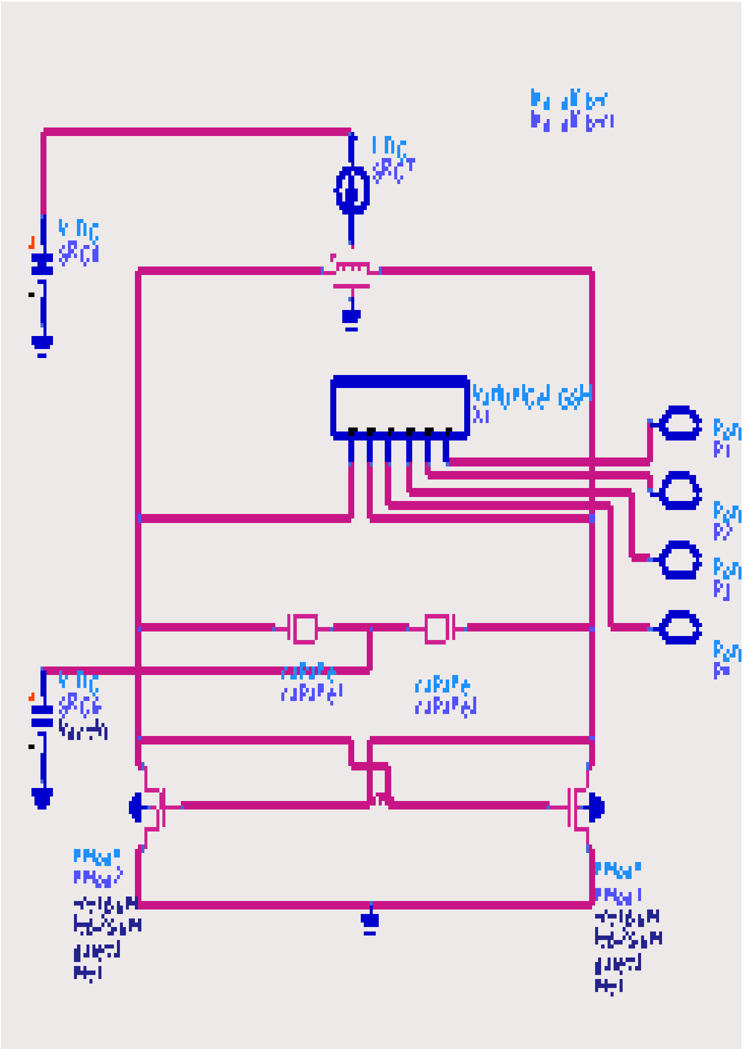


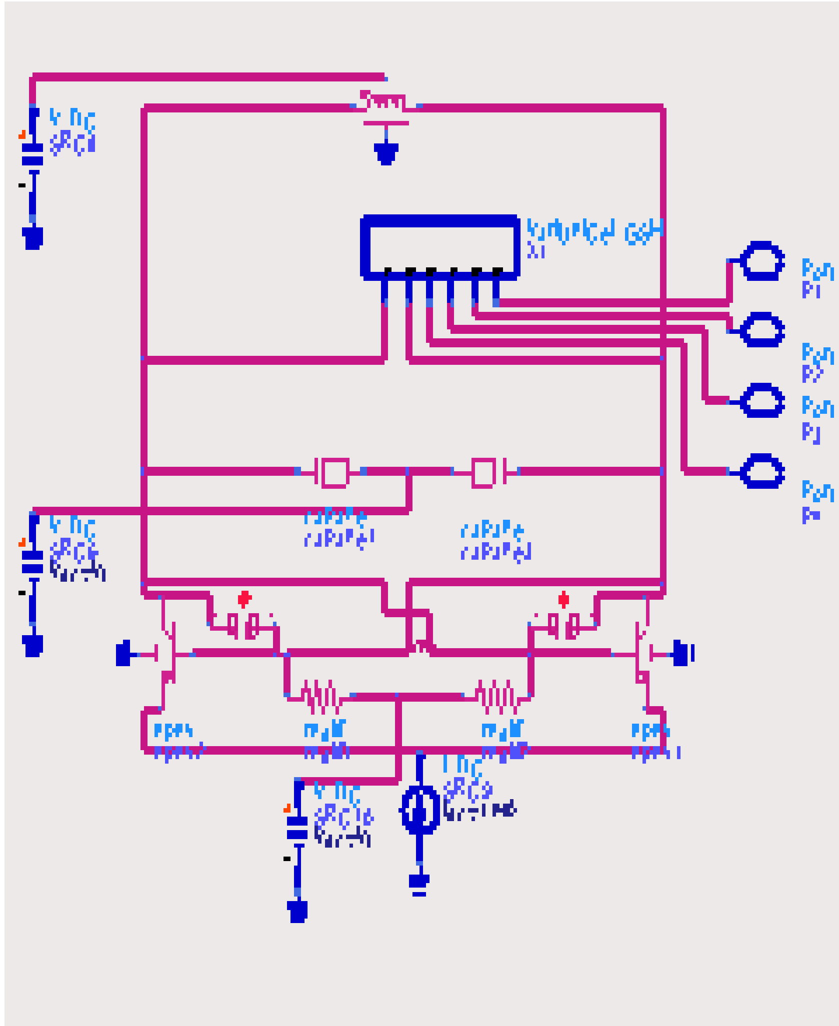


VCO: Architectures, Design and optimization

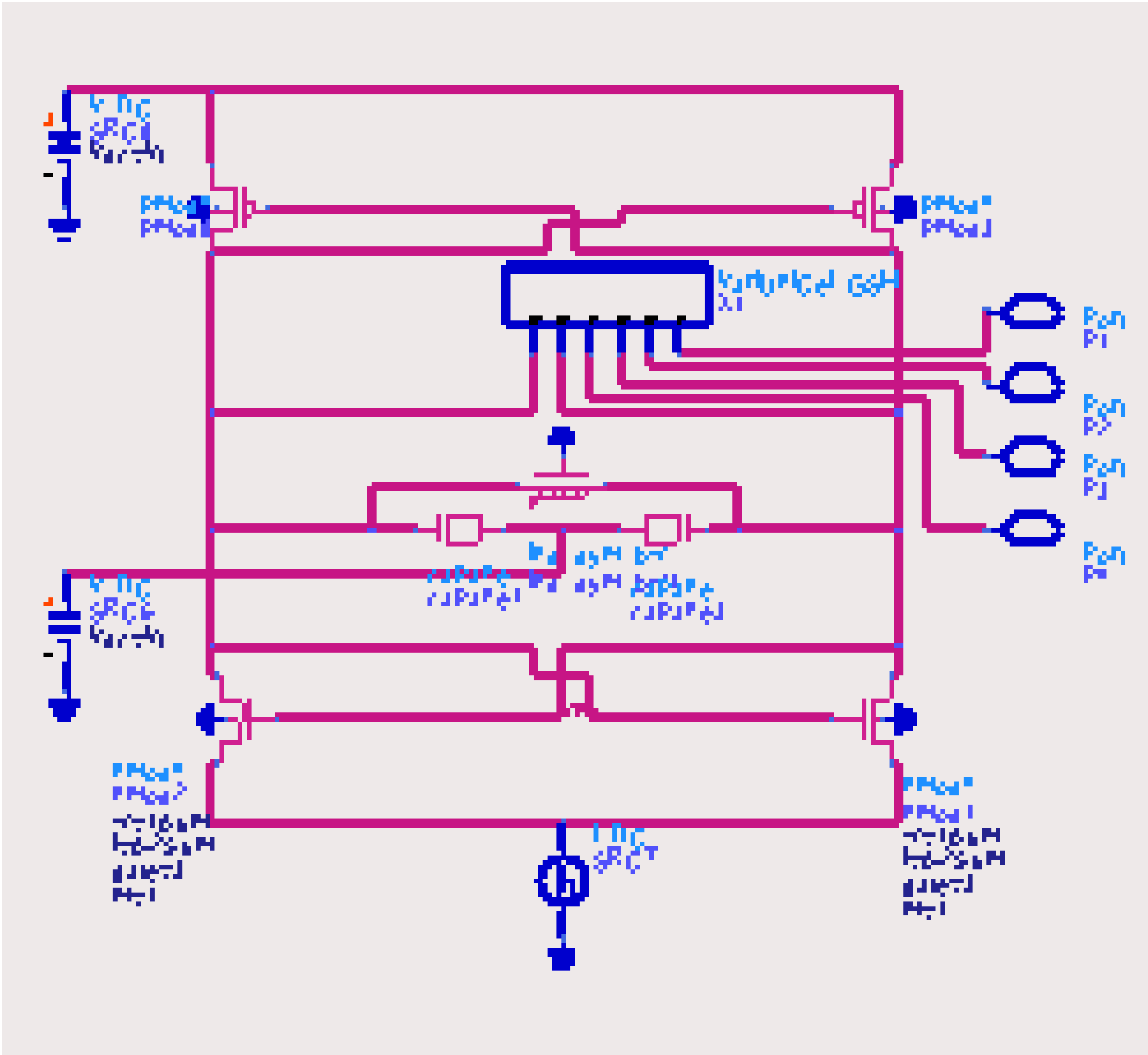
- nMOS-only VCO
- pMOS-only VCO
- Complementary nMOS-pMOS VCO
- Bipolar VCO

Designed VCOs

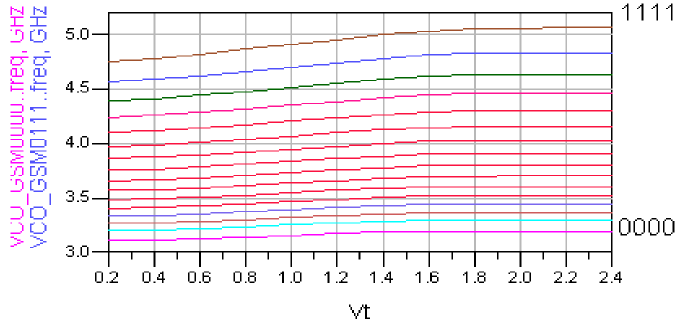


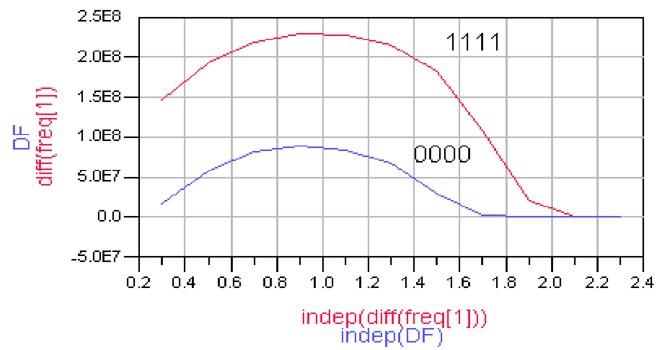


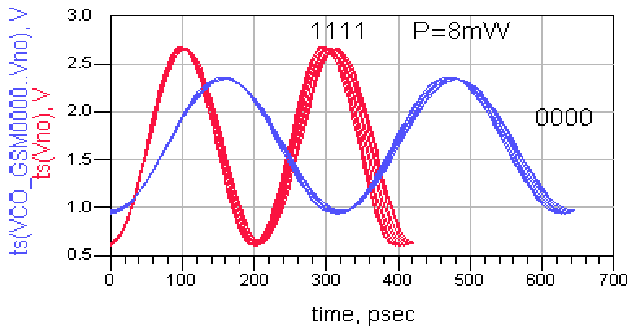
Selected VCO

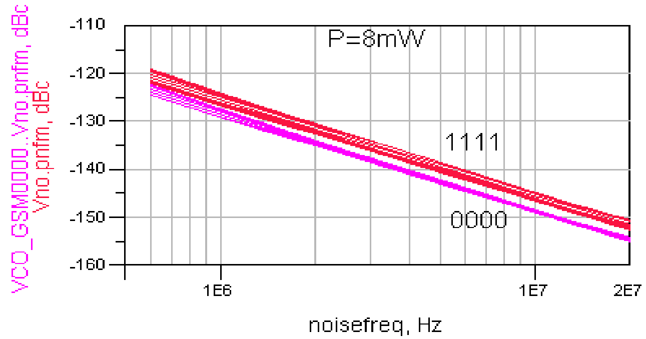


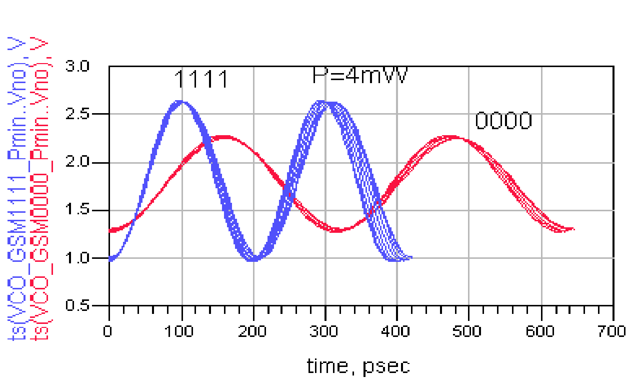
Performances of the Selected VCO

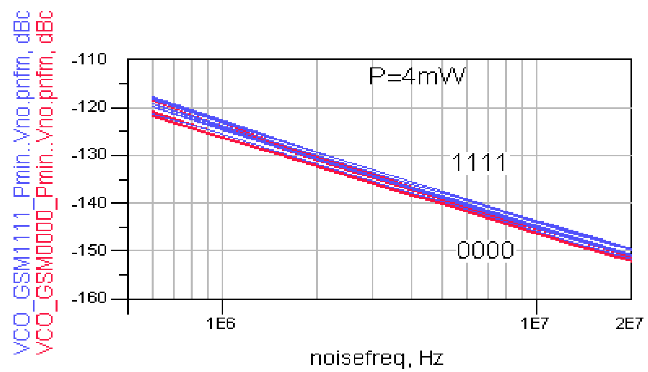








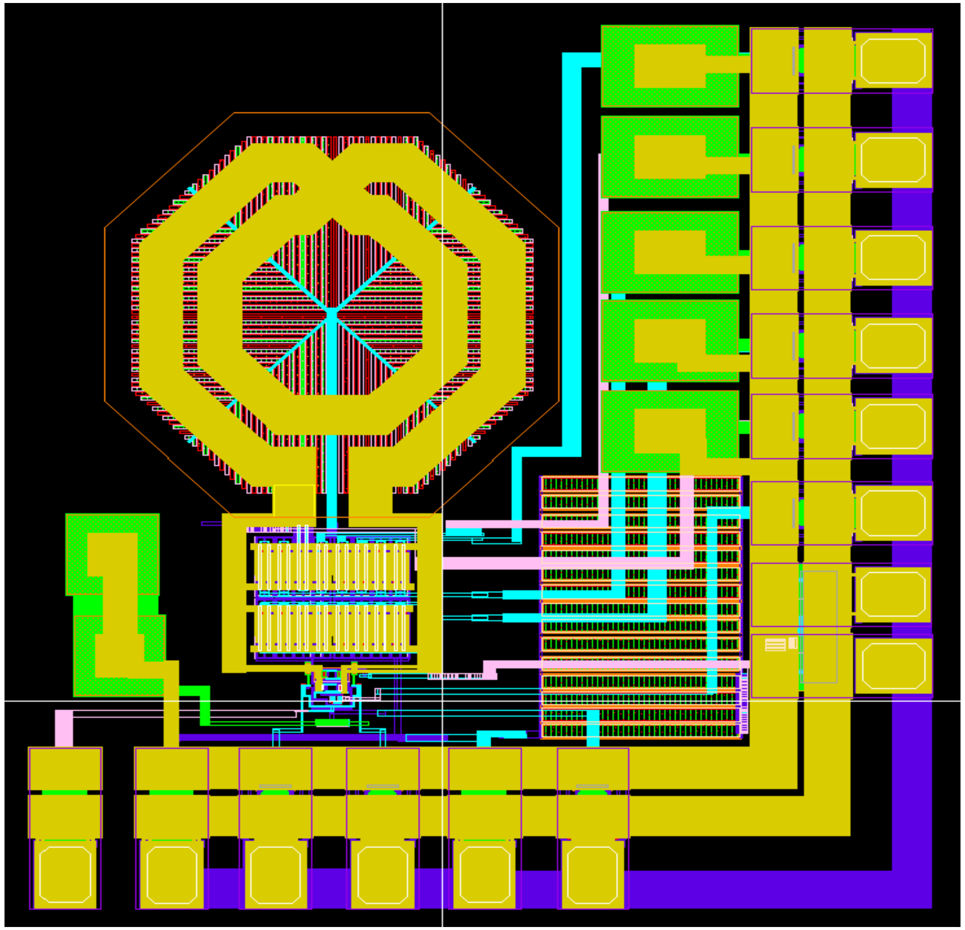


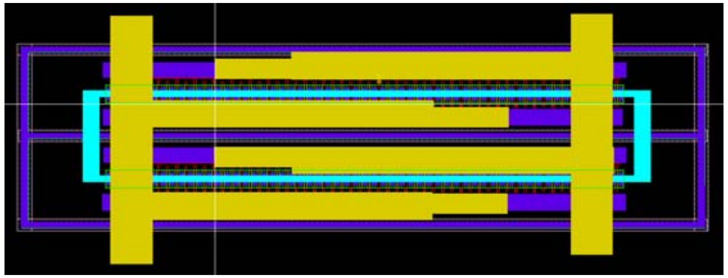


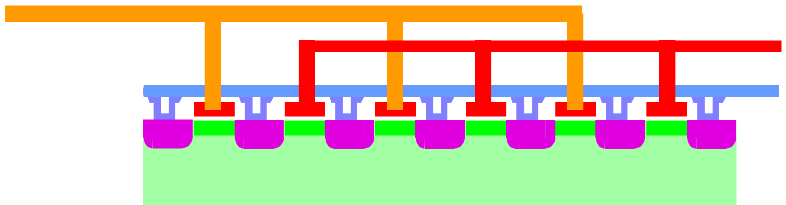
Comparative study

		VCOI(nMOS)	VCOII(nMOS)	VCOIII(nMOS/pMOS)
F_{Max} F_{Min}		4.45GHz 3.71GHz	4.35 3.8	5GHz 3.1GHz
K_{VCOMax} K_{VCOMin}		800MHz 167MHz	170MHz 43MHz	228MHz 89MHz
PhaseNoise (dBc/Hz)	600KHz	X	X	[-124 to -119]
	3MHz	-128	-131.9	[-139 to -135]
	5MHz	-132	-135.97	[-143 to -139]
	10MHz	-138	-141.95	[-149 to -145]
	12.5MHz	-140	-143	[-151 to -146]
	15MHz	-142	-145	X
	20MHz	-144	-147.9	[-155 to -150.6]
	80MHz	-157	-160	X
Power consumption (without buffers)		6mW	6mW	4mW to 8mW
Digital Control		none	3 bit	4 bit

Layout and integration







Conclusion

- The Design of the VCO for reconfigurable multi-mode systems is a challenging problem.
- The advantages and the limitations of the topology with a switchable-capacitor-array SCA according to the multi-mode system specifications and the technology used, are identified .
- Several investigations of the various solutions that enable to fits our requirements are studied. The focus was on :
  - The design of the Varactor and of the SCA with High quality factor and low parasitic capacitances.
  - Design various VCO topologies
  - A comparative study (phase noise/ power dissipation/ tuning range capabilities).
- The circuit was integrated on BiCMOS7-SiGe technology of ST