Workshop MUMOR Project
25-26 / 02 / 2004
EPFL, Lausanne

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Outline

- The topic of the presentation is to give an overview of the WP4 activities about the baseband demonstrator.
- Part 1 : recall of objectives and the work to achieve,
- Part 2 : generalities about reconfigurability and requirements,
- Part 3 : architecture
  - Presentation of the general architecture of the demonstrator
  - Some designed blocks
    - Channel estimator
    - Rake combiner
    - Cell Searcher
  - Synthesis result and conclusion
- Future work

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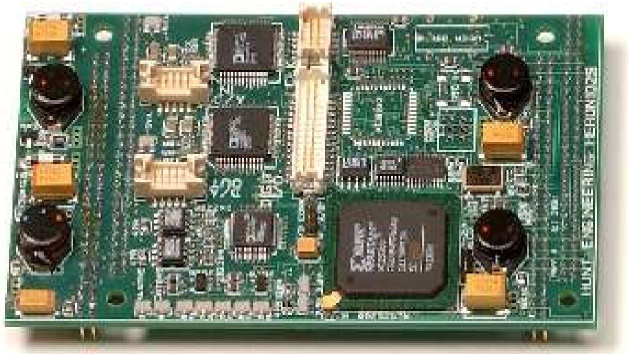
- Study the physical layer architecture for the three modes of UMTS transmission (TDD, FDD, HSDPA/FDD), and merged them into a reconfigurable architecture.
- Get a real-time demonstration based the results of the HW/SW partitioning.
- Design a FPGA ensuring a natural translation into an ASIC
  - meanwhile, use the newer FPGA resources and avoid the floating point modules.
- Implement the DSP code compliant with the TI tools.
- Integrate the HW blocks on the platform
- Validate the selected architecture of blocks, and perform a global demonstration through BER and BLER measurements on PC processing.



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Reconfigurability / General concept

- Goal : be able to process the three mode without hardware redundancy.

- Reuse of resource :
  - identify the operators that can be shared in a module to reduce hardware. When a mode is not running, switch off the operators in order to reduce the power consumption.
  - Ex : accumulators, arithmetic functions …

- Reconfigurability :
  - Multiplexing
  - Synchronisation signals : regarding the mode, a reconfigurable mode generate different synchronisation signals i.e. different length of pulse, different ways of sequencement… the hardware remains the same,
  - Loading of DSP assembling code from FPGA, but this task is not real-time.

- Target Platform provided by Hunt Engineering

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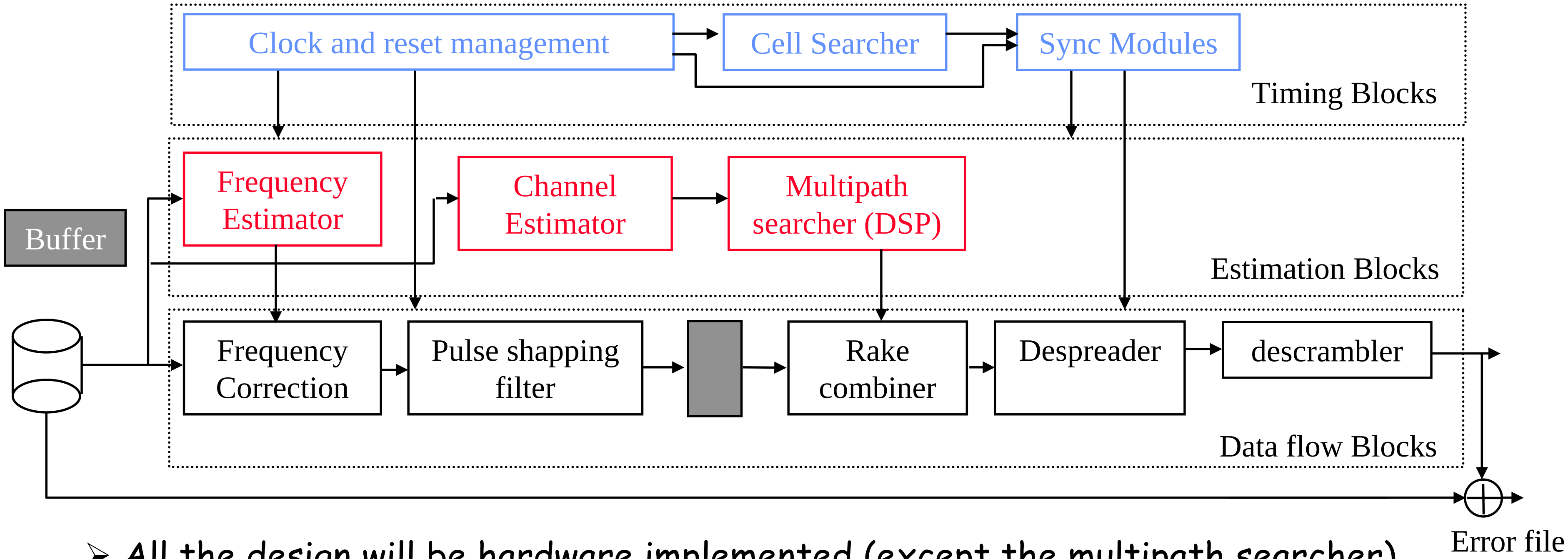
Overview of the physical layer architecture

- Design of the physical layer embedded in the mobile for the downlink decoding.



- All the design will be hardware implemented (except the multipath searcher).
- Cell Searcher will not be connected with the other modules.

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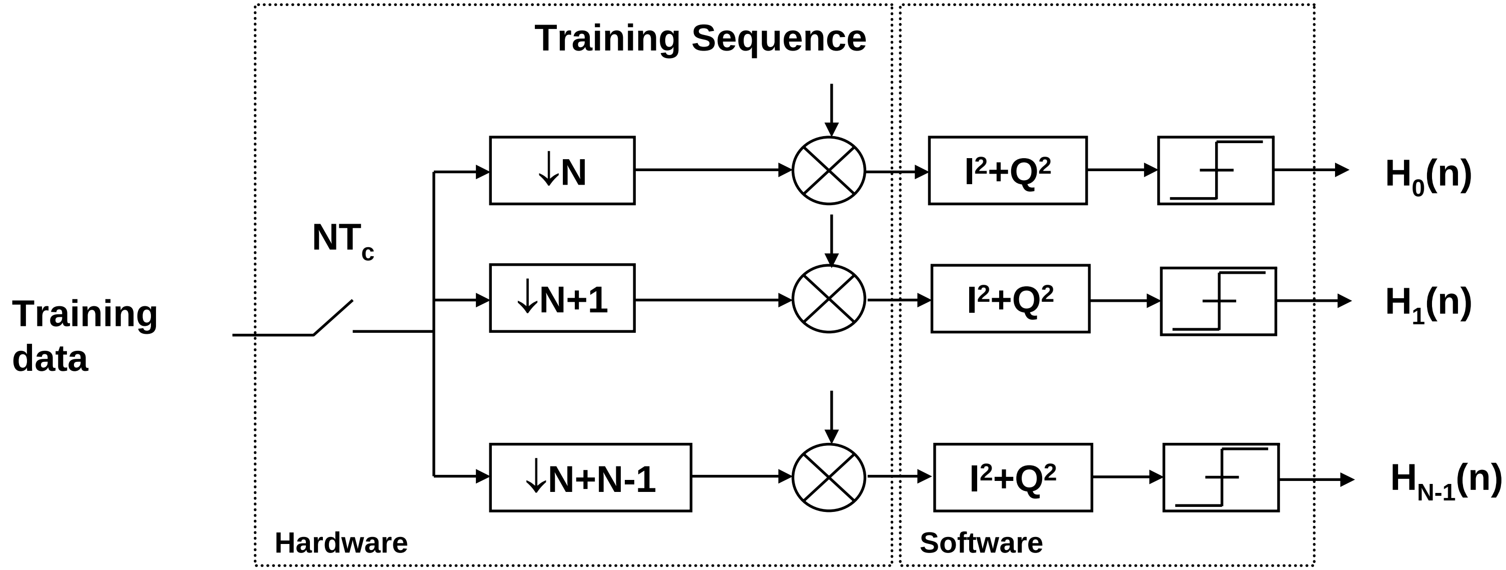
Channel Estimator – Theoritical overview (1)



- This structure estimates the Amplitude and the Delay of each path :

$$Hi(n) = \Sigma p \in [0; P-1]\ ap\delta(n-\tau p)$$

- The threshold is calculated by a percentage of the sum of the energy of each branch within « max delay length » window (e.q. P = 57).

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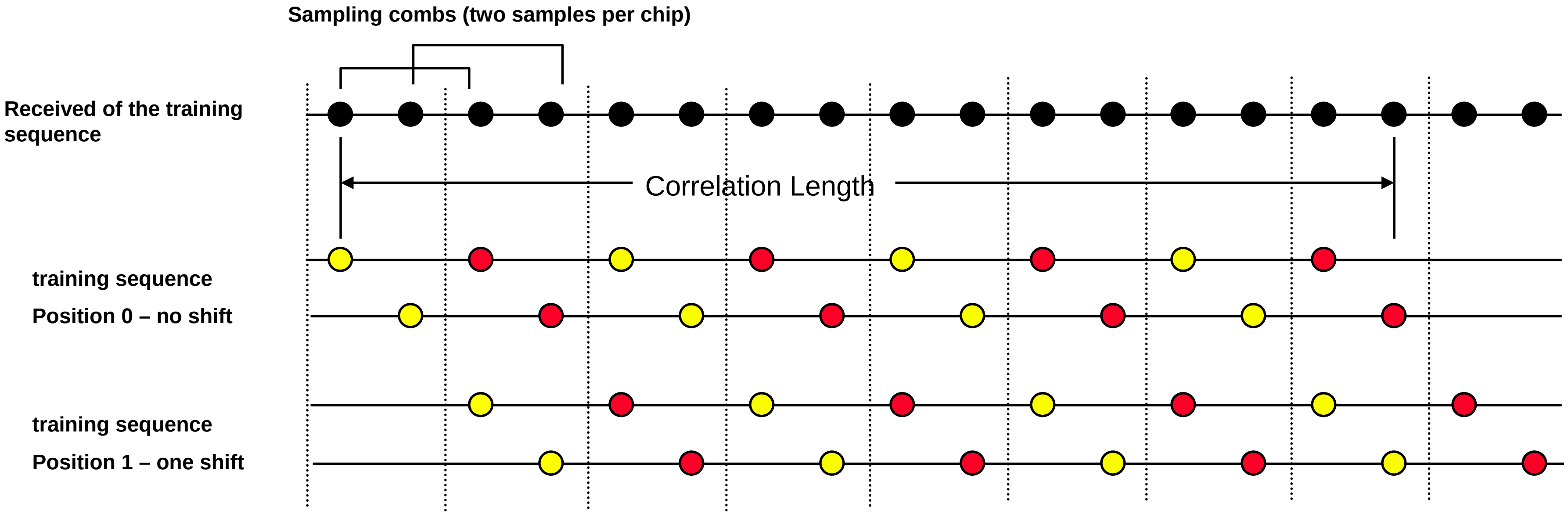
Channel Estimator – Theoritical overview (2)

- Description :
  - Correlation of each sample position (within a searching Window) with the training sequence.
  - The correlation outputs enables to find the path for each sampling comb.



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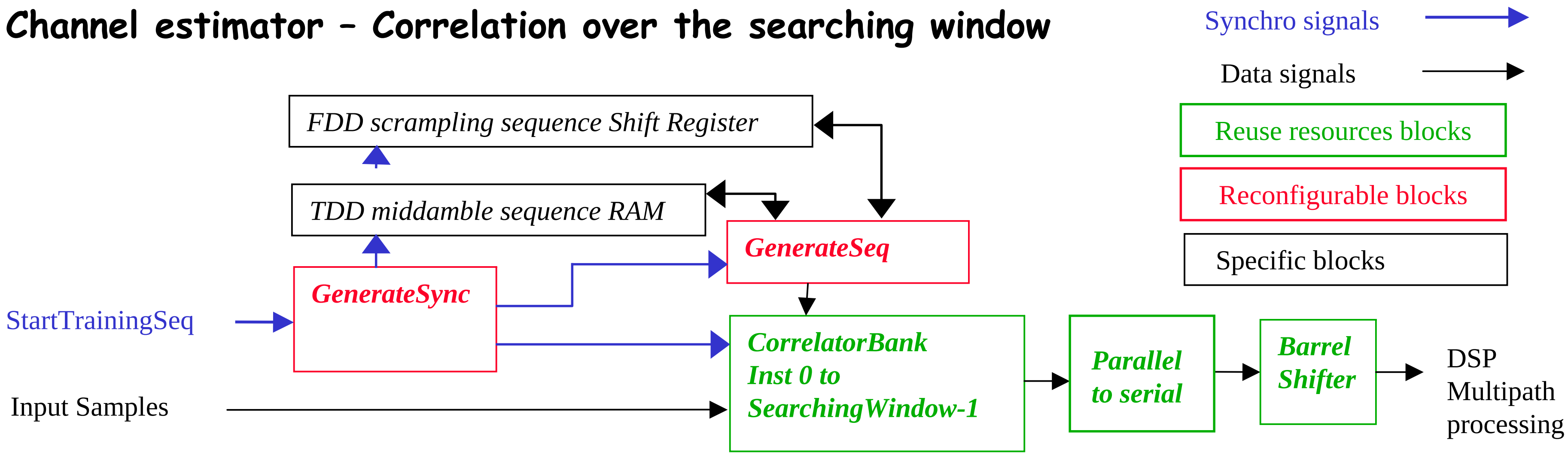
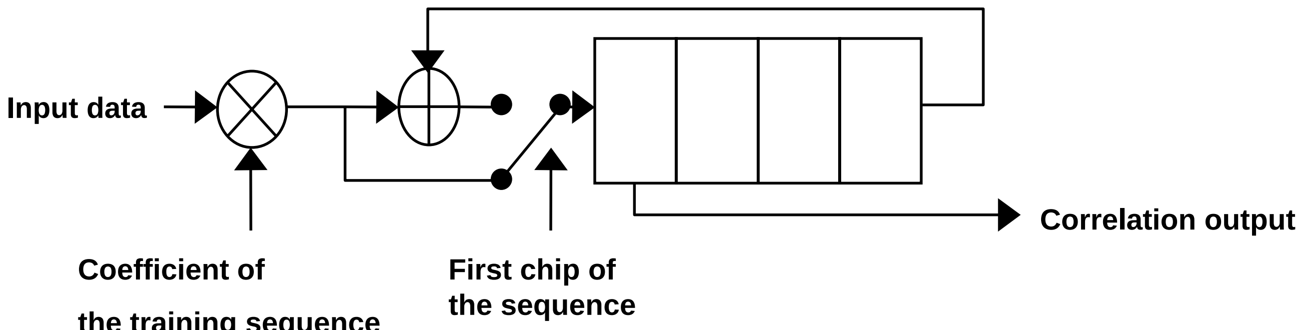
Example of reconfigurability and harware limitation : the channel estimator (1)

Channel estimator – Correlation over the searching window



Basic correlator – 4 samples per chip – correlation over the training sequence



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Example of reconfigurability and hardware limitation : the channel Estimator (2)

- Design hypotheses (default parameters) :
  - The start of the training sequence is known,
  - Sampling rate = 4 samples per chip,
  - Input dynamics = 12 bits
- In the three modes, the correlation length and the searching window size are different.
- The number of correlators and their dynamics are constrained by the FDD mode.
- Correlators are activated through "enable" signals over the sequence length, managed by the "GenerateSync" block.
- The TDD mode reuses a part of the hardware resources.

	FDD/HSDPA	TDD burst 1	TDD burst 2	Choosen parameter
Searching Window Size	297	64	57	64
Correlation length	2048	512	256	2048

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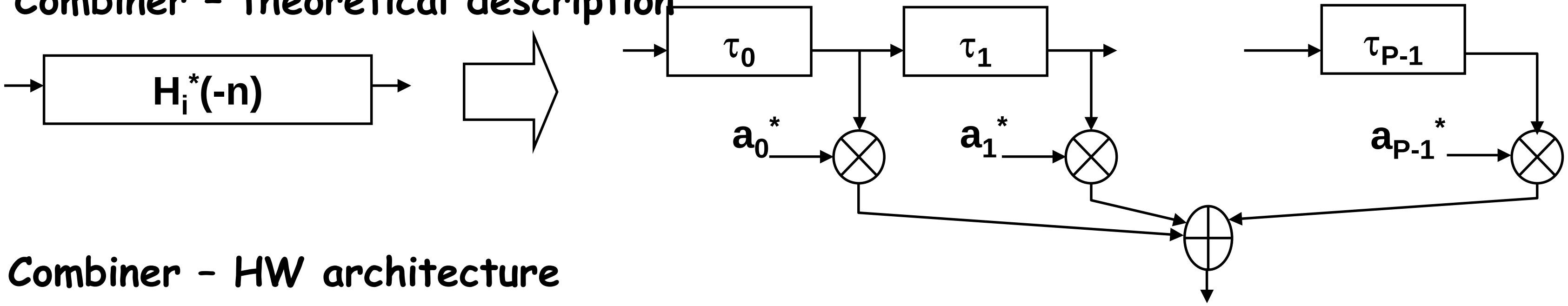
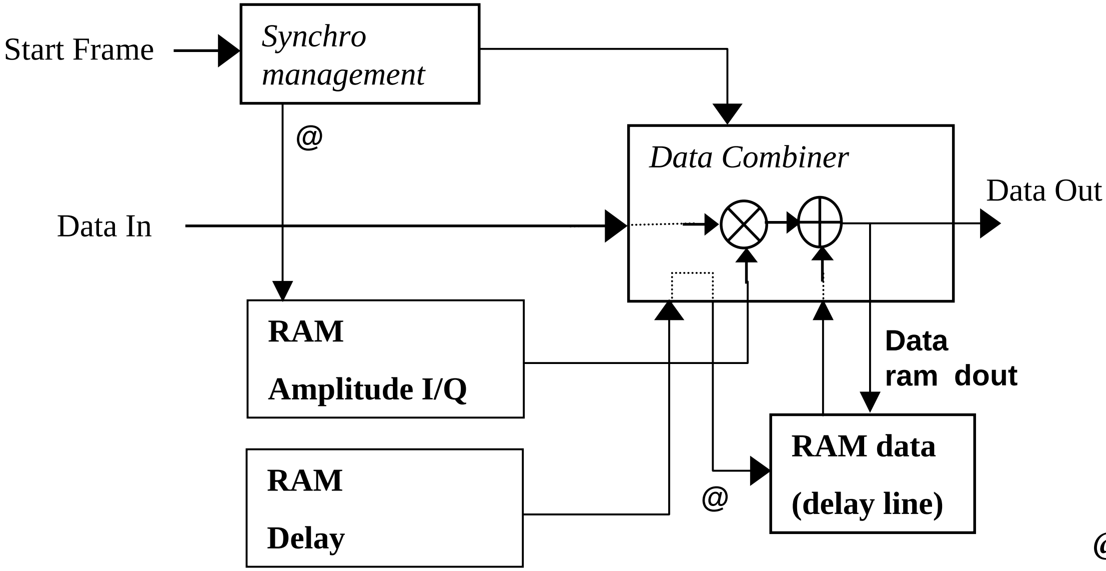
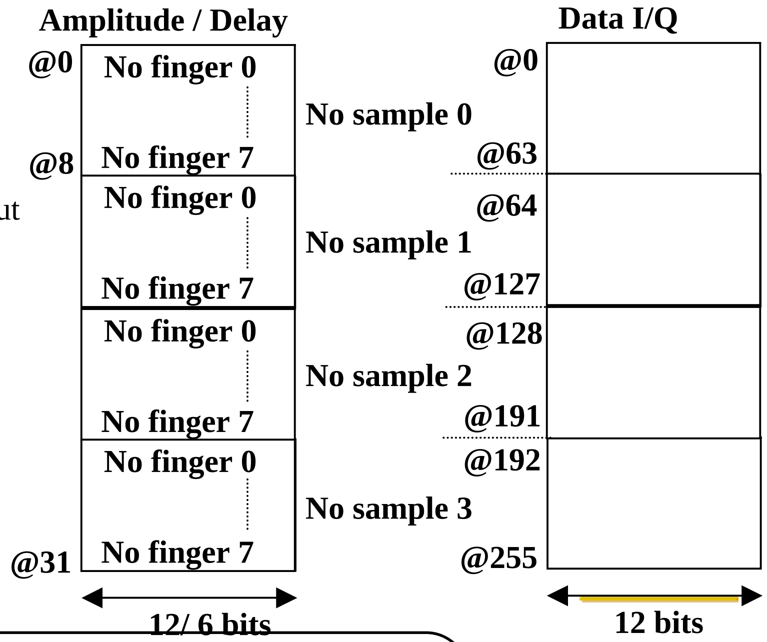
Example of mapping of architecture into HW: the Rake Combiner – architecture (1)

Rake Combiner – theoretical description



Rake Combiner – HW architecture





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Example of mapping of architecture into HW: the Rake Combiner – the delay line (2)

➢ Timing constraint with 8 finger and 4 sample per chip, and a serial processing of the data (not as on the theoretical scheme) :

During one chip period, we have to process P Ram access : 1 writing and P-1 reading.

Thus, processing frequence must be up to :

$$Fclk = P \times Nspc \times Fchip$$

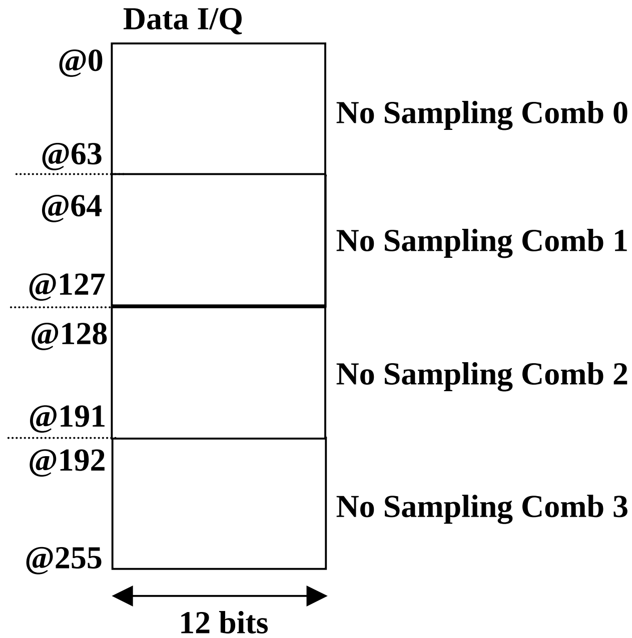
$$Fclk = 8 \times 4 \times 3.84 = 122.88 \text{ Mhz}$$

➢ Address processing of the delay line :

@Read(NoSample) =

@Write(NoSample) – Delay[NoFinger, NoSample]

mod SearchingWindow



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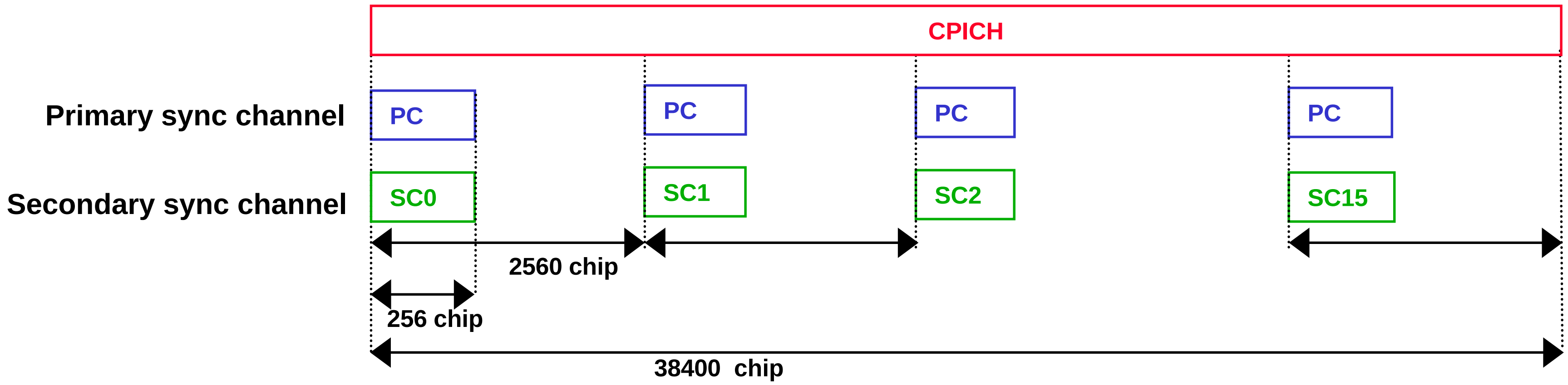
Cell Searcher : main purpose

- The synchronisation channel (for FDD mode) is the following :



- The Cell Searcher is divided into three steps :

Step 1 : finding the **slot synchronisation** by processing the primary code (PC),

Step 2 : finding the **frame synchronisation** by processing the secondary code (SCx) and finding the **scrambling code group**,

Step 3 : finding the **scrambling code** of the cell by processing the CPICH.

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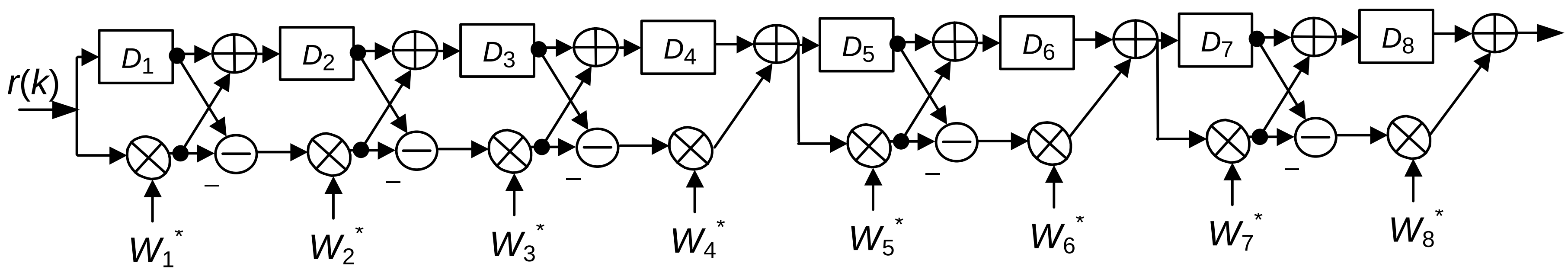
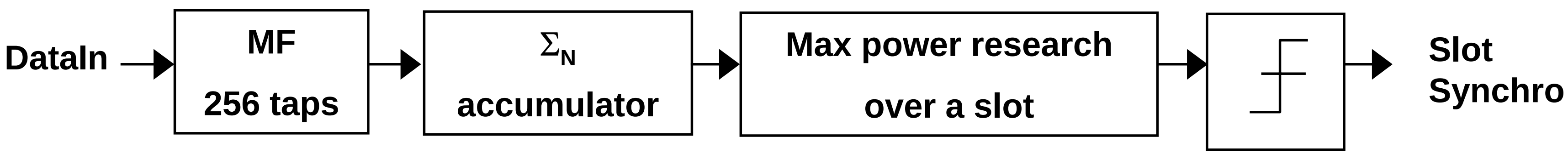
Cell Searcher : Step 1 - Primary Synchronisation Code

- Correlation over **the** primary synchronisation code,
- The implementation of a golay structure (possible due to the sequence properties) instead of a classic matched filter leads to a gain of 3 in terms of hardware resources.



- The result of the correlation is averaged over N slots to get the « good » correlation peak :



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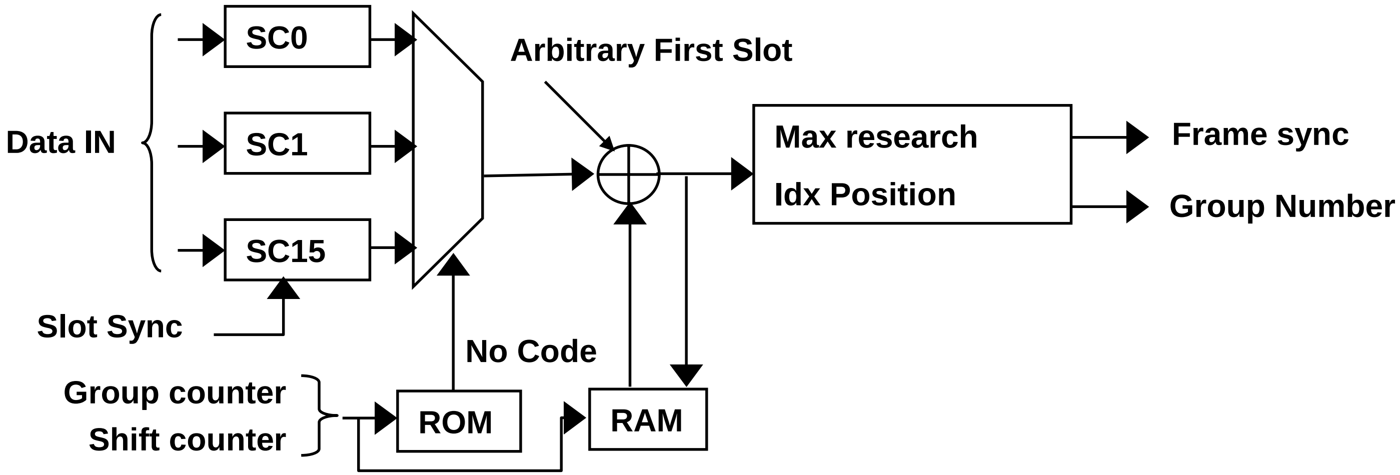
Cell Searcher : Step2 - Secondary Synchronisation Code

- Correlators SCx are initialized by the step 1 synchronization signal (Slot Sync).
- Get the 16 output results of the correlation.
- Soft algorithm on the decision variable **max(|I|+|Q|)**,
- Two memories :
  - A ROM (16×15 adresses; 4 bits words) which allocates the secondary scrambling codes for secondary synchronisation channel according to the standard.
  - A RAM (16×15 adresses; 24 bits words) which stores the decision variables for every group and every shift position.



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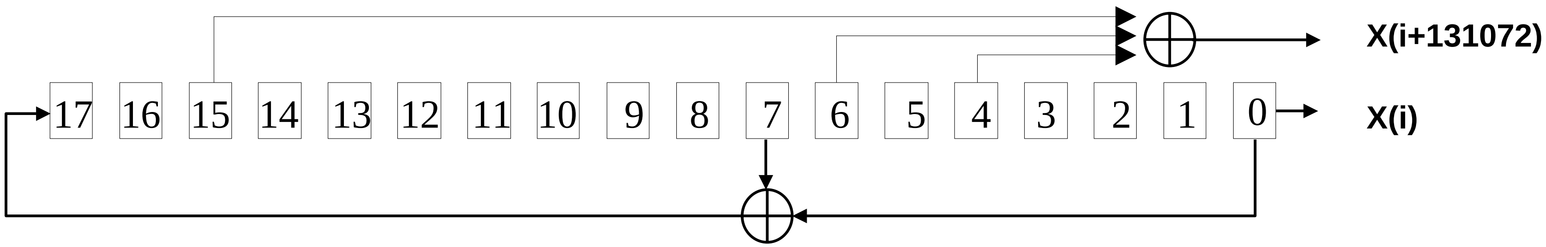
Cell Searcher : Step3 – CPICH decoding - 1

- The aim of this step is to determine the scrambling code among 512 according to the formula : $16 \times 8 \times G + 8 \times K$. From the step 2, we know G ($\in$[0;63]). The step 3 enables to calculate K ($\in$[0;7]) by searching the max over the 8 correlation outputs with the shifted scrambling register
- The basic scrambling code generator X register is :



- We have to calculate the 512×2 following shifts :

  Group = 0 : 0, 8, 16, 24, 32, 40, 48, 56 and 131072, 131080, …., 131128

  Group = 1 : 128, 136, 144, 152,160, 168, 176, 184 and 131200, 131208, …, 131128

  Group = 63 : 8064, 8072,…, 8120 and 139136, 139144, …, 139192

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Cell Searcher : Step3 – CPICH decoding - 2

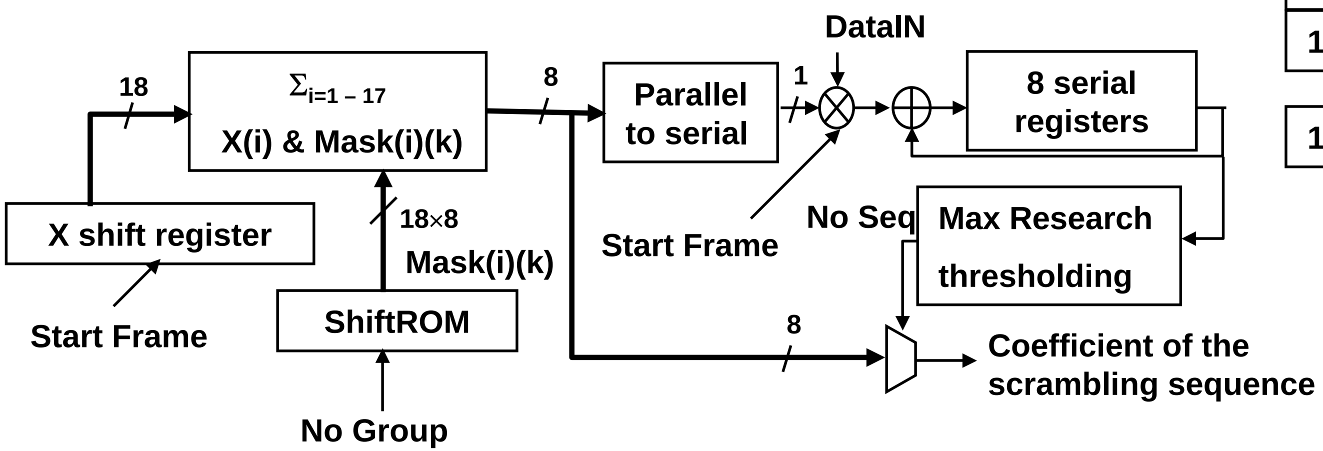
- Definition of a ROM (width : 18×8; depth : 64) fulfil with the shifted mask of the X register,

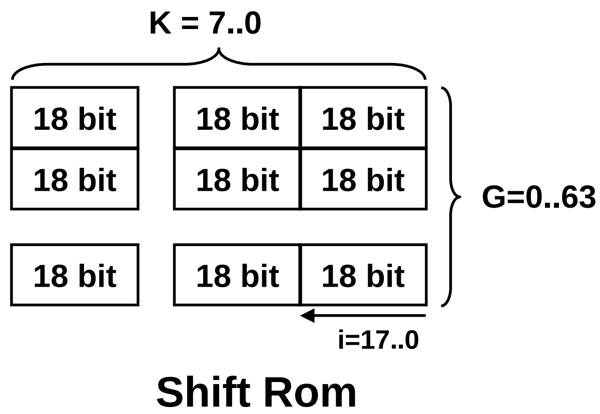
  Ex : G = 1, K = 7 $\Rightarrow$ 184 shifts; the output of the X register is

  $X(16) \oplus X(13) \oplus X(12) \oplus X(8) \oplus X(7) \oplus X(6) \oplus X(4) \oplus X(1) \oplus X(0)$

  The associated mask is 131D3 (hex value)

- One eigth register contains the maximum of the correlations. This maximum enables to get the number of the sequence and thus the coefficient.





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Synthesis results & conclusions

Hypotheses : 4 samples per chip; 8 Rake fingers; Delay max = 64, 12 bits input data.

Include Hunt board hardware design

	Channel Estimator	Data Combiner	CellSearcher Step 1 & 2
Frequency max (expected)	32MHz (15.36 MHz)	126 MHz (122.88MHz)	Not constrainted
Nb of Slices (% of a 4M gates Xilinx)	13845 (60%) (88% if 8 spc)	660 (3%)	5415 (23%)

Conclusions :

- Importance to target the adequate component, to prove that the design is feasible or not (for example, a parallel architecture is not feasible due to the duplication of hardware).

- The FDD searching window (297) is not supported by a single FPGA (in terms of area).

- The parameters of one "data combiner" block must verify $Nspc \times Nfinger \leq 32$; In the other case (e.g. 8 spc, 8 fingers) we have to duplicate the block.

- Power consumption vs frequency and area (e.g. Data Combiner – Power estimation using HCMOS 9 process : 0.05µW/MHz, 20% switch gates $\Rightarrow$ 0.15mW)

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WP4 : Future work

Year 2003												Year 2004								
10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	Front-end demonstrator 4.1																			
			Baseband demonstrator 4.2																	
Clustering and standardisation activities 4.3																				
																		4.4		

- Future activities :
  - Integration of the WP3 results (bit true modelling) in the preliminary design,
  - Integration of the partner modulesGeneration of test files from the multimode software chain; test on HW simulation and implementation board,
  - Carry on the design of building blocks, and Cell Searcher.

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