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# Multi-mode approach for frequency synthesizers

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**MUMOR – IST-2001-34561**

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# Outline

- Requirements on multi-mode synthesizers
- Description of the target application
- Comparison of synthesizer architectures
- Design description
- Summary
- Conclusion

# Requirements on multi-mode synthesizers

- In transceiver frontends, multi-mode operation concerns the synthesizer mainly in terms of...
  - frequency bands
  - phase noise / spurious performance
  - settling times
- Combining hardest spec from each mode into single "all-purpose synthesizer" often results in a over-designed system => costs, power
- Building separate synthesizers for each mode is straight-forward, but needs additional silicon area and board space => costs
- A multi-mode synthesizer combines low area and low power by sharing reconfigurable components for multiple modes

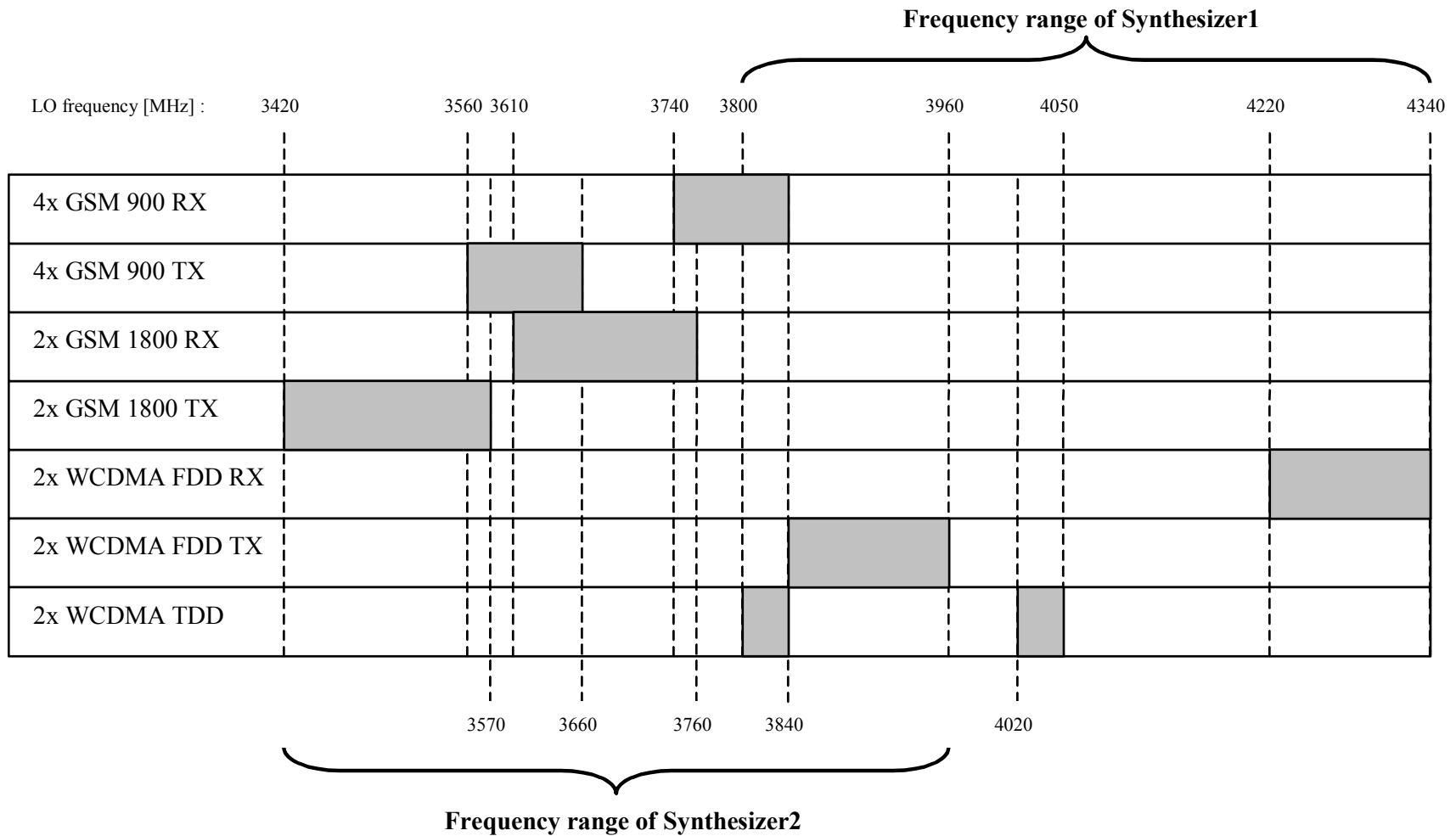
# Target application

- Direct conversion frontend supporting WCDMA / HSDPA and GSM 900 / 1800 modes

	WCDMA-FDD	
	WCDMA Mode	GSM Mode
<b>Synthesizer1:</b>	WCDMA RX	monitoring WCDMA
<b>Synthesizer2:</b>	WCDMA TX, monitoring GSM	GSM RX & TX
	WCDMA-TDD	
	WCDMA Mode	GSM Mode
<b>Synthesizer1:</b>	WCDMA RX & TX	monitoring WCDMA
<b>Synthesizer2:</b>	monitoring GSM	GSM RX & TX

Proposed two-synthesizer architecture

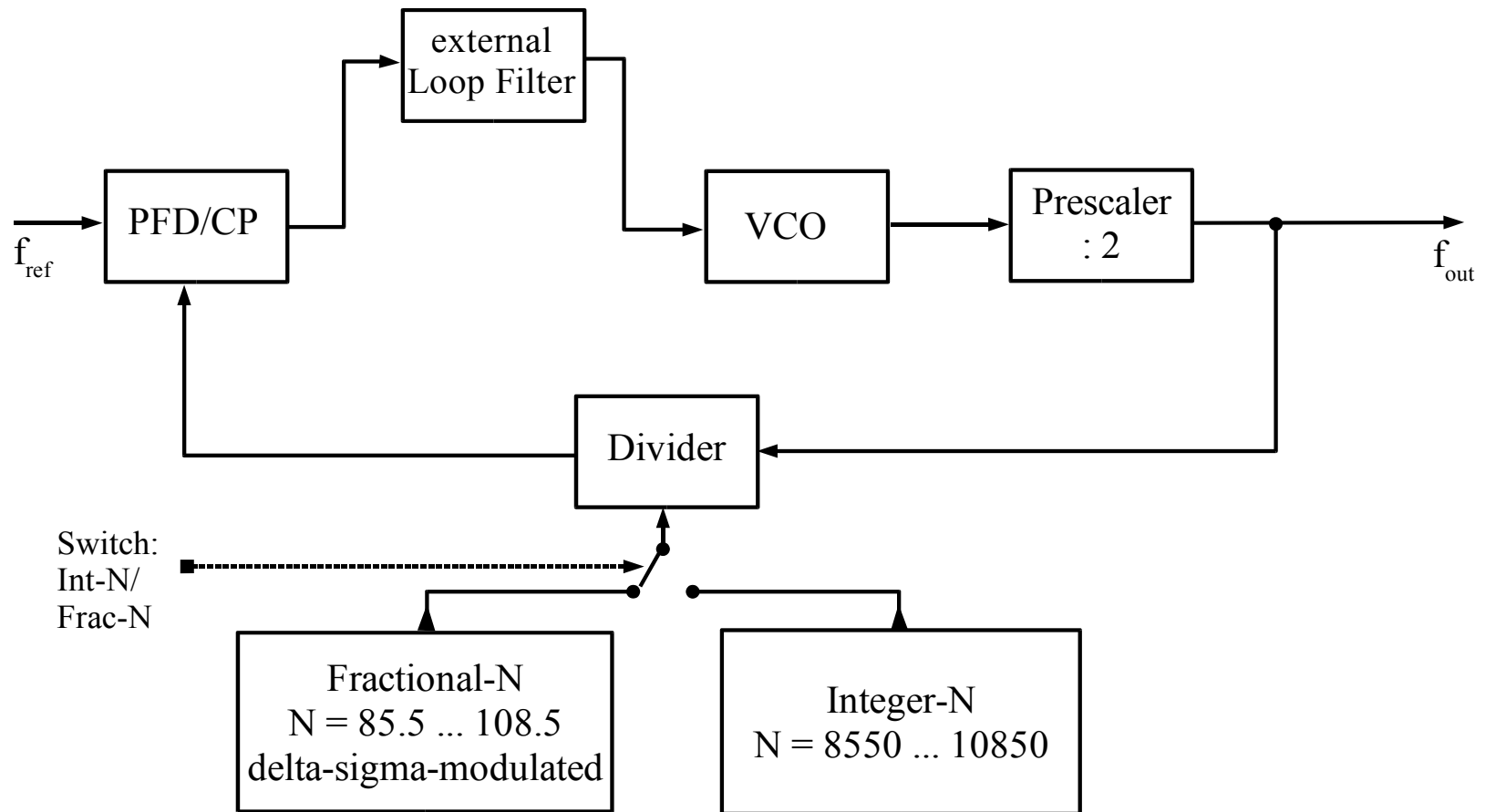
# Frequency plan



# Comparison of PLL synthesizers

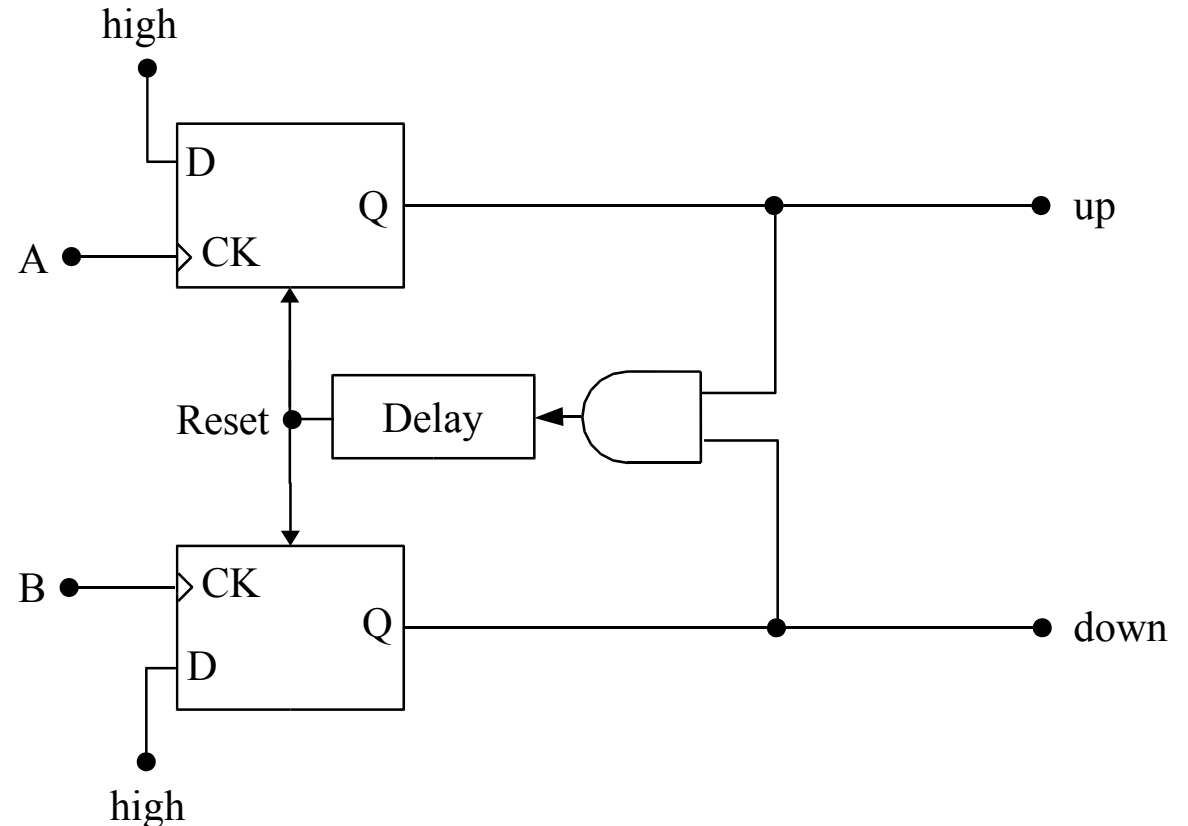
	Integer-N PLL	$\Delta\Sigma$ Frac. N PLL	Dual Loop PLL	SO PLL	DDS & Int-N PLL
<b>Loop bandwidth</b>	low	medium	high / low	medium/high	medium
<b>Settling time</b>	slow	fast	slow	fast/fast	fast
<b>Required VCO phase noise performance</b>	high	medium	medium / medium	high/medium	medium
<b>Created noise level</b>	medium	high	high	high/low	high
<b>Design complexity</b>	medium	high	high	high/medium	high
<b>Area consumption</b>	low	medium	high	medium/low	high
<b>Power consumption</b>	low	medium	high	medium/low	high

# Synthesizer block diagram



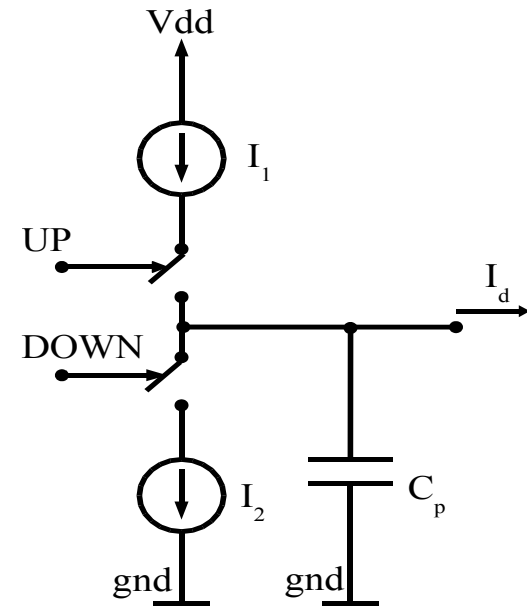
# Phase and frequency detector

- Implemented with CMOS standard cells
- No dead-zone
- Minimum CP pulse width programmable via delay cell in reset path



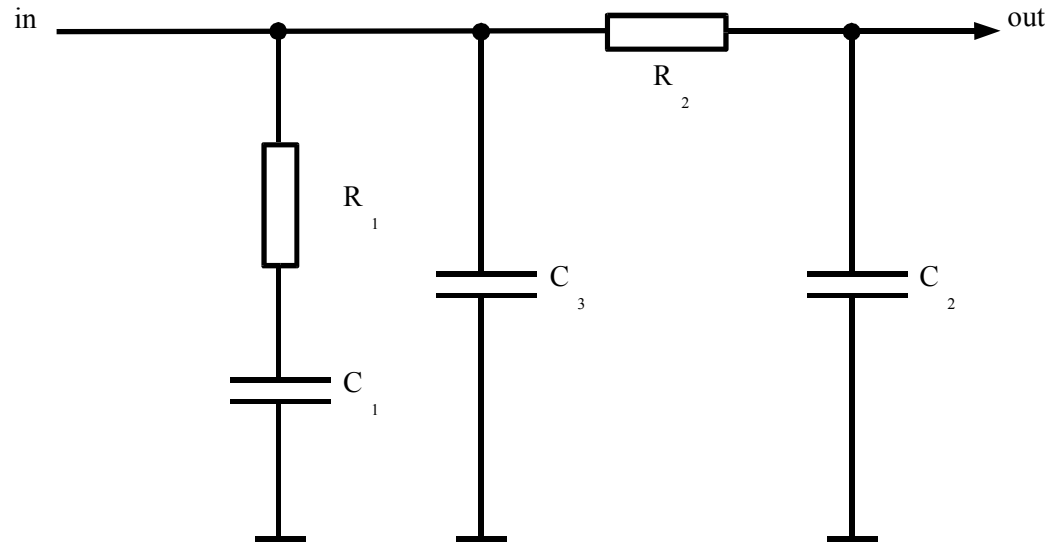
# Charge pump

- Standard CMOS implementation
- UP / DOWN current mismatch critical for spurious performance => especially in fractional-N mode
- UP / DOWN currents can be adjusted independently



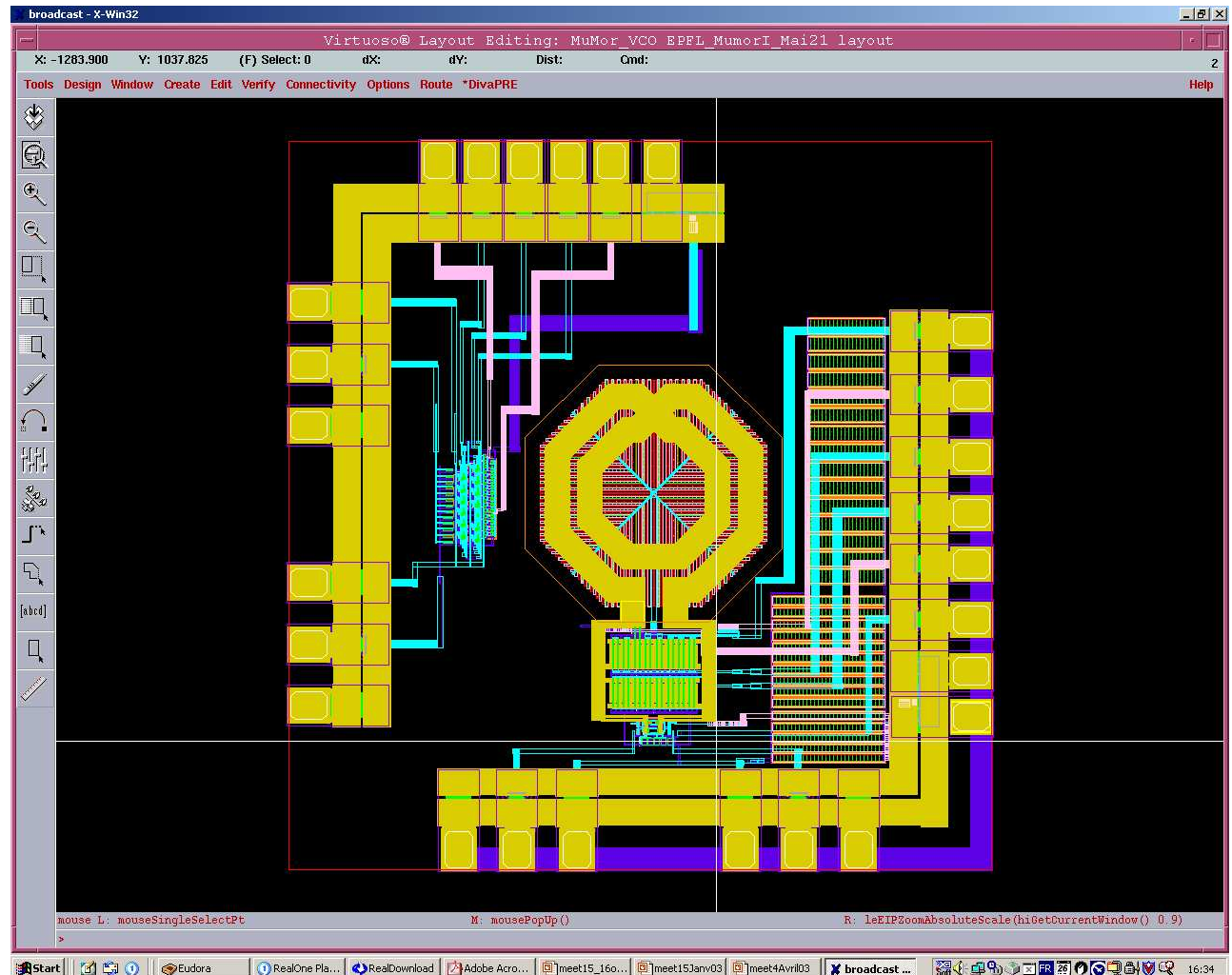
# Loop filter

- 3rd order passive loop filter
- current input, voltage output
- left off-chip for extended flexibility



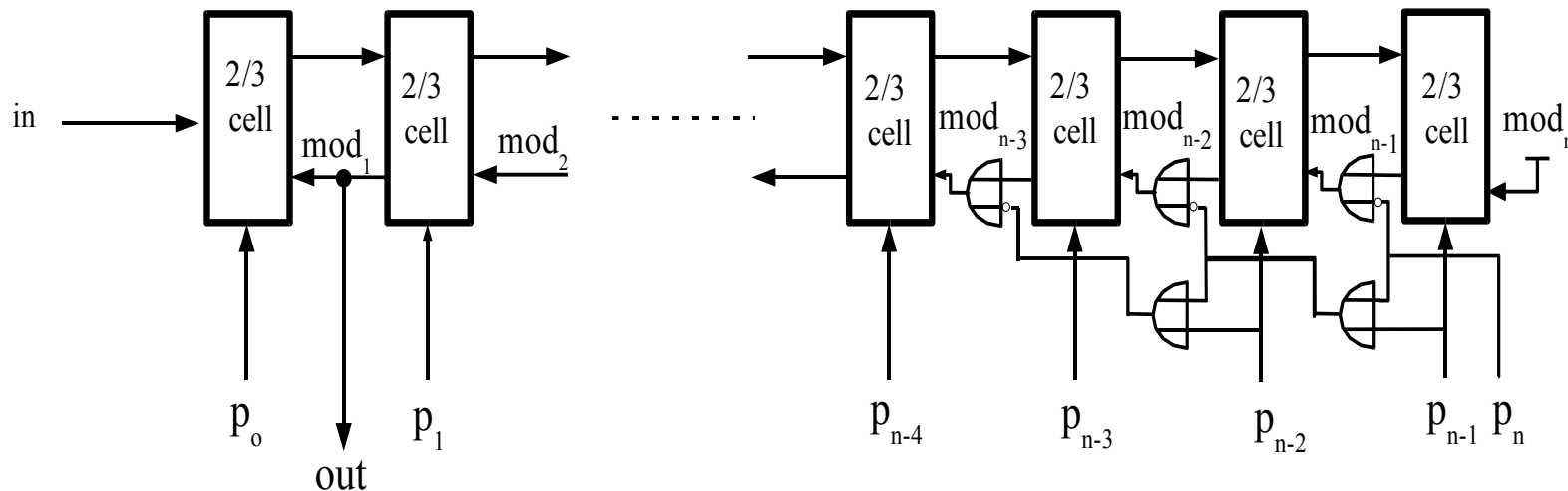
# Voltage controlled oscillator

- Multi band VCO with switched capacitor network
- Phase noise optimized design
- Low power consumption
- Developed by EPFL



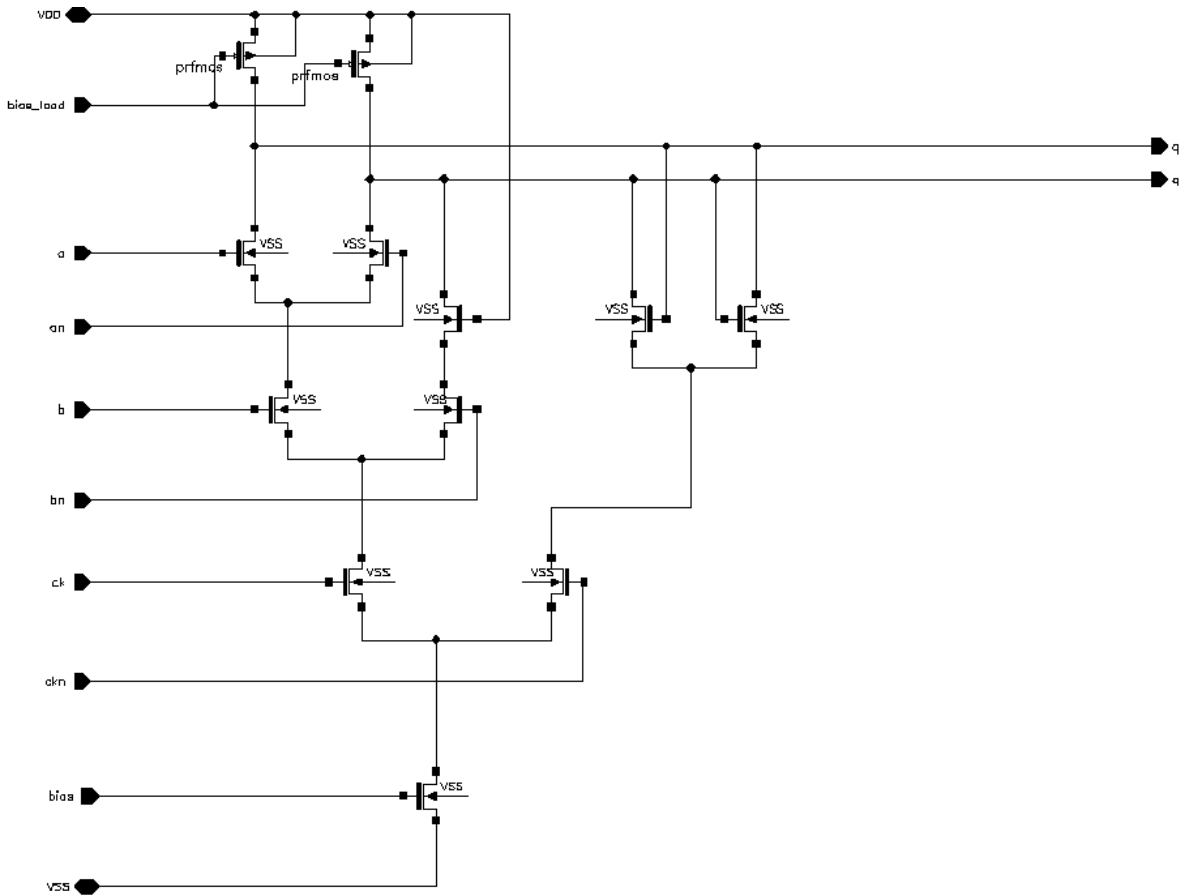
# Frequency divider

- Non-standard asynchronous divider utilizing concatenated 2/3 cells
- Achieves ultra wide division range ( $N = 64 \dots 16384$ ) for both integer- $N$  and fractional- $N$  operation





# Frequency divider (contd.)



- Current scaling in SCL gates: Subsequent stages need less current since frequency is decreased after each stage
- Quiescent current and load impedance adaptable to process / temperature conditions

SCL latch with integrated AND gate

# Frequency synthesizer summary

Parameter	Value	Unit	Notes
DC supply voltage	2.5	V	
DC supply current	2.2	mA	excl. VCO, DS
VCO frequencies	3420 .. 4340	MHz	modulo-2 prescaler provides LO for IQ mixing
Divider ratio N	8550 .. 10850 85.5 .. 108.5		Integer-N mode Fractional-N mode
Reference frequency	200 20	kHz MHz	Integer-N mode Fractional-N mode
Phase noise	-119 -139 -150	dBc/Hz @ 600 kHz dBc/Hz @ 5 MHz dBc/Hz @ 20 MHz	based on VCO simulations (EPFL)
Silicon area	0.08	mm <sup>2</sup>	PLL core
Process	B7 (STMicro)		0.25μm BiCMOS

# Conclusion

- A multi mode synthesizer for a direct-conversion WCDMA/HSDPA and GSM 900 / 1800 RF frontend has been developed
- It incorporates a multi-band VCO and a flexible frequency divider that enables Integer-N and Fractional-N operation
- Asynchronous frequency divider
  - chain of 2/3 divider cells
  - combination of SCL and standard CMOS logic optimizes power consumption
  - extremely wide division range
- Synthesizer designed to operate with voltage-controlled oscillator developed by EPFL