



Reconfigurable pipeline Analog/Digital Converter for WCDMA/GSM operation

**T.NIKOLAIDIS, A.VARAGIS, D.FRAGOPOULOS
B.S.SINNIS and N.VENIOS**



OUTLINE:

- **Specifications**
- Pipeline ADC architecture operation
- Behavioral modeling
- Transistor level design of 10bit/15MHz pipeline ADC
- Results on schematic and layout extracted simulations
- Conclusion

Specifications for ADC

Parameter	UMTS FDD/TDD	UMTS HSDPA	GSM
Signal bandwidth	~2.5MHz	~2.5MHz	~200KHz
Resolution	8bits	10bits	10bits
ENOB	-	>9bits	>9bits
Sampling Frequency	15.36Msamp/sec	15.36Msamp/sec	2.16Msamp/sec
SNR	>40db	-	-
Peak signal amplitude	1.0V	1.0V	1.0V
Input impedance	>100kO	>100kO	>100kO

8-10bit/2.16-15.36MHz reconfigurable architecture

Brief description of Nyquist ADC architectures

Architecture	Performance				
	Resolution	Speed	Power	Area	Mismatch Sensitivity
Flash	Medium (up to 8bits)	Very fast	Very high	High	Medium to Low
2step	Medium (upto 8 bits)	Fast	Medium	Medium	Medium to Low
Interpolative	Medium (upto 8bits)	Fast	Medium	Medium	High
Parallel	Medium to high	Fast	Medium	Medium	High
Pipeline	High (upto 16bits)	Fast	Low	Low	Low

Pipeline architecture offers: a) low power, b) high speed
c) high resolution and d) modularity.

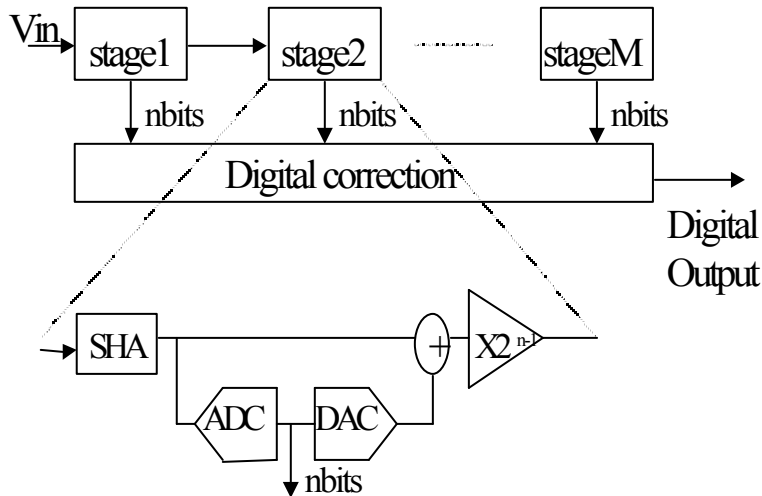


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Pipeline ADC architecture operation

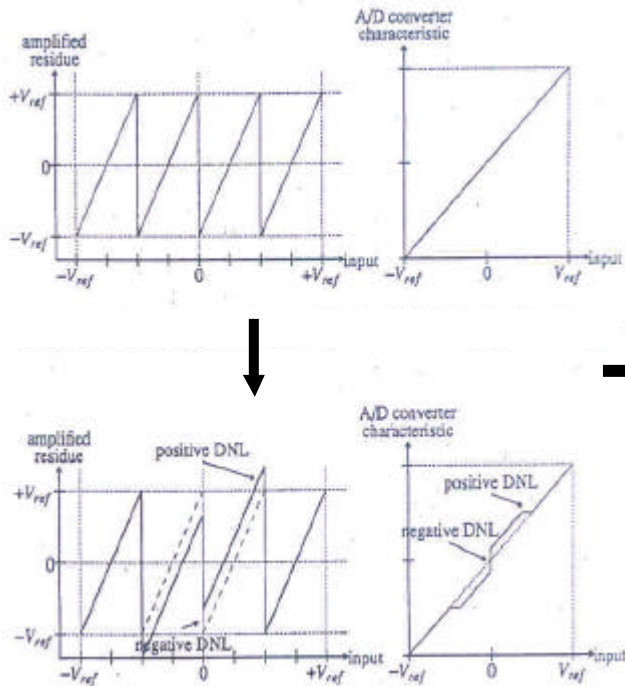
Errors in pipeline ADCs



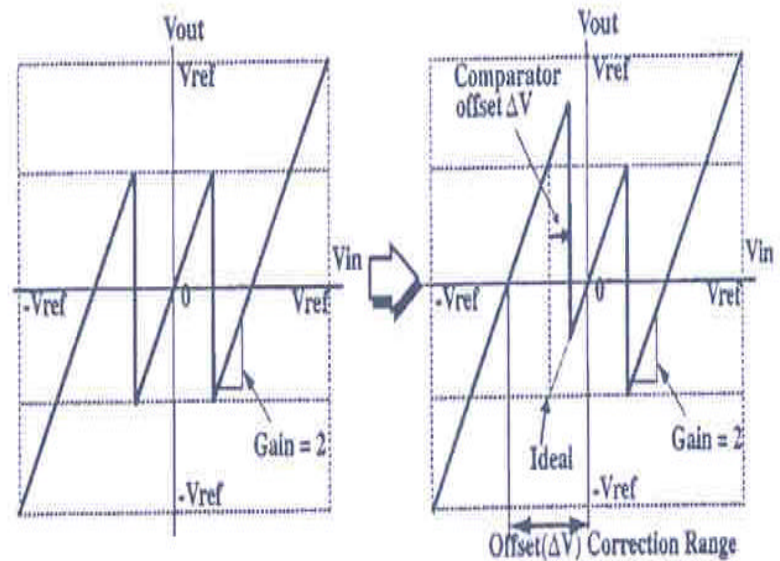
Error sources	Problems	Solutions
Sample and Hold Offset Gain error	DC offset Nonlinearity & Missing codes	Input-referred offset Calibration
Sub ADC Offset Nonlinearity Gain error	Nonlinearity & Missing codes	Digital error cor.
Sub DAC Offset Nonlinearity Gain error	DC offset Nonlinearity & Missing code	Input referred offset Calibration
Residue amplifier Offset Nonlinearity Gain error	DC offset Calibration	Offset cancelation Calibration

Stage operation

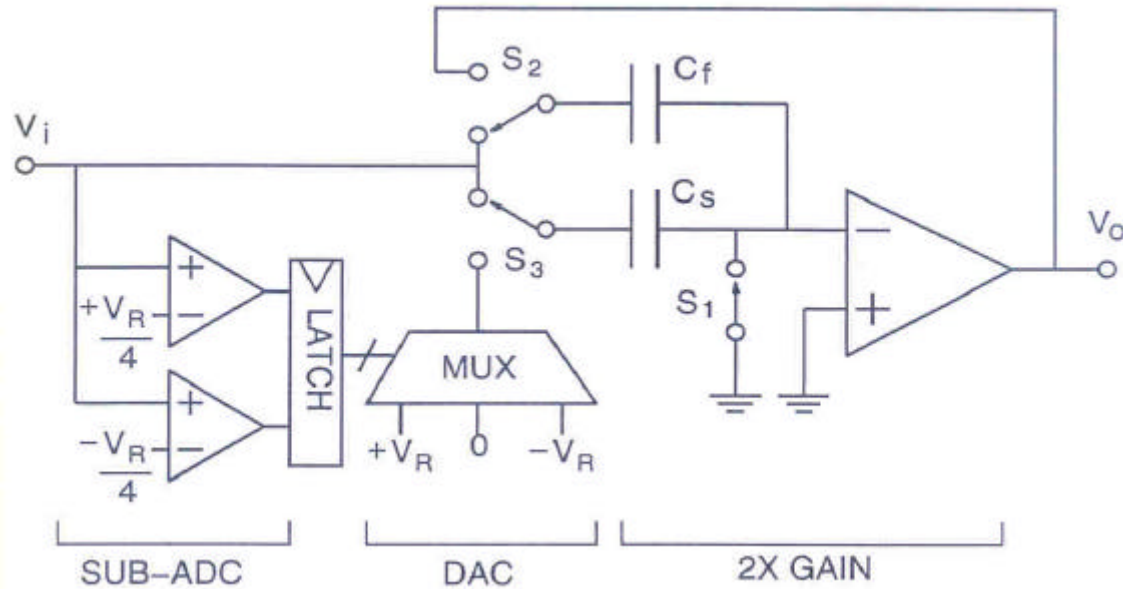
2bit per stage resolution



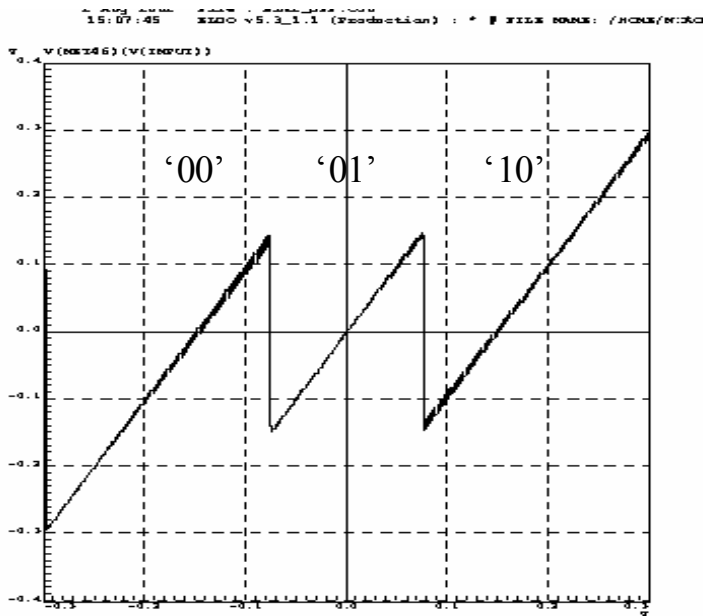
1.5bit per stage resolution



1.5bit resolution stage architecture



Vo versus Vin (Residue amplification)

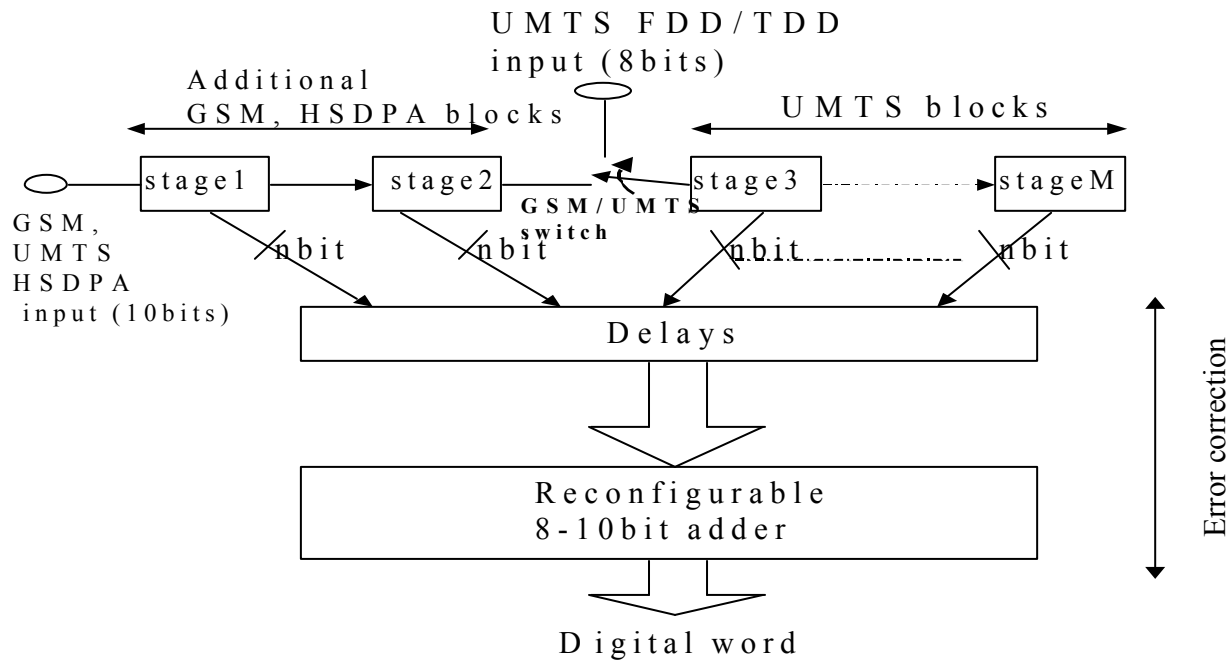


$$V_o = \left(1 + \frac{C_s}{C_f}\right)V_i - V_{ref}, V_i > V_{ref}/4 \quad \text{Code '10'}$$

$$V_o = \left(1 + \frac{C_s}{C_f}\right)V_i, -V_{ref}/4 \leq V_i \leq +V_{ref}/4 \quad \text{Code '01'}$$

$$V_o = \left(1 + \frac{C_s}{C_f}\right)V_i + V_{ref}, V_i < -V_{ref}/4 \quad \text{Code '00'}$$

Proposed reconfigurable ADC architecture





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Main Design Characteristics

For N bit linearity and F_{clock} sampling frequency:

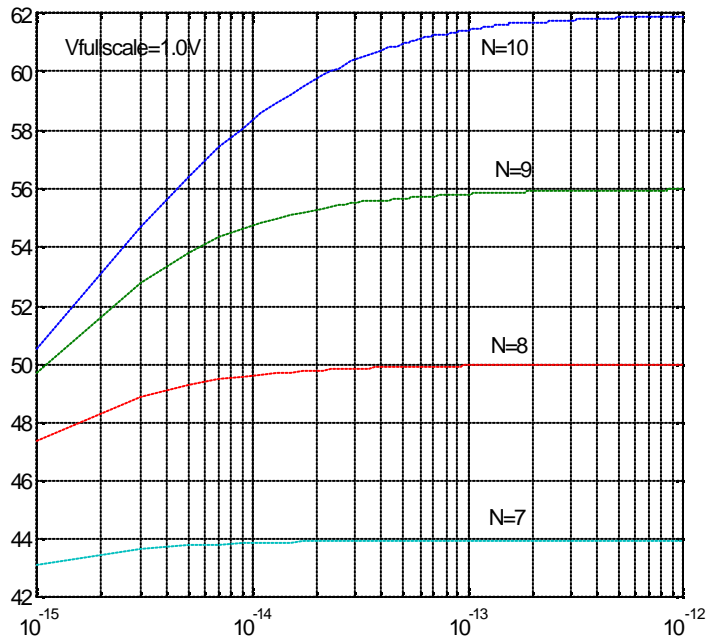
- Amplifier open loop DC gain $> 2^{N+2}$
- Settling time $T_{\text{settle}} < 1/(2 * F_{\text{clock}})$
- Gain Bandwidth GBW $> N \ln 2 / (p * T_{\text{settle}})$
- Noise $V_{\text{noise rms}} < (1/6) * \text{LSB}$
- Capacitor mismatch $(\Delta C/C) < 1/2^N$.

The above parameters relax as we proceed down the pipeline chain. Capacitor mismatch is the most critical parameter.

For 10bit linearity $\Delta C/C < 0.1\%$.

MIM capacitors and careful layout can lead to 10bit linearity.

Extraction of pipeline stage capacitances



$$SNR = 10 \log \left(\frac{V_{fs}^2 / 2}{\frac{(2V_{fs} / 2^N)^2}{12} + \frac{kT}{C}} \right)$$

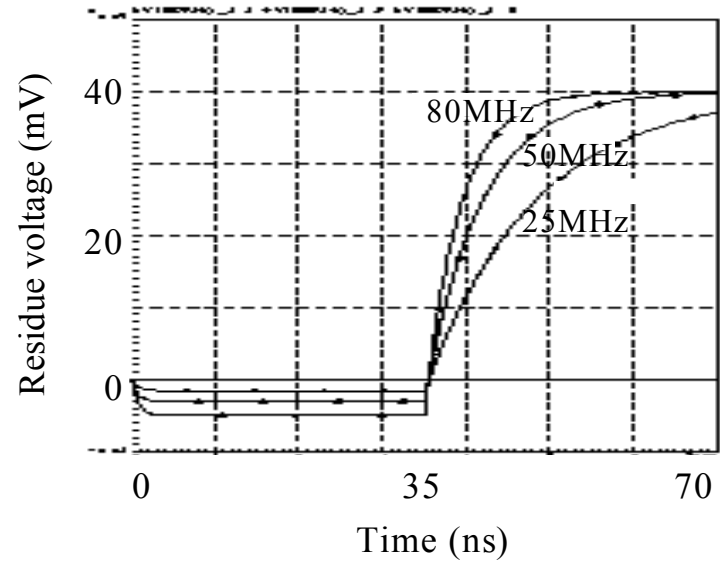
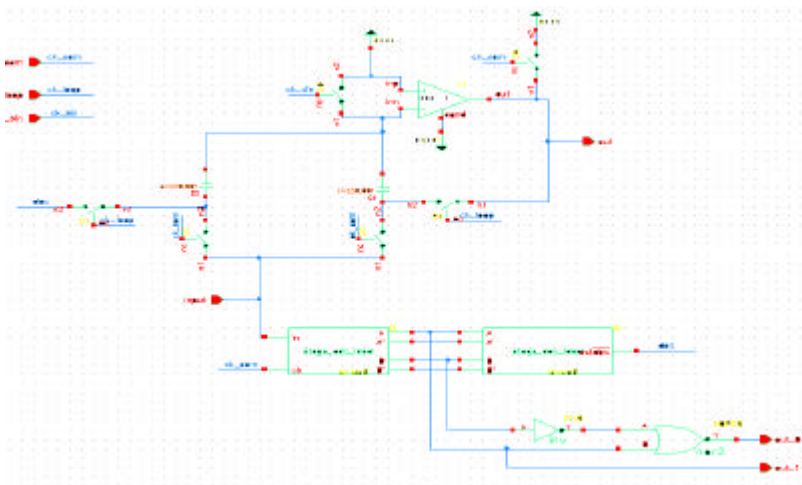
For 10 bit resolution (first two stages):

$$C_1=250\text{fF}, C_2=250\text{fF}.$$

For 8 bit resolution (third and subsequent stages):

$$C=100\text{fF}.$$

Behavioral stage modeling

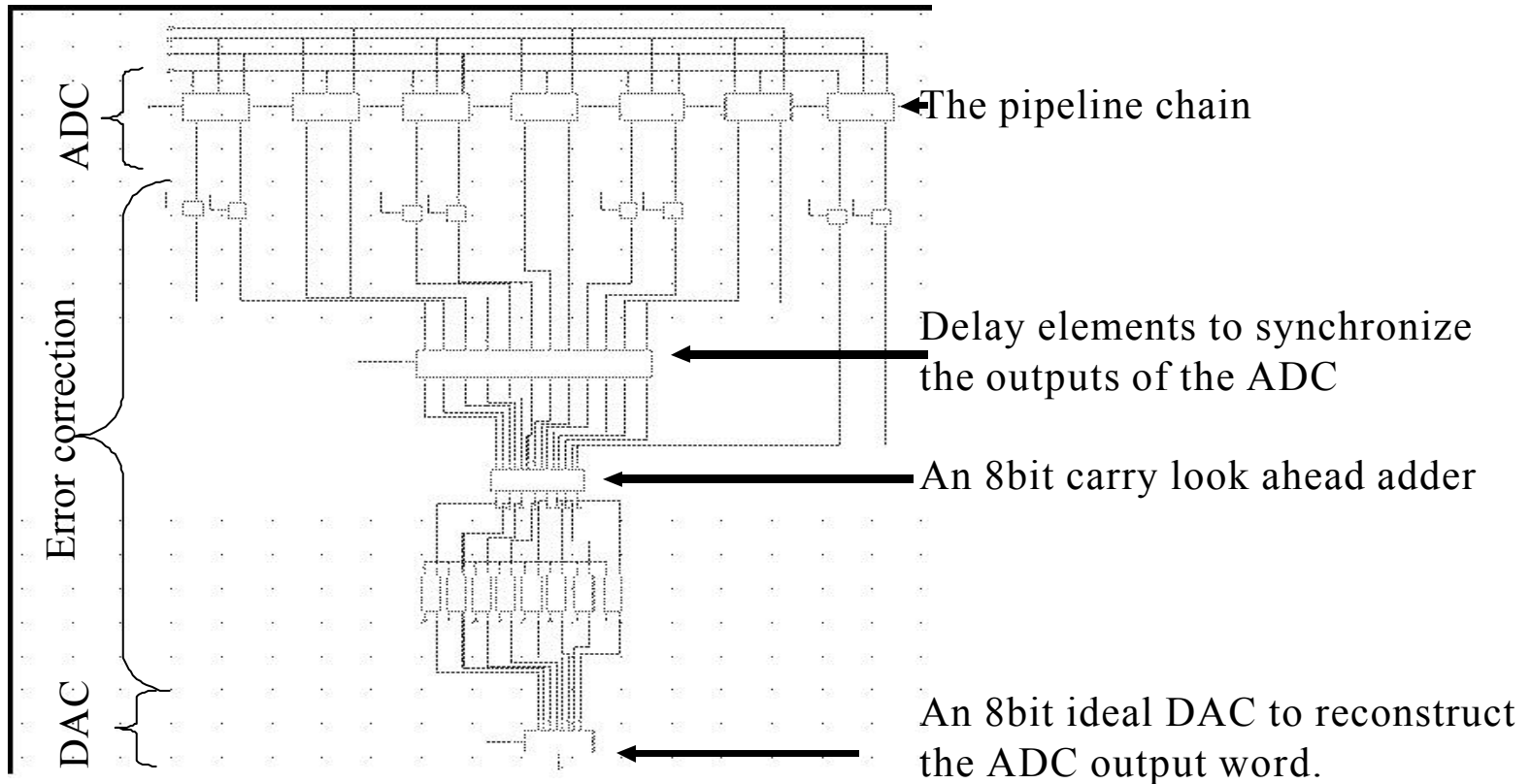


Extraction of switch RON, amplifier GBW

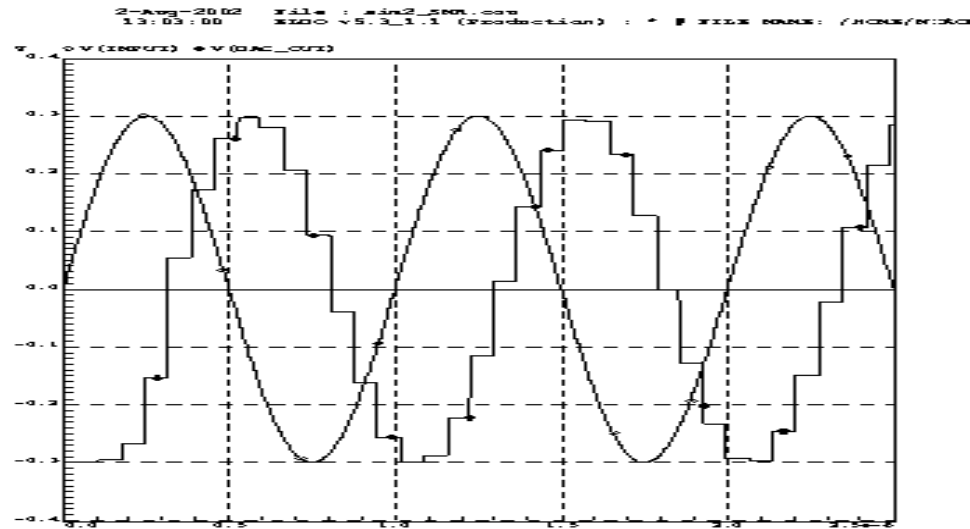
Stage amplifier specifications

Mode of operation	Stage OTA characteristics		
	1 st and 2 nd stage (10bit resolution)	3d and 4 th stage (8 bit resolution)	Subsequent stages
UMTS HSDPA	DC gain>72db GBW>75MHz Cload=0.5pF	DC gain>60db GBW>60MHz Cload=0.25pF	Dc gain>60db GBW>50MHz Cload=0.25pF
UMTS TDD/FDD	-	DC gain>60db GBW>60MHz Cload>0.25pF	Dc gain>60db GBW>50MHz Cload=0.25pF
GSM	DC gain>72db GBW>10MHz Cload=0.5pF	DC gain>60db GBW>8MHz Cload=0.25pF	DC gain>60db GBW>6MHz Cload=0.25pF.

Modeling the ADC (8bit/15MHz)



Digitization of a sinusoidal input signal@1MHz



Behavioral pipeline ADC model for UMTS
TDD/FDD 8bit/15MHz



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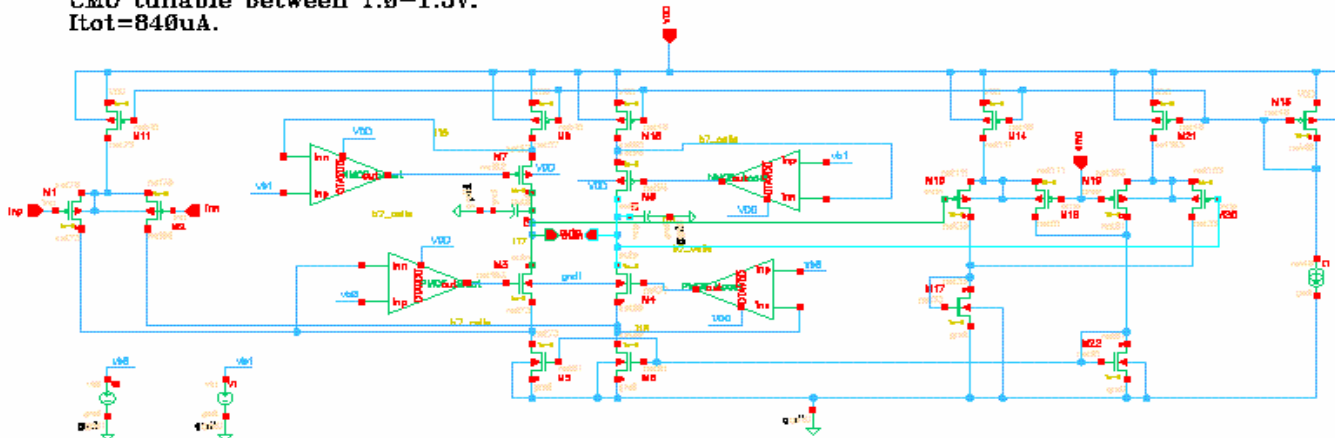
ADC

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Amplifier design

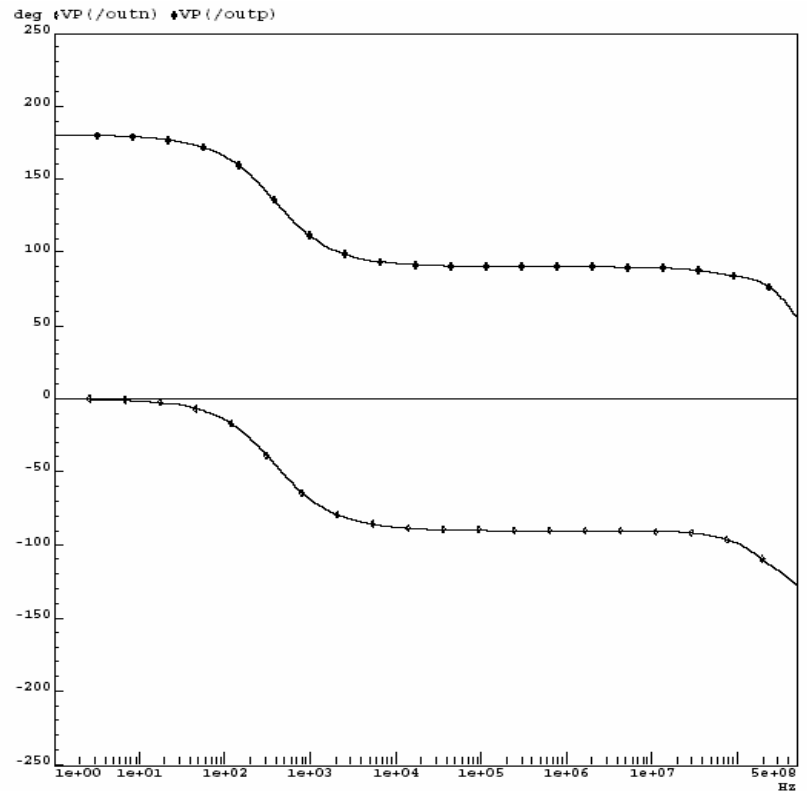
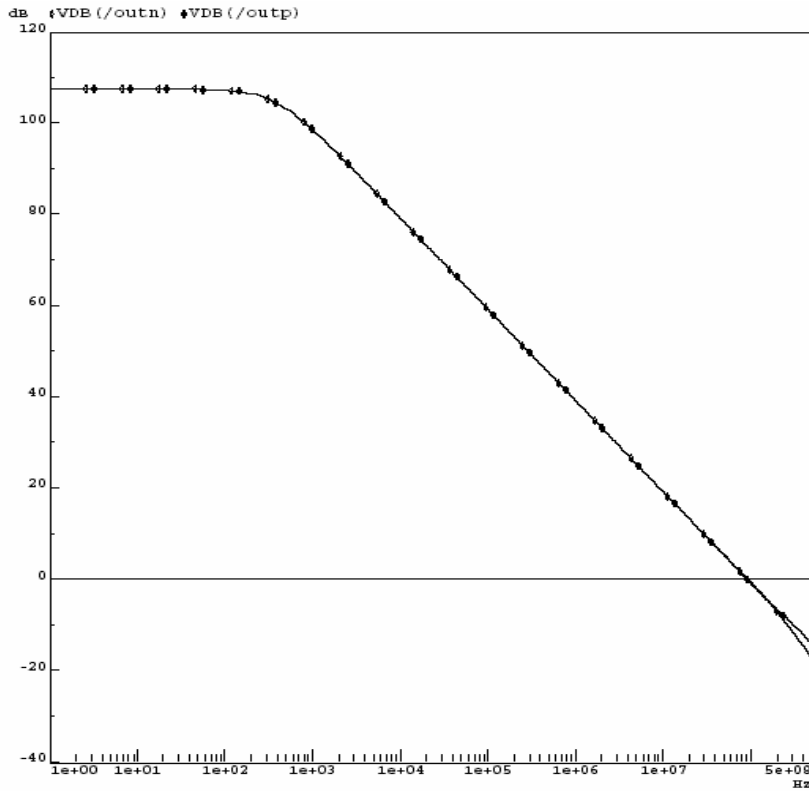
OTA Folded Cascode + gain boosting
with Long Tail Pairs for CMFB.

DC gain~107db, $F_u \sim 90\text{MHz}$, $P_m > 80\text{deg}$ ($C_l = 750\text{fF}$).
CMO tunable between 1.0–1.5V.
 $I_{tot} = 840\mu\text{A}$.

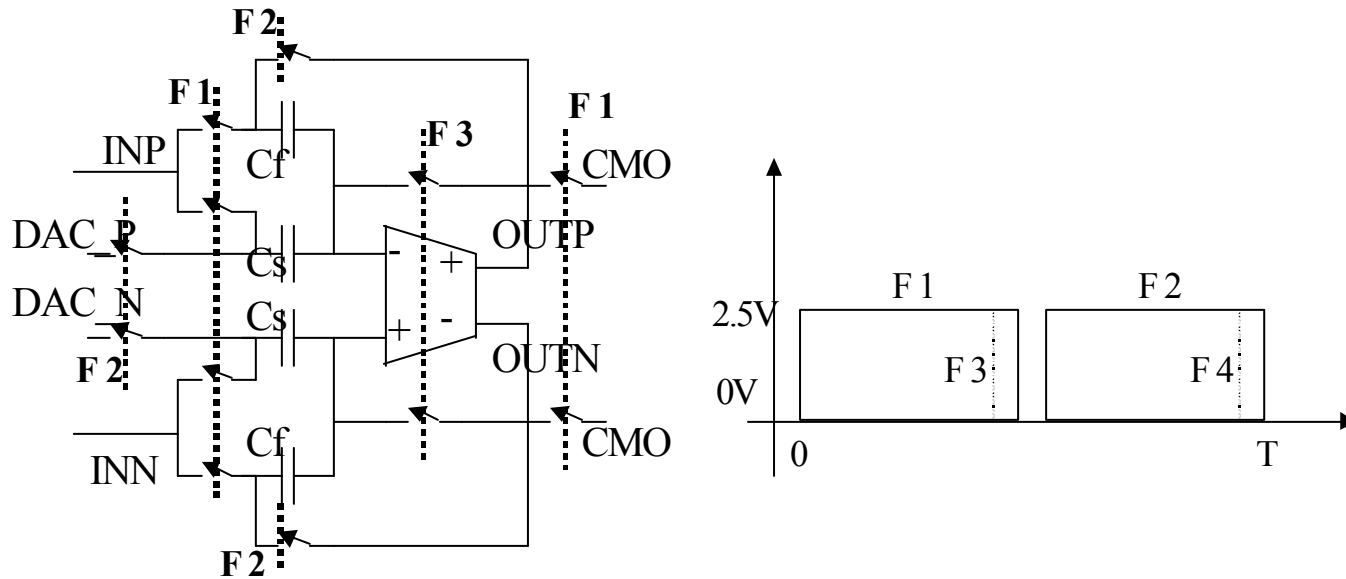




Amplifier performance

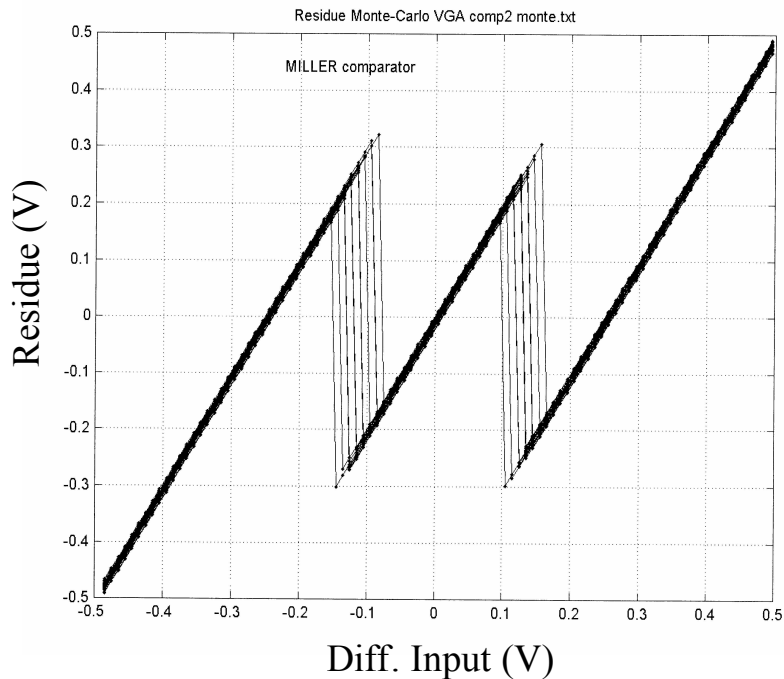


Differential stage implementation



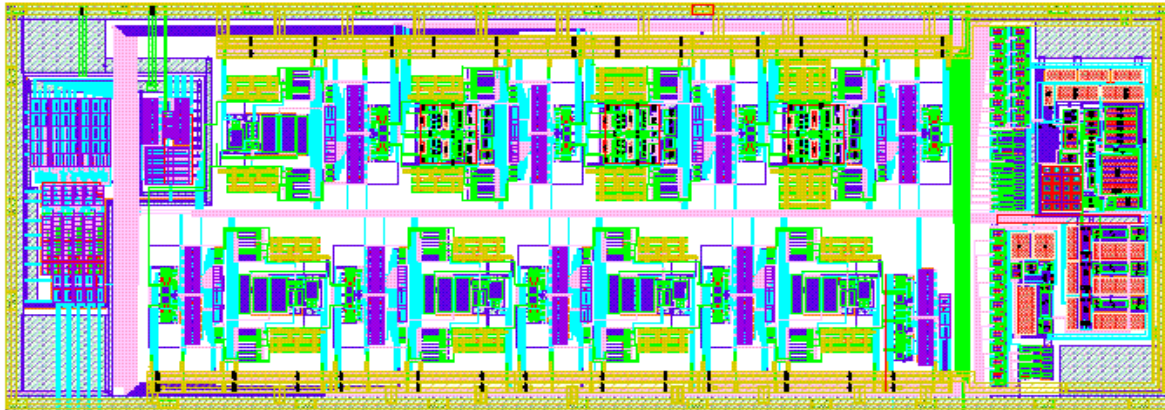
2-phase non overlapping clock scheme

Stage Monte Carlo analysis



Reproduced residue vs input characteristic of pipeline ADC stage after 50 Monte Carlo runs

ADC layout

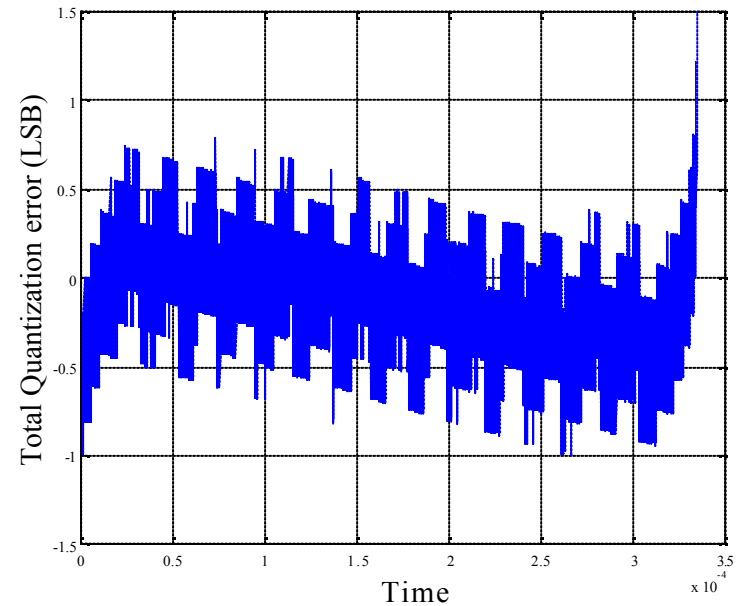
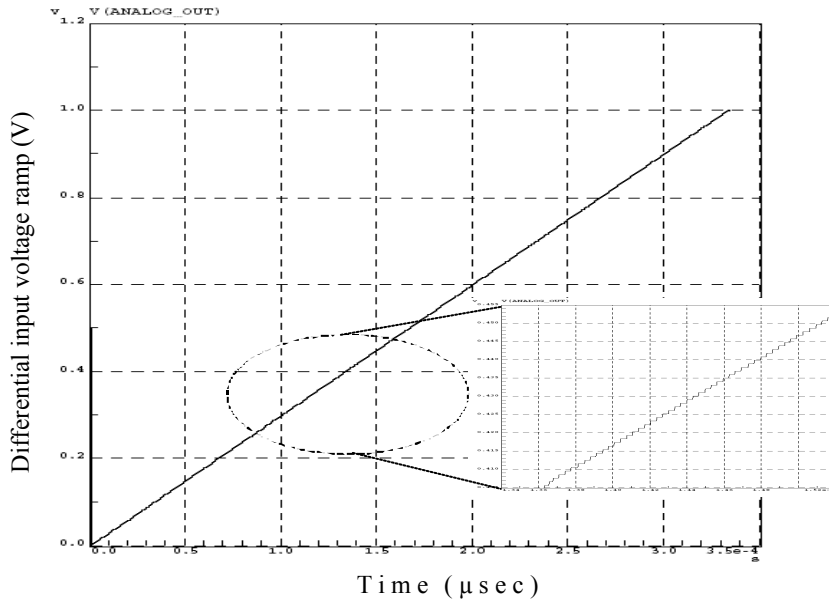




OUTLINE:

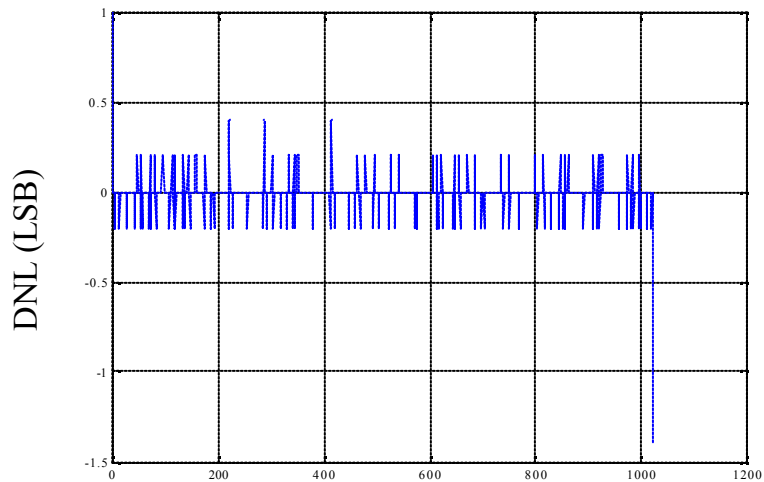
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Digitization of an input ramp signal

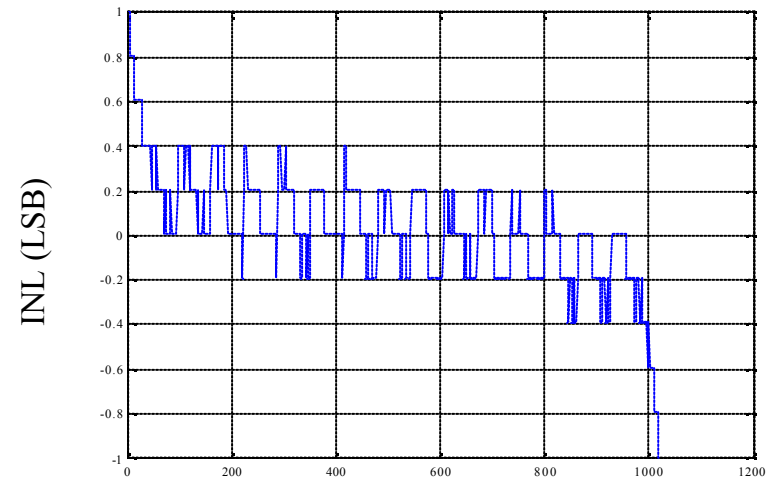


No missing codes, monotonic behavior.
 Total RMS noise=0.3870LSB -->SNDR>58db.

10b/15MHz ADC nonlinearities (DNL, INL)



Output codes

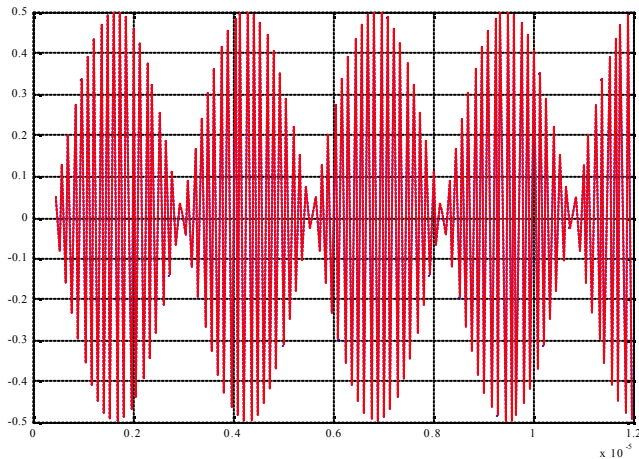


Output codes

DNL: +/- 0.4LSB, INL: +/-1LSB

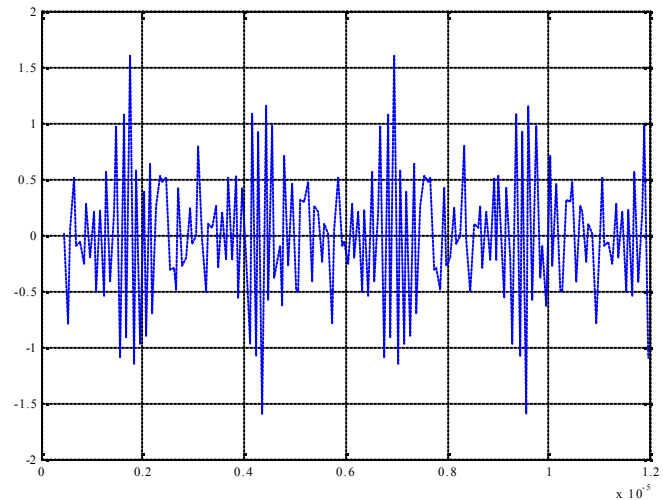
Digitization of 7.5MHz (Nyquist Frequency) sinusoidal input signal

Reconstructed output sinusoidal signal
(7.5MHz) and sampling (15MHz) points.



Time (sec)

Error from sinusoidal (7.5MHz)
digitization in LSBs



Time (X10⁻⁵) μsec

Total rms noise=0.5943LSB --> SNDR>55.7db
ENOB=8.96bits (@7.5MHz) (Nyquist frequency)

Performance summary

Parameter	Performance
Technology	0.25 μ m CMOS option of BiCMOS7
Power Supply	2.5V
Resolution	10bits
Sampling Frequency	15MHz
Architecture	Pipeline 9stages of 1.5bits per stage resolution
Input voltage	1.0Vpp differential
DC level	1.0V – 1.5V tunable
Amplifiers	Gain boosted folded cascode: DC gain>110db, GBW>80MHz (105C, slow)
Capacitors	MIM, scaled through the pipeline Cmax=0.3pF, Cmin=0.1pF.
Clocks	Two non-overlapping phases
Digital Error Correction	10bit look ahead adder
Differential NonLinearity (DNL)	+/- 0.4 LSB (105C, slow)
Integral NonLinearity (INL)	+/- 1 LSB (105C, slow)
Noise (rms value)	0.3870 LSB (@ low frequencies) 0.5943 LSB (@7.5MHz) (Nyquist frequency)
SNDR (signal to noise and distortion ratio)	>58db (@low frequencies) >55.7db (@7.5MHz) (Nyquist frequency)
ENOB (Effective number of bits)	9.5bits (@low frequencies) >8.96bits (@7.5MHz) (Nyquist frequency)
Total Current Consumption	~5.5mA @ 2.5V power supply. (Analog + digital blocks, without bandgap)
Estimated area	~0.15mm ² (Full analog + digital blocks + bandgap)



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- **A pipeline Analog/Digital Converter suitable for WCDMA/GSM operation for 3G mobile systems has been designed.**
- **The 1.5bit per stage resolution has been chosen for low power operation.**
- **Behavioral model analysis using ELDO macromodels have been performed for the extraction of the main design parameters.**
- **The 10bit/15MHz pipeline ADC has been designed with the BiCMOS7 library of ST Microelectronics.**



- **Extensive Monte Carlo analysis has been performed in order to optimize the ADC stage performance at the schematic and layout extracted levels.**
- **The pipeline ADC achieves ~8.9bits ENOB @ Nyquist frequency, +/- 0.4LSB DNL and +/-1 LSB INL for WCDMA operation (clock @ 15MHz).**
- **The pipeline ADC power consumption is ~13.5mW, with 2.5V power supply**
- **It occupies < 0.2mm² silicon area.**