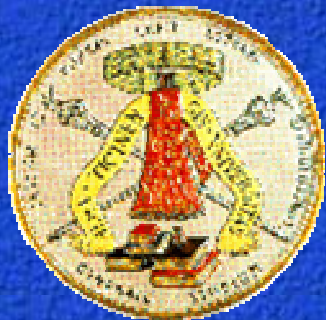


A Direct Conversion CMOS Receiver Front-End with on-chip LO for UMTS

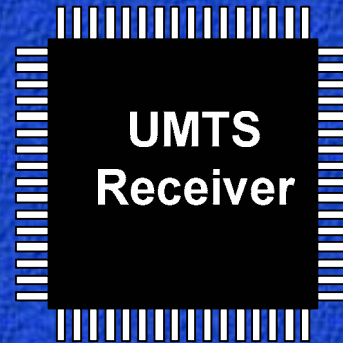
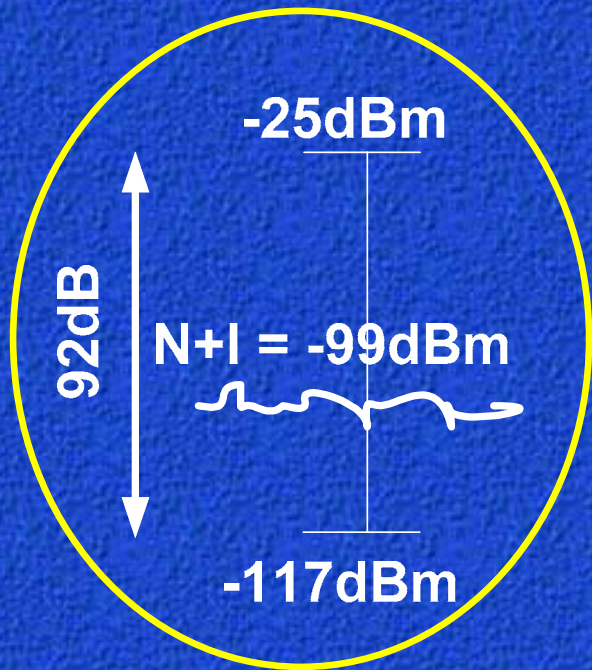
Francesco Svelto



Microelectronics Lab
University of Pavia, Pavia, Italy



Highly integrated, low power solution



Low Power

Low Cost

Few External Components

Direct conversion, adjacent channel Low-IF



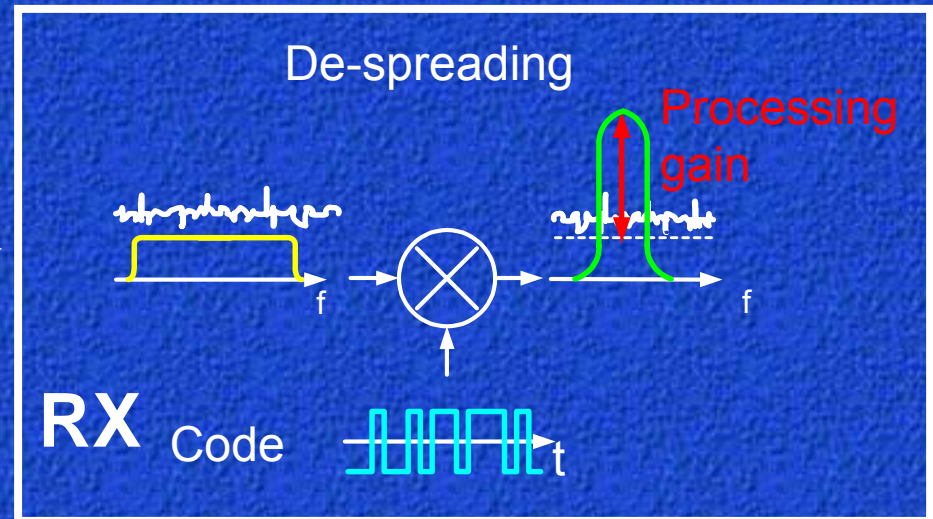
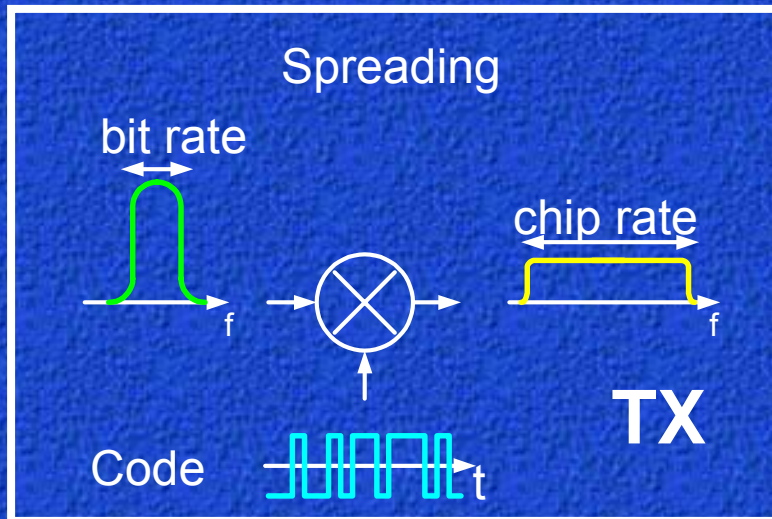
Both suffer from peculiar problems as $1/f$ noise and second order inter-modulation distortion

Presentation Outline

- Receiver Specifications
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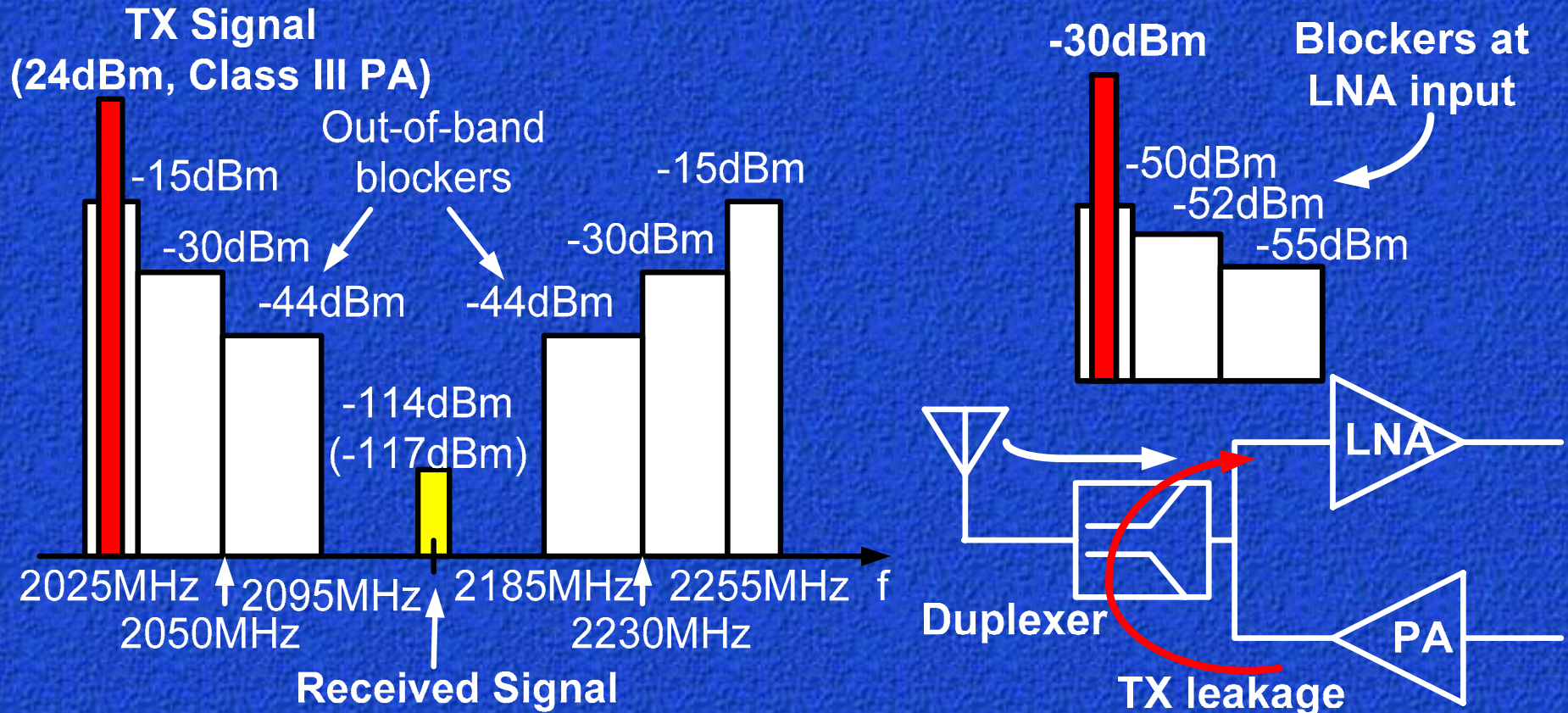
UMTS Terrestrial Radio Access

Direct Sequence Spread Spectrum



- Duplexing:
 - Uplink: FDD (full duplex) 1920-1980MHz
 - Downlink: 2110-2170MHz
- Variable Bit Rate: 8 / 384 kbps
- Chip Rate: 3.84Mcps
- Modulation: QPSK

Out-of-band Blocking



Transmitter leakage (-30dBm) dominates out-of-band blockers and determines out-of-band IIP3 and IIP2 requirements.

Sensitivity test

Tests conditions

- Bit Rate 12.2kbps
- Chip Rate (B) 3.84MHz
- BER 10^{-3}
- Minimum Signal -117dBm

Processing Gain

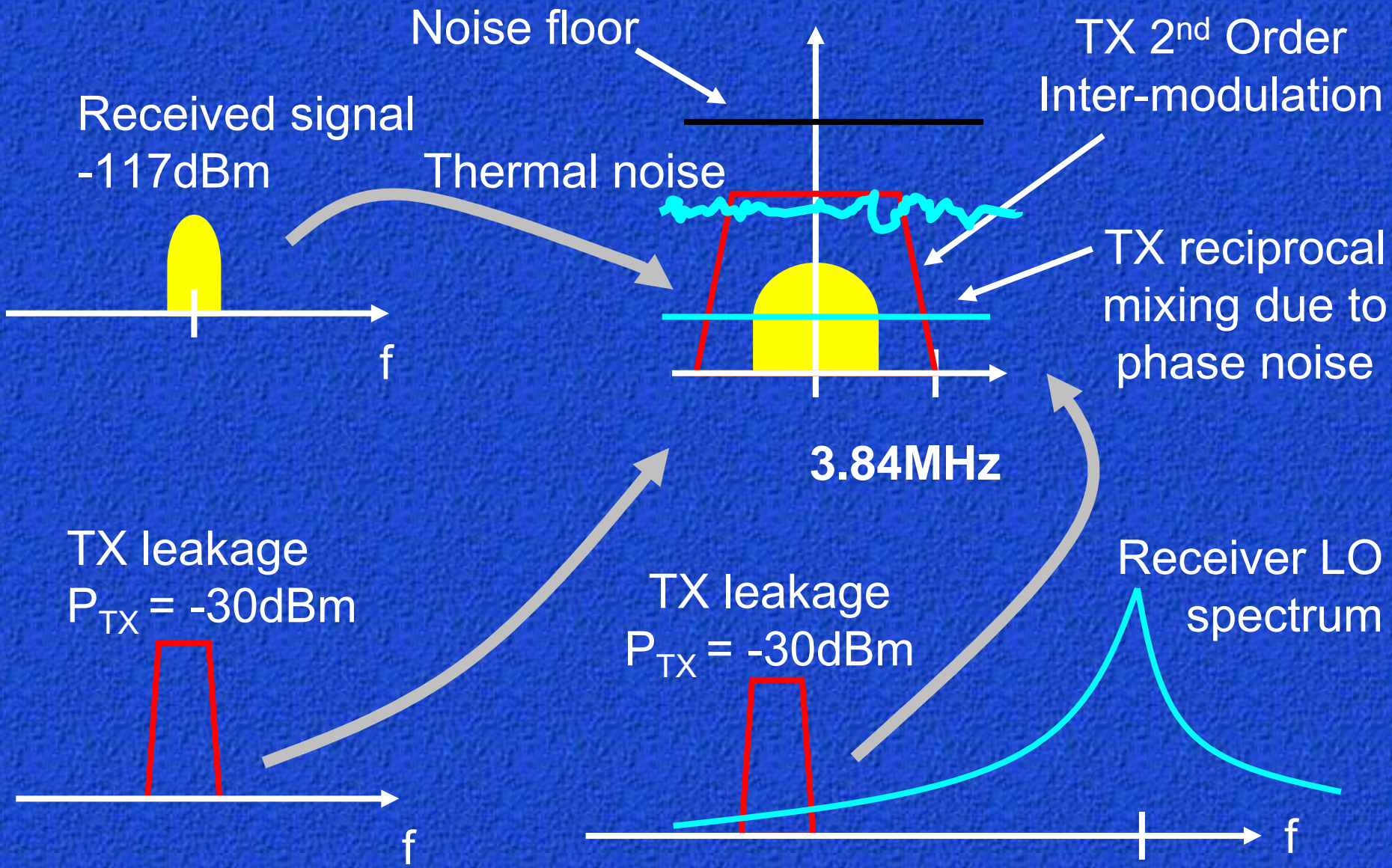
$$G_P = \frac{\text{ChipRate}}{\text{BitRate}} = 25\text{dB}$$

$$E_b / N_0 = 7\text{dB}$$

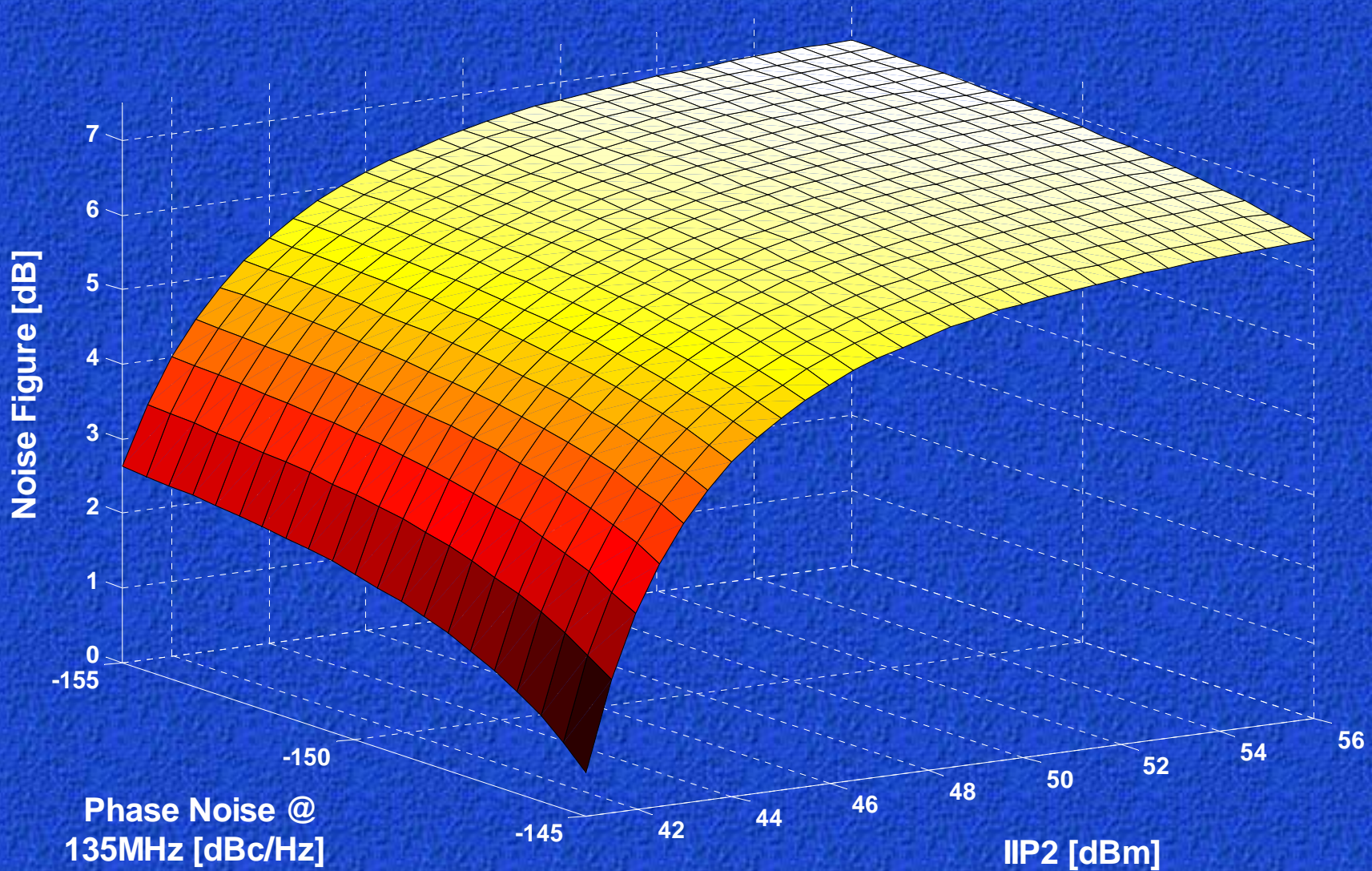
$$\text{SNR}_{\text{ANALOG}} = E_b / N_0 - G_P = -18\text{dB}$$

$$\text{Noise Floor} = \text{Min. Signal} - \text{SNR}_{\text{ANALOG}} = -99\text{dBm}$$

Desensitization due to TX leakage

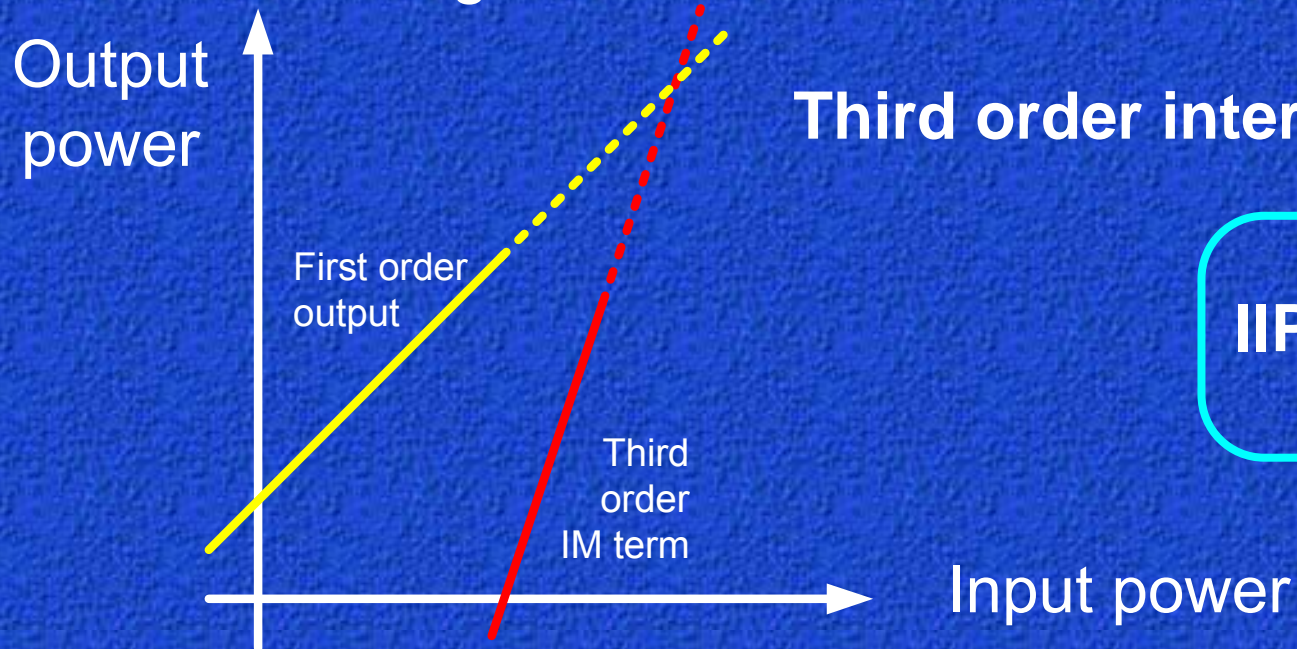
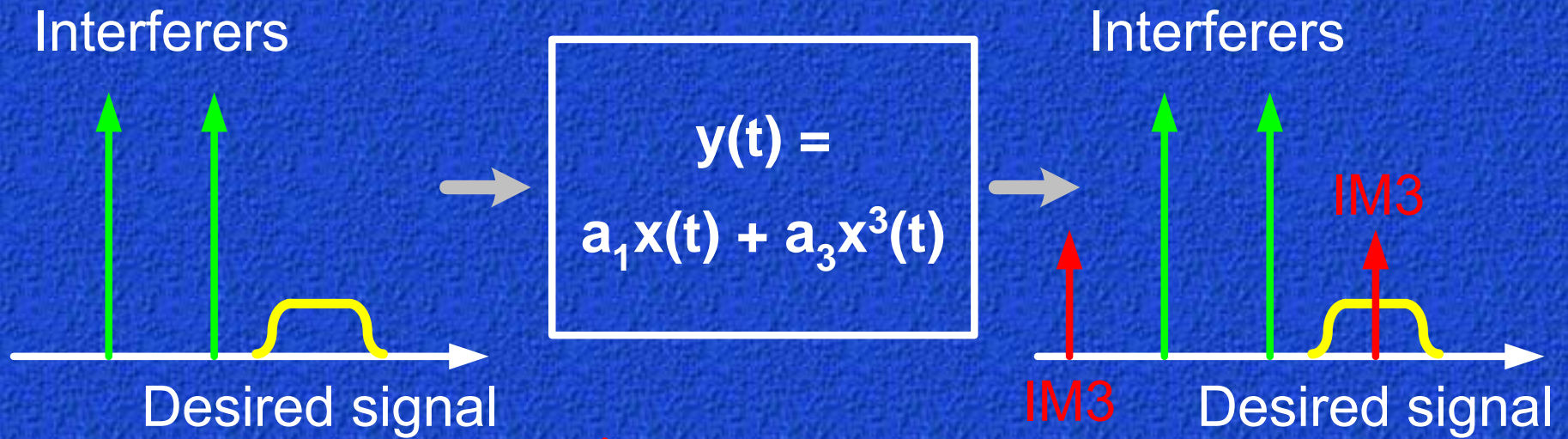


Receiver design trade-off



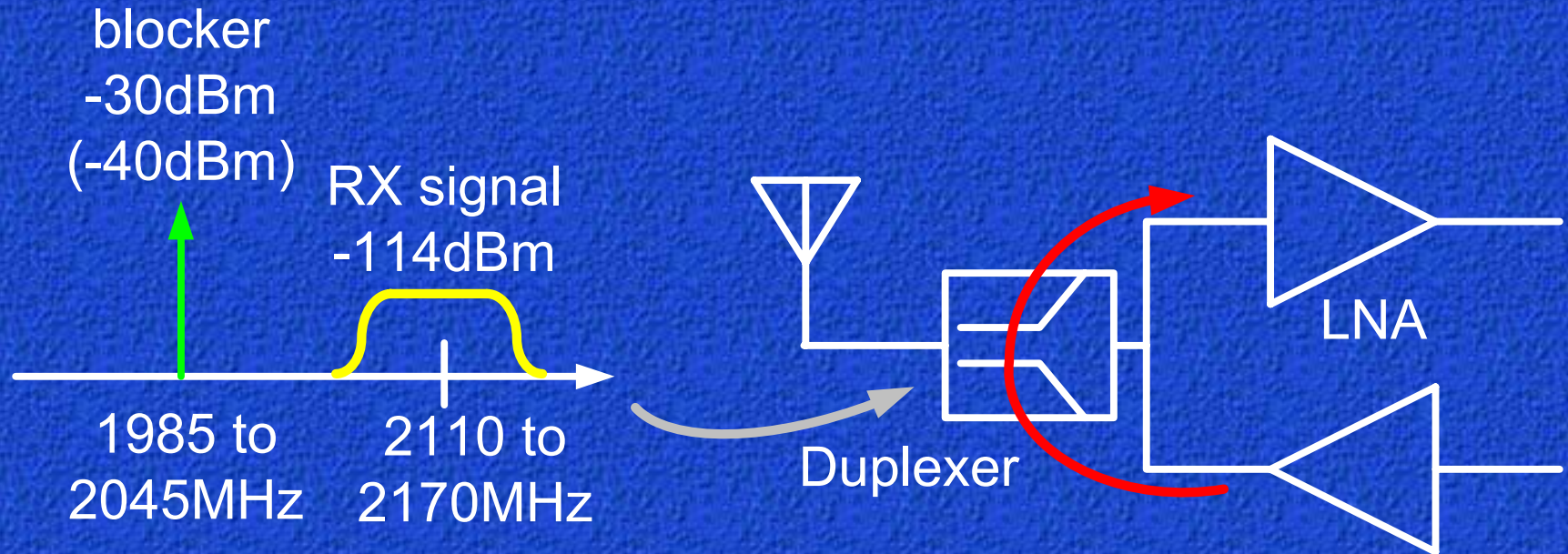
Noise + IM2 + $P_{\text{rec mix}} < -99\text{dBm}$

IIP3: basic concept



$$IIP3 = \frac{2}{3} \left| \frac{a_1}{a_3} \right| \frac{1}{R_s}$$

Out of band IIP3 Requirements

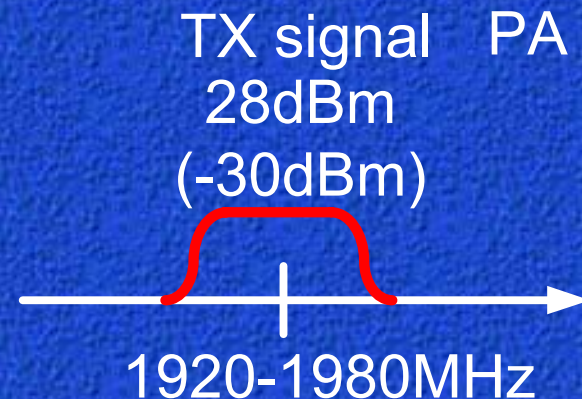


$$IM3 = 2P_{\text{blocker}} + P_{\text{TX}} - 2 IIP3$$



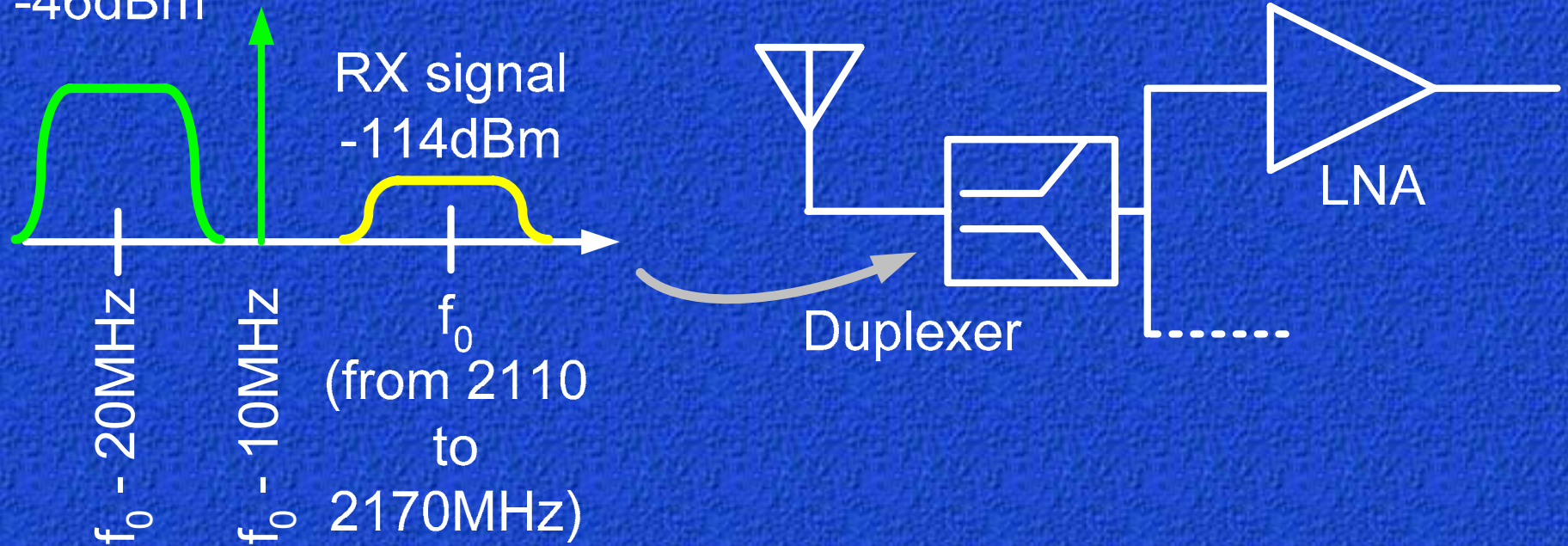
$$IIP3_{\text{out-of-band}} = -4.6\text{dBm}$$

(antenna referred)

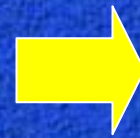


In band IIP3 Requirements

In band blockers
-46dBm



$$IM3 = 2P_{\text{blocker}} + P_{\text{TX}} - 2 \text{IIP3}$$



IIP3 in-band = -17dBm
(antenna referred)

Receiver Requirements

Access Technique	DS-CDMA
Sensitivity	-117dBm
Channel Bandwidth	3.84MHz
Max Signal Level	-25dBm
Bit Rate	8/384 kbps
Modulation	QPSK
Receiver specs	
NF	< 6dB
PN@ 135MHz	< -150dBc/Hz
IIP3 out of band	> -6.4dBm
IIP3 in band	> -18.8dBm
IIP2	> 46dBm

$E_b/N_t = 7\text{dB}$
Processing Gain
25dB
 $N+I = -99\text{dBm}$

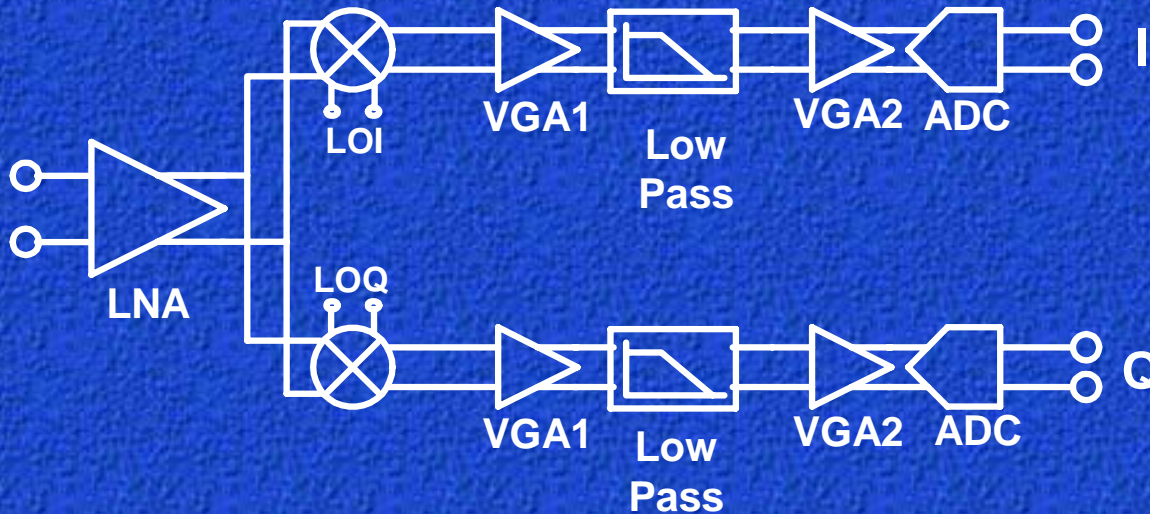


Receiver
Specifications

Presentation Outline

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Adjacent Channel Low-IF Architecture



RF section

	Gain	Noise	IIP3
LNA	16dB	2.5dBNF	-1dBm
Mixer	12dB	3.5nV/ $\sqrt{\text{Hz}}$	8dBm

- 10 bit A/D converter
- 6° order Butterworth LP filter

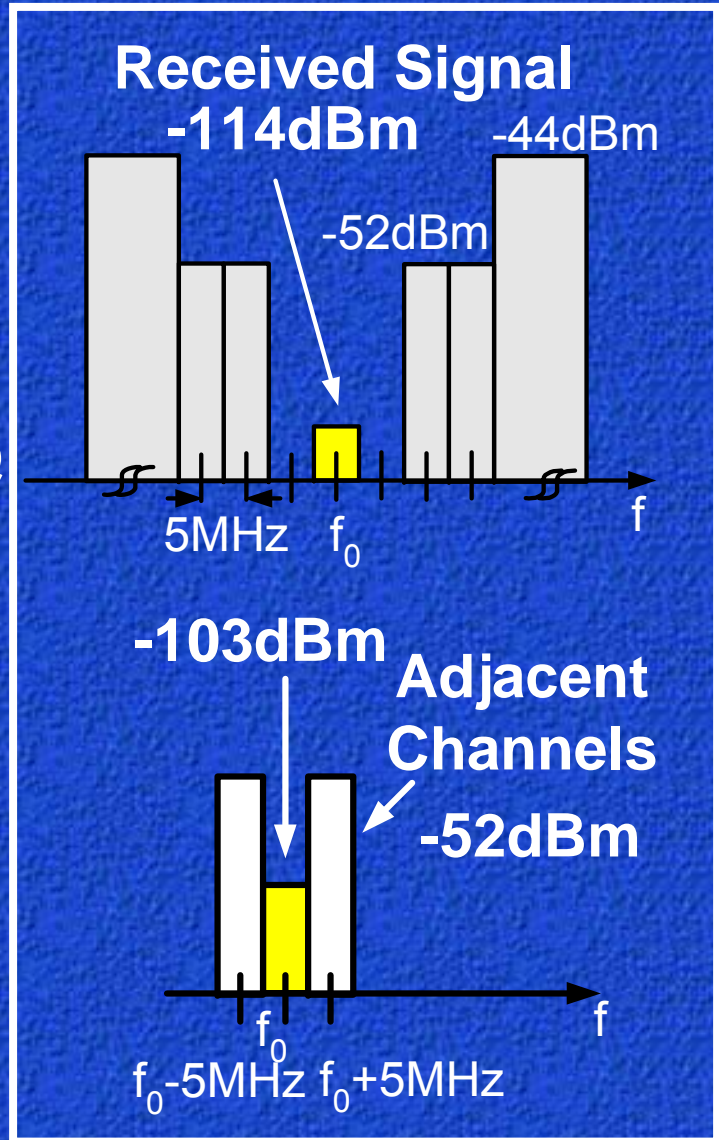
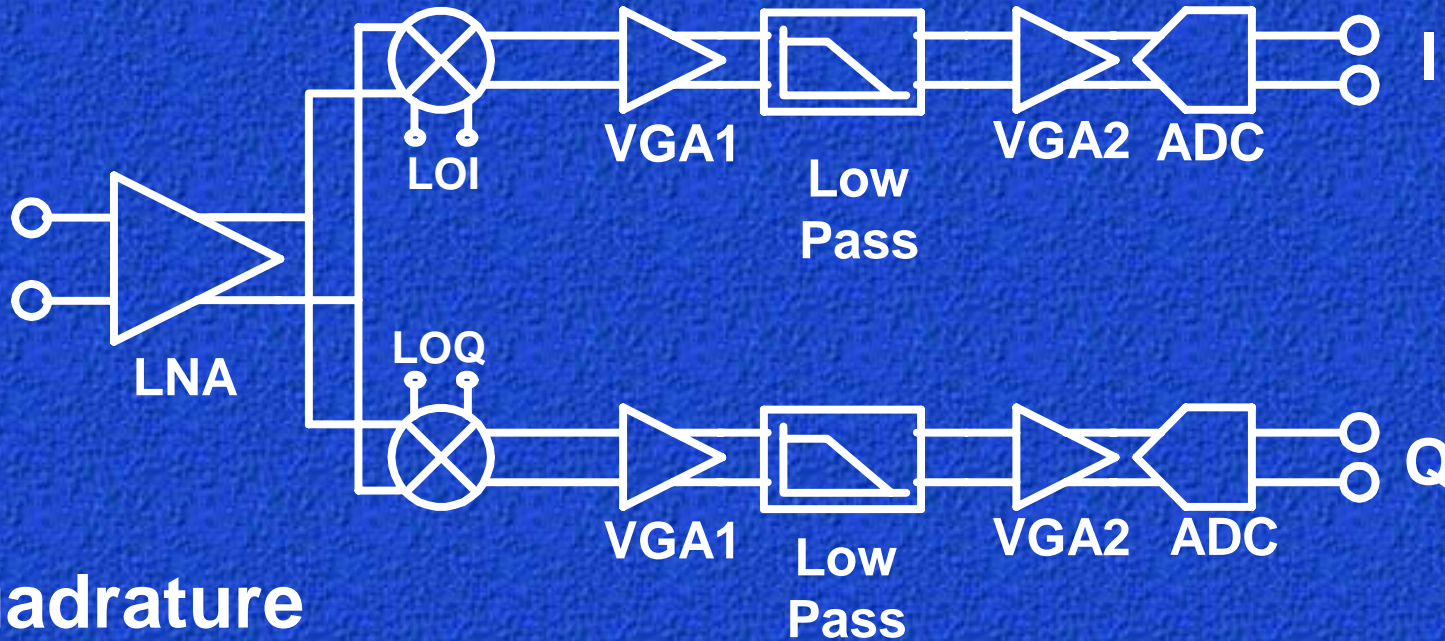


Image Rejection 33dB

Direct Conversion



Quadrature

Accuracy 23dB

- 6 bit A/D converter
- 4° order Butterworth LP filter

RF section

	Gain	Noise	IIP3
LNA	18dB	2.5dB/√Hz	-1dBm
Mixer	13dB	5nV/√Hz	10dBm

Architectures Comparison Conclusions

- **Adjacent Channel Low-IF and Direct Conversion:**
 - low image rejection requirements
 - suffer from second order inter-modulation
 - low phase noise at large frequency offset (135MHz)
- **Adjacent Channel Low-IF:**
 - high dynamic range requirements in IF circuitry and ADC

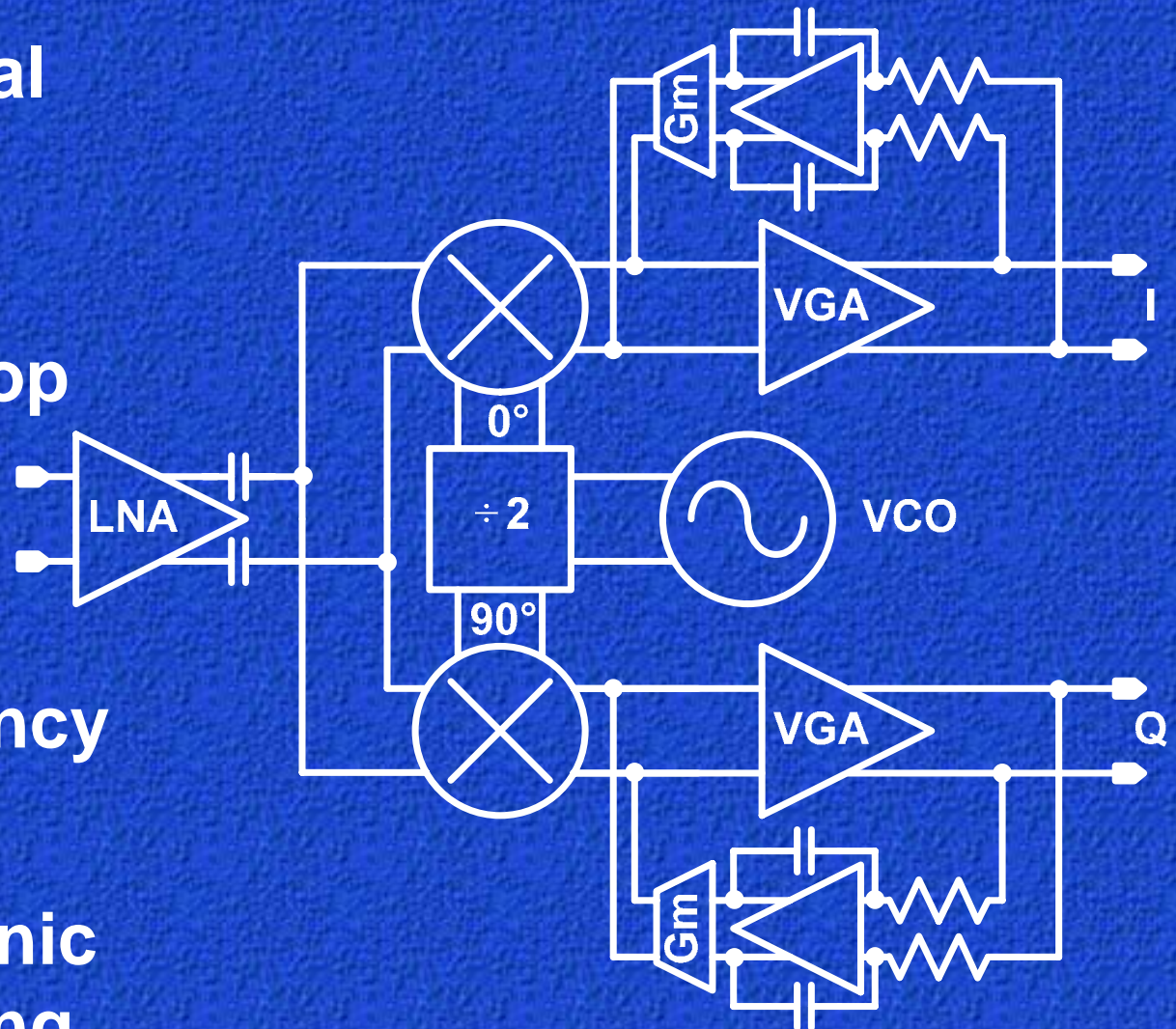
Direct conversion is the most suitable architecture for a UMTS receiver

Presentation Outline

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CMOS Direct Conversion front-end

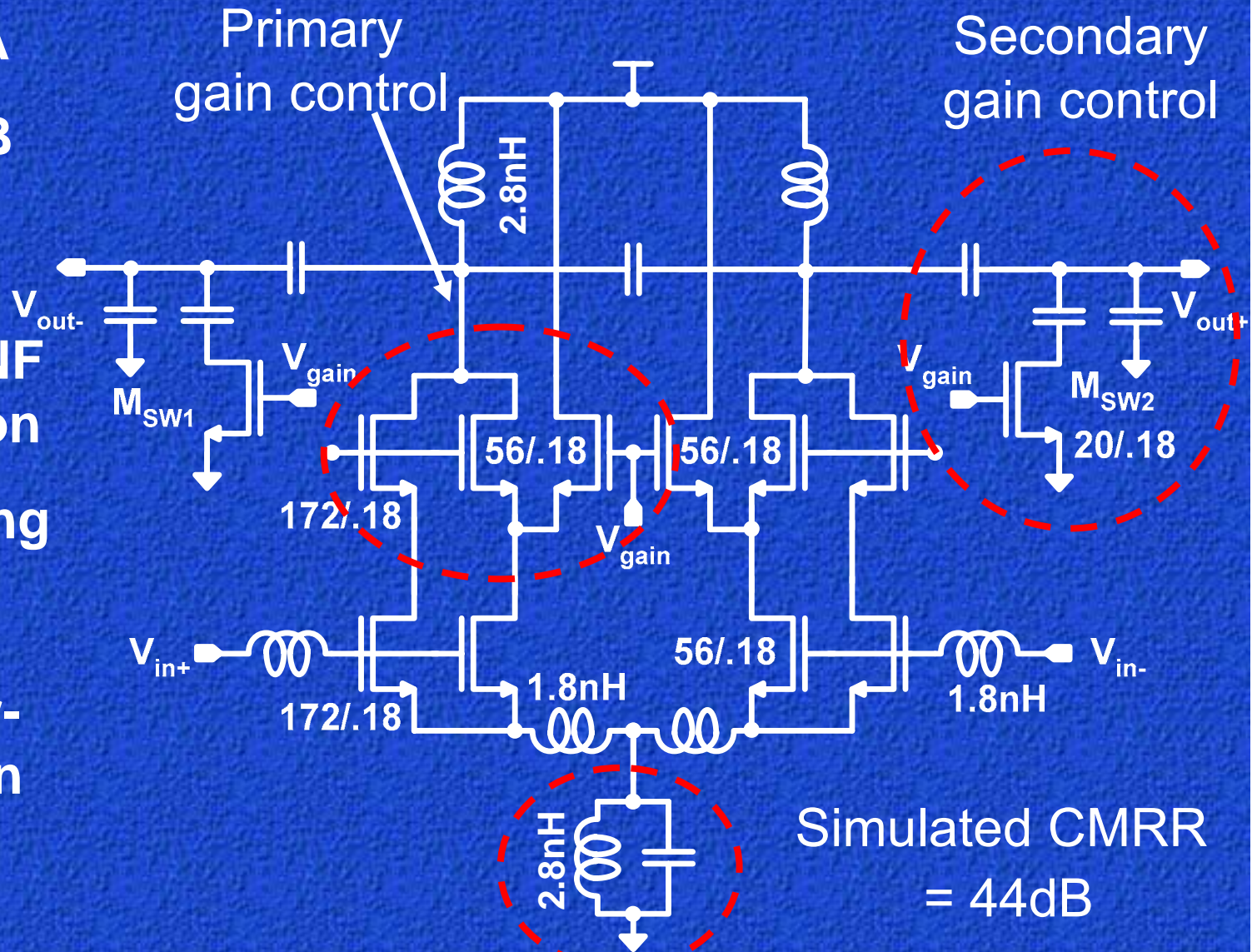
- Fully Differential Topology
- DC offset cancellation loop
- 0.18 μm CMOS Technology
- Double Frequency VCO
- Second-Harmonic Injection Locking Dividers



Servo-loop around the VGA implements a 3kHz high pass filter

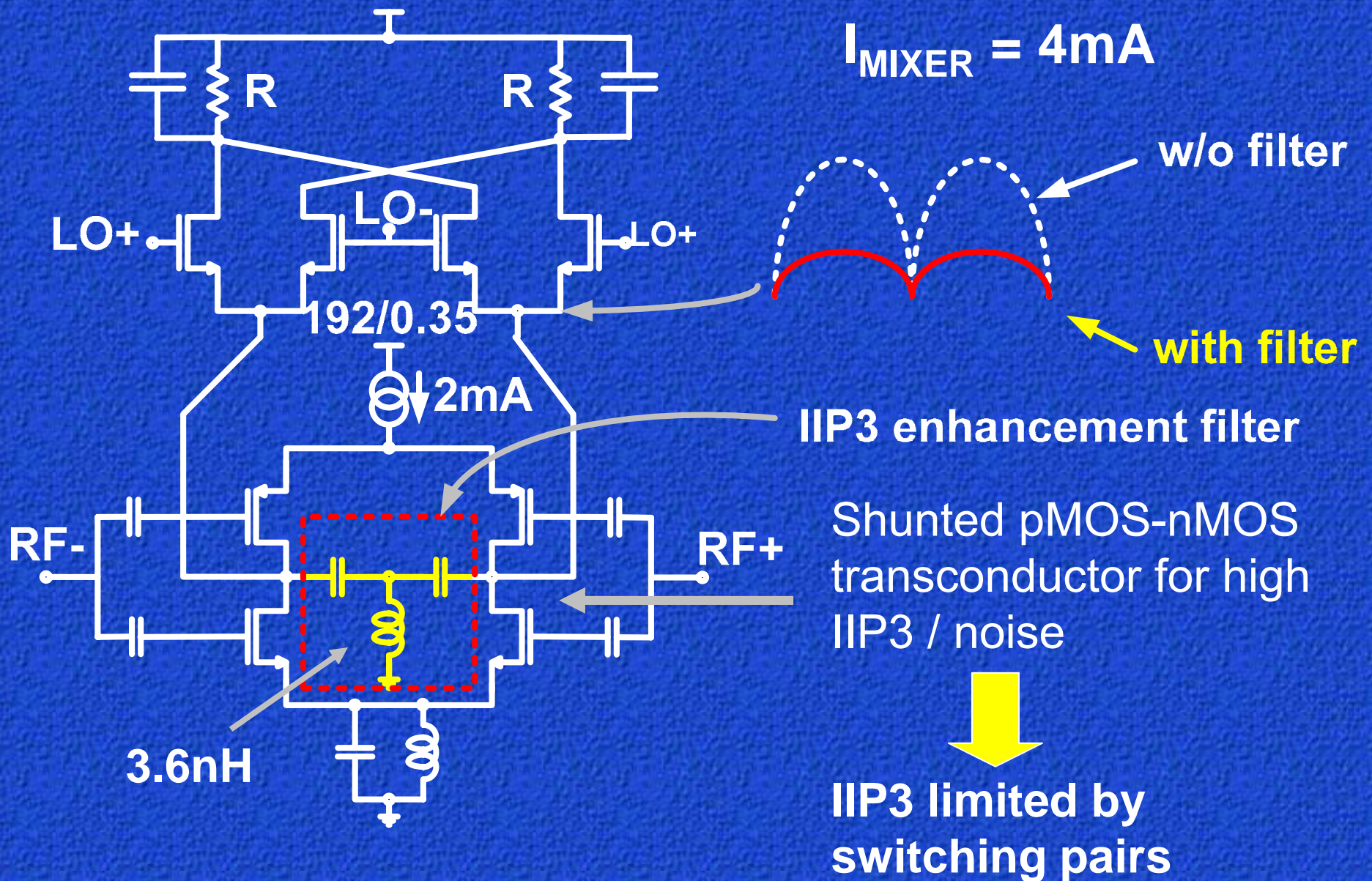
Low Noise Amplifier

- $I_{DISS} = 5\text{mA}$
- $NF = 2.5\text{dB}$
- 9dB gain variation with 1dB NF degradation
- AC coupling filters out second order inter-modulation products

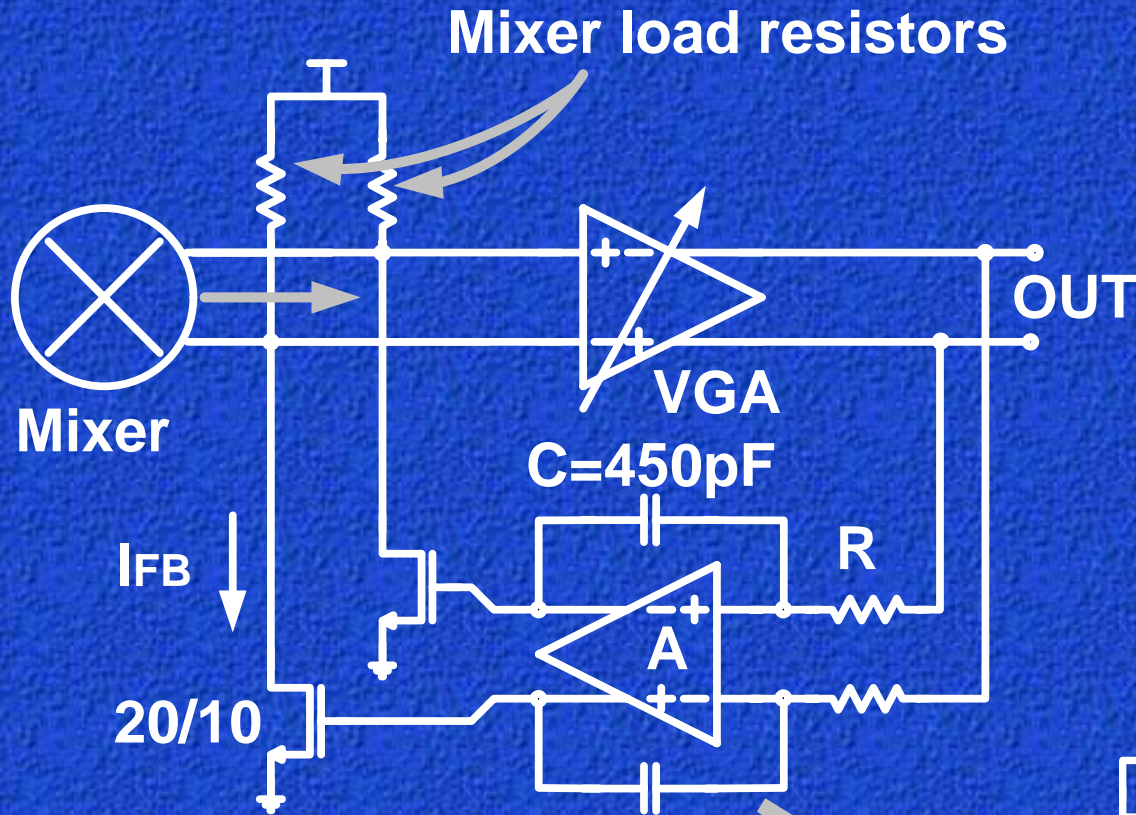


IIP3(LC) > Fully Differential (-8dBm)

Direct down-conversion mixer



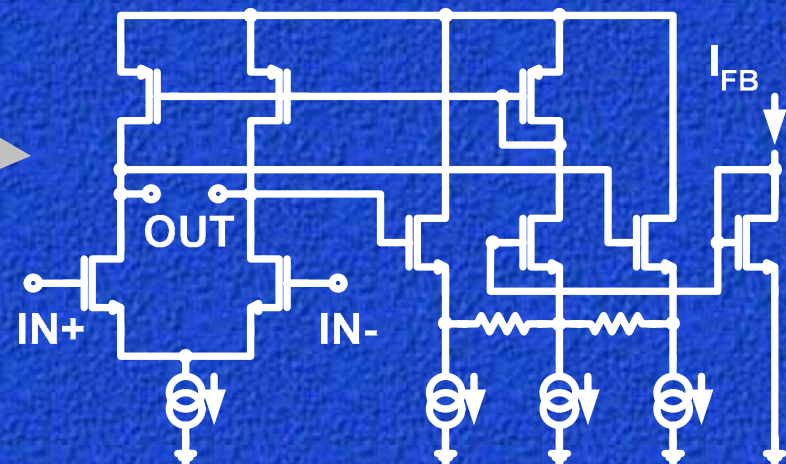
Offset-cancellation loop



C is realized on-chip with poly-well + metal-insulator-metal + lateral flux capacitors and occupies 0.1mm²

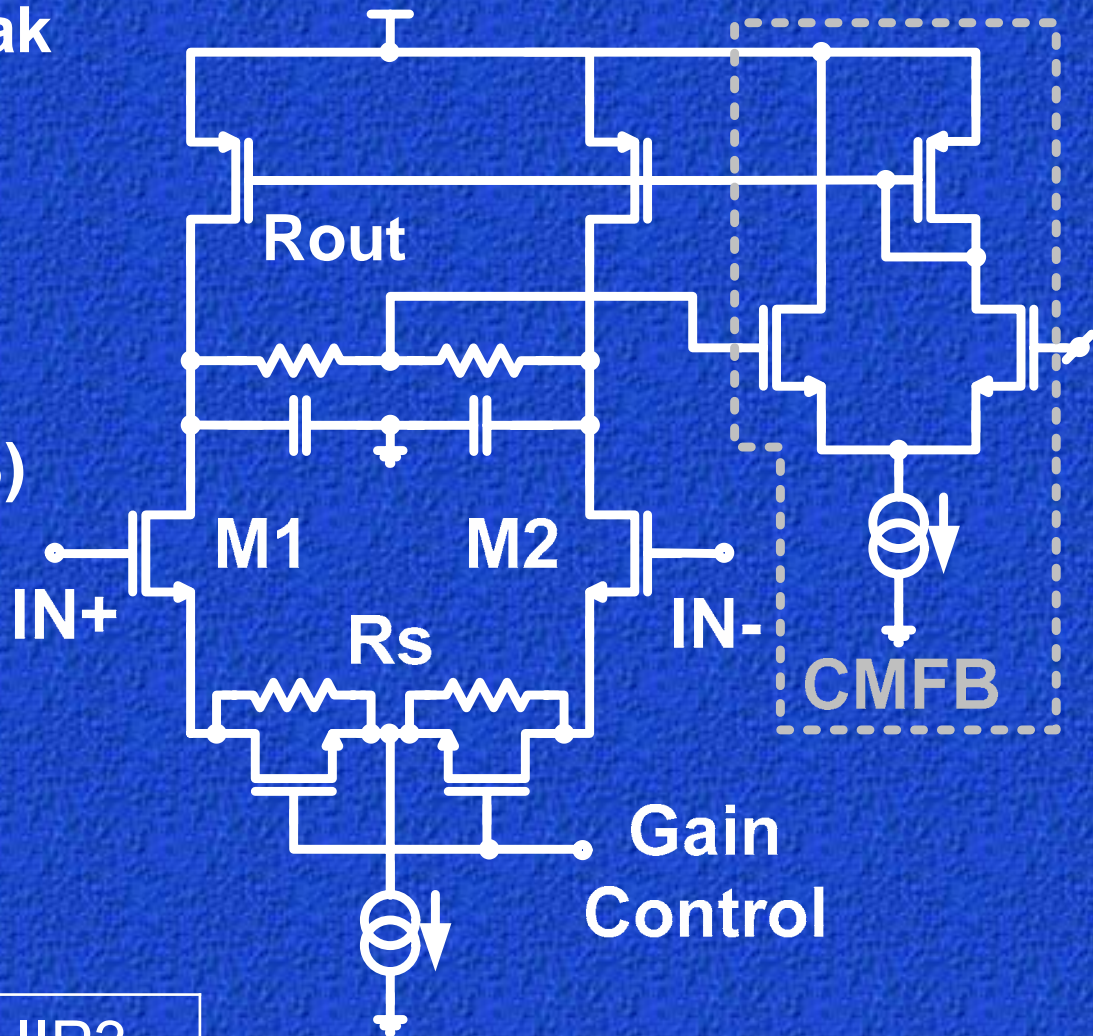
Transfer function

$$f_{hp} = \frac{G_{loop}(0)}{2\pi ARC}$$



Variable Gain Amplifier

- M1/2 operate in weak inversion to maximize g_m
- R_{out}/R_s sets minimum gain (0dB)
- Common mode feedback

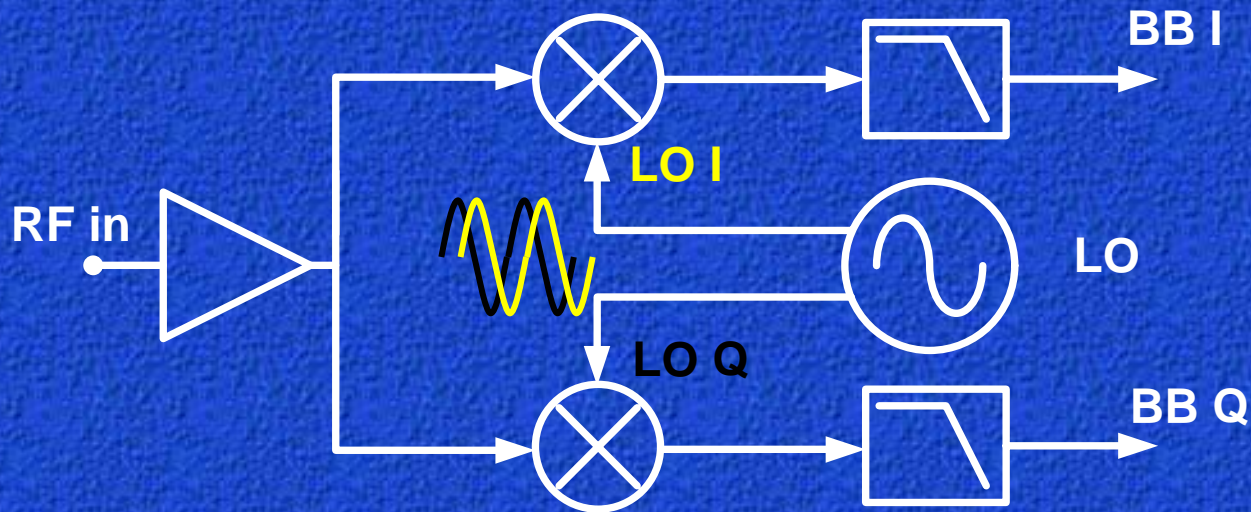


Design targets

Gain	Noise	IIP3
0-16dB	4nV/ $\sqrt{\text{Hz}}$	3dBm

$$I_{VGA} + I_{\text{Servo Loop}} = 1\text{mA}$$

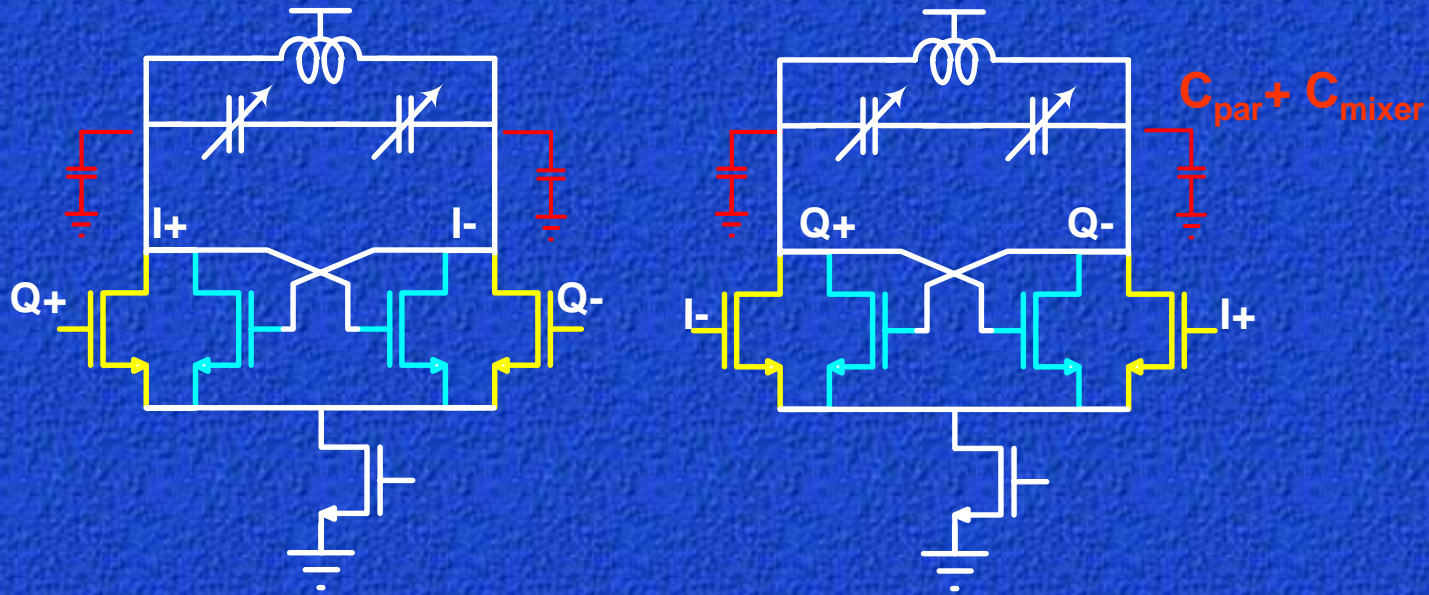
Local Oscillator Generation



- Low phase noise at large offset
- Large tuning range
- Minimum power consumption

while driving large mixer LO input capacitance

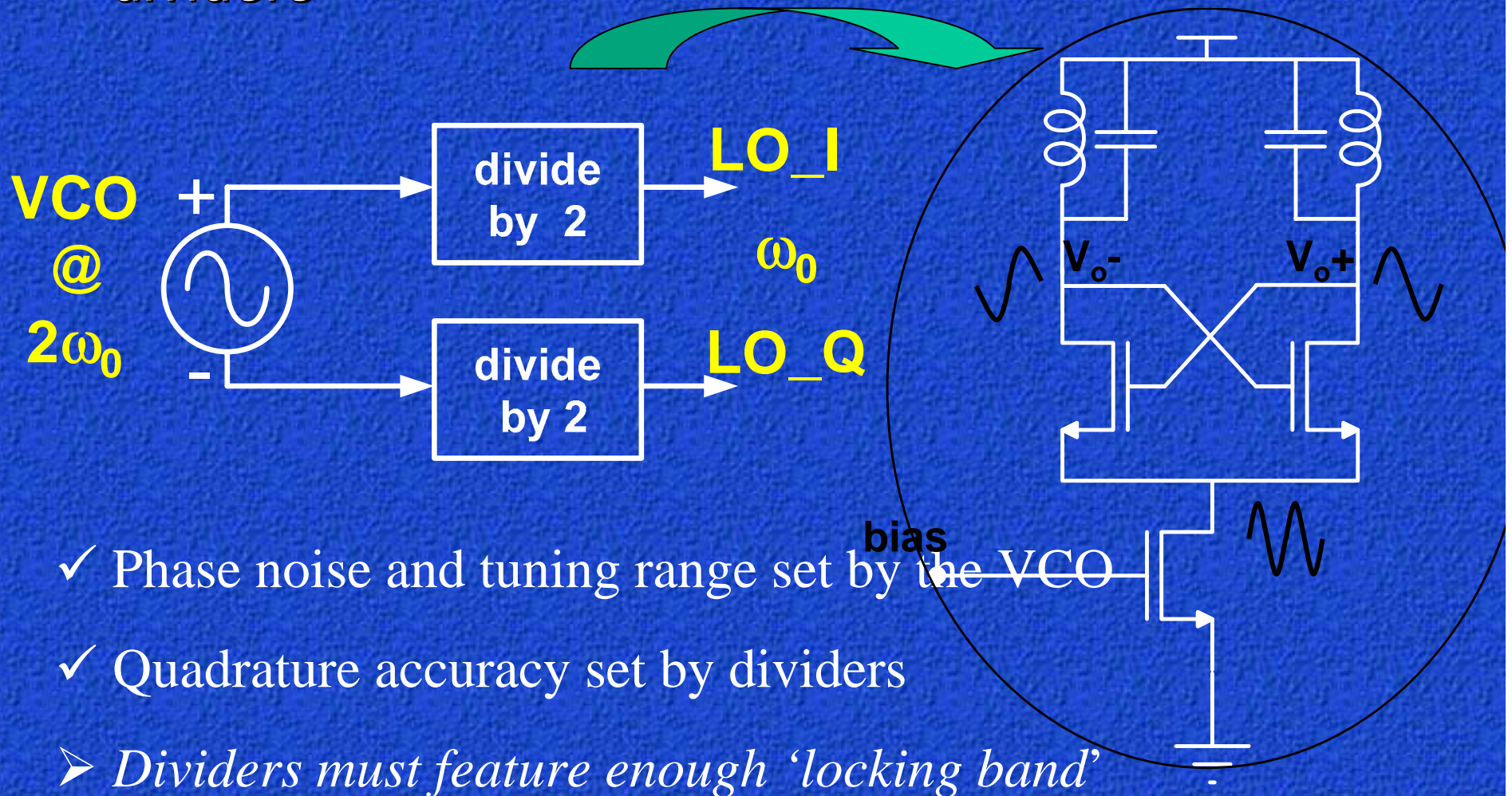
Coupled LC Oscillators



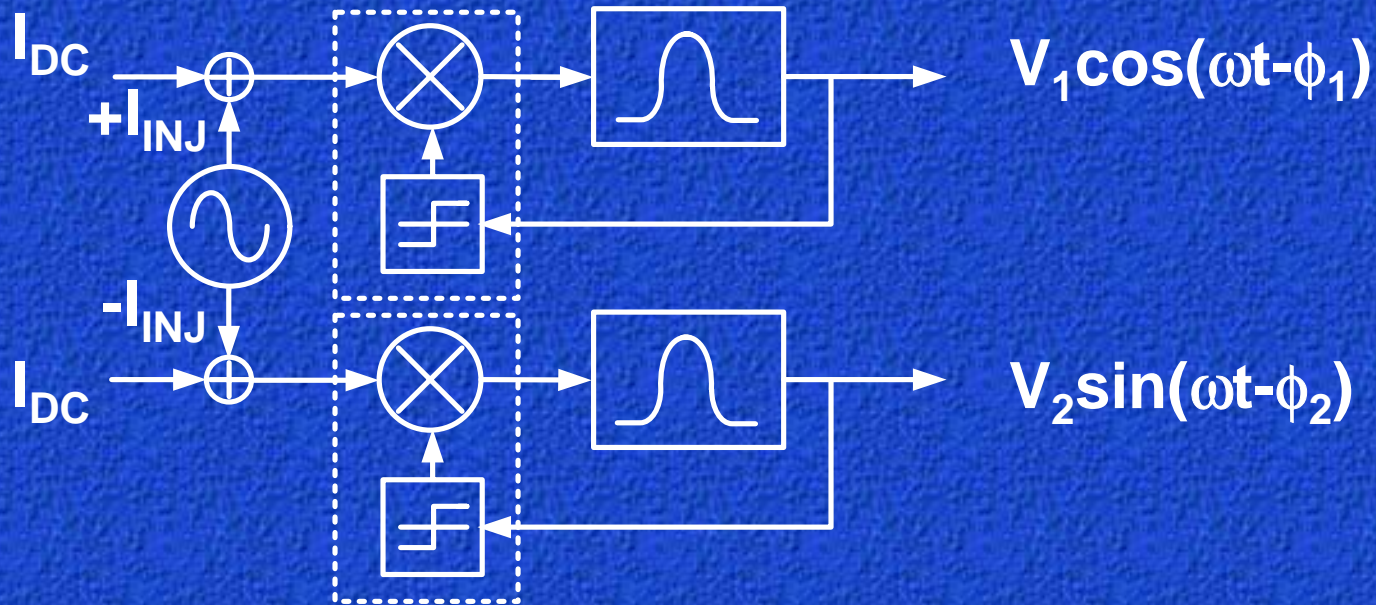
- ✓ Quadrature accuracy trades-off with phase noise
- ✓ Fixed capacitances reduce the available tuning range

Injection Locking Frequency Dividers

A VCO running at $2\omega_0$ drives two LC frequency dividers



Behavioral Model of LC Dividers

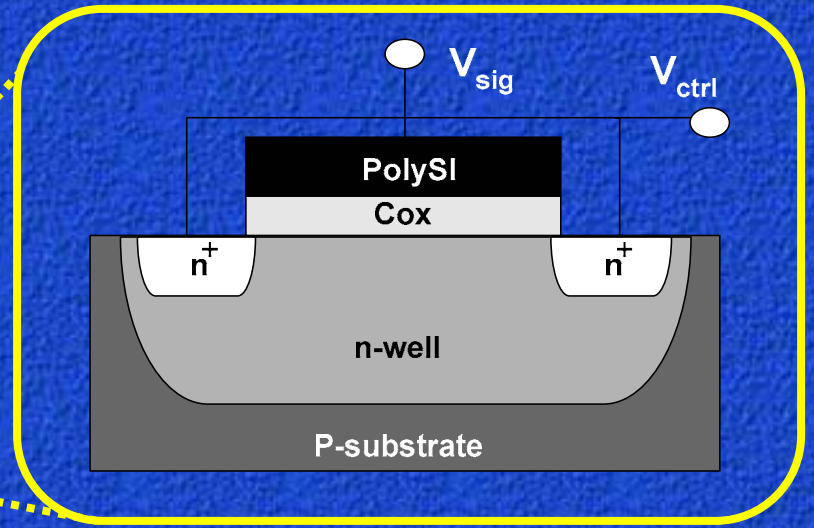
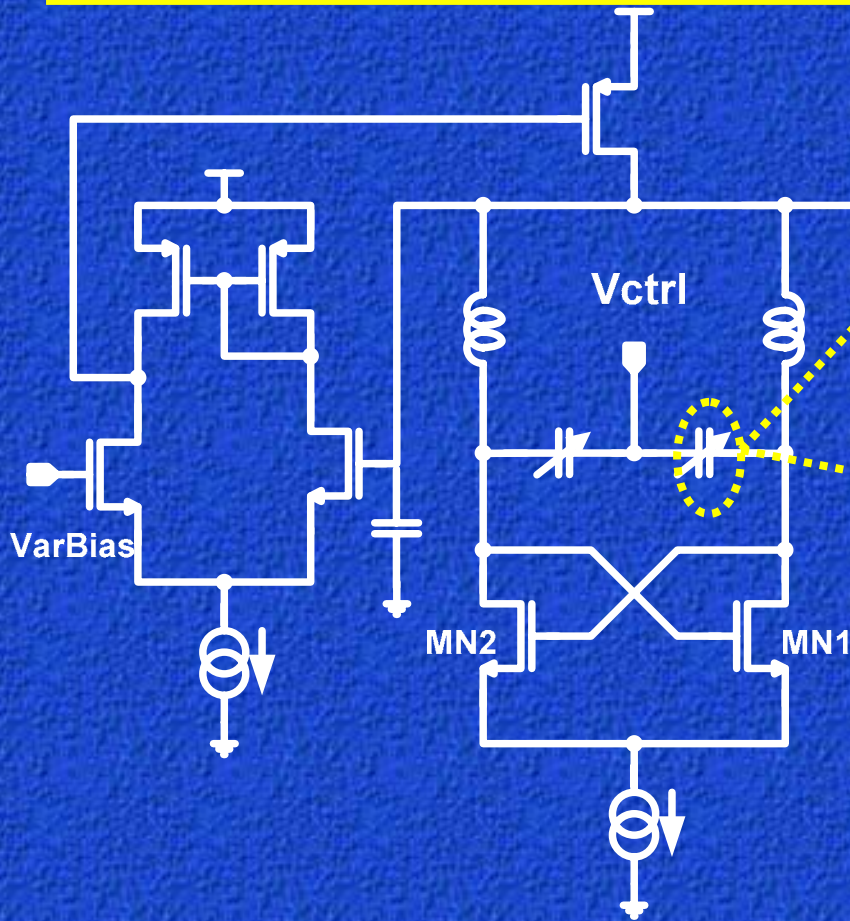


$$Ph_{dev} = Q \frac{X}{4} \left(\frac{3}{\left(\frac{I_{inj}}{I_{DC}} \right)} + 1 \right)$$

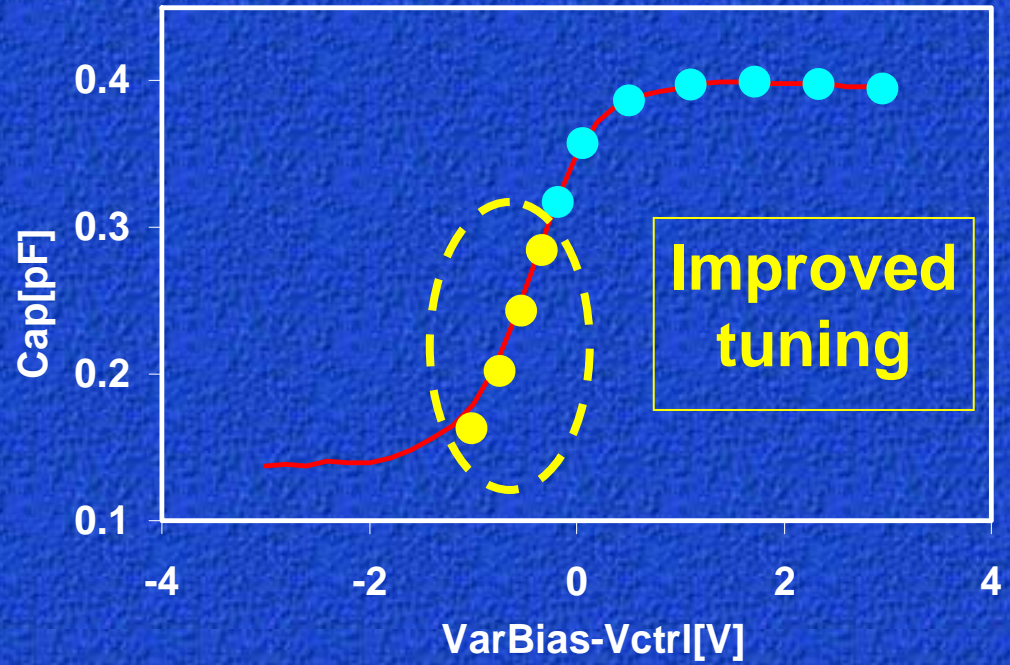
$$\frac{\Delta \omega}{\omega_0} = \frac{2}{3} \left(\frac{I_{inj}}{I_{DC}} \right) \frac{1}{Q}$$

Locking-range and phase accuracy improve
 reducing load Q and increasing injection ratio

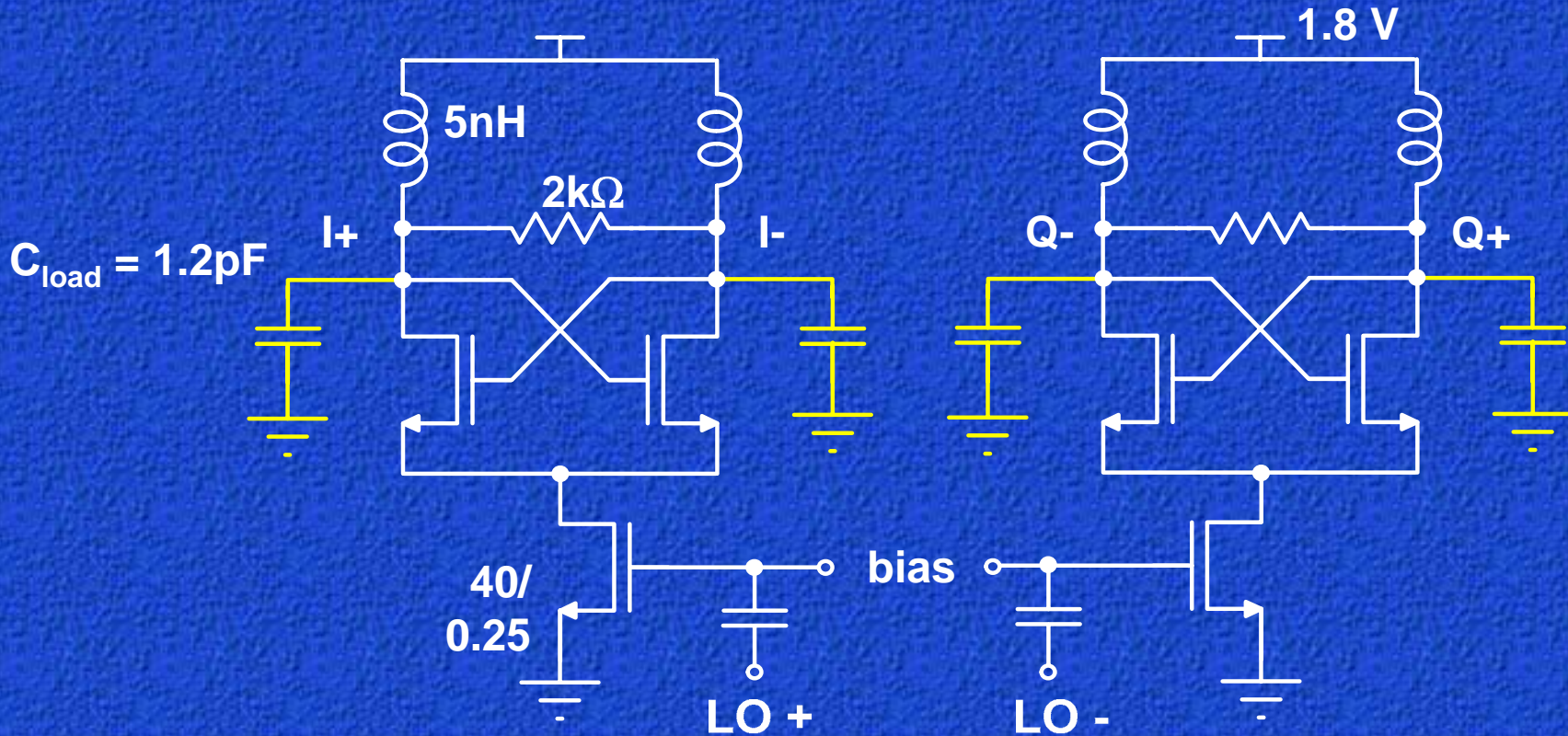
Double Frequency VCO



Separate supply voltage:
Improved tuning Range
Improved PSRR



Dividers Implementation

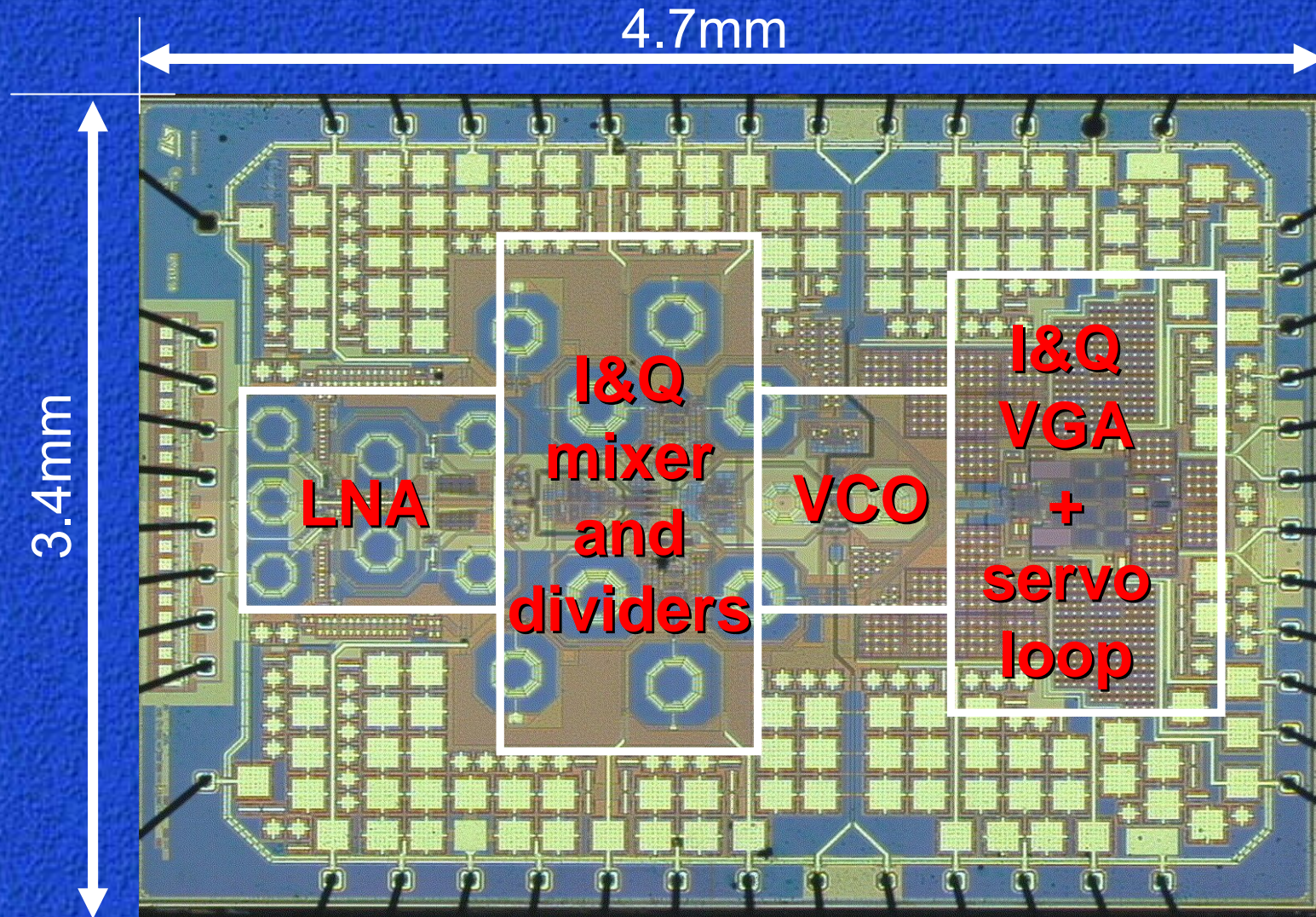


- ✓ Capacitive load: parasitic only
- ✓ Q lowered to 4 to keep a safety margin on quadrature error
- ✓ Input transconductor in subthreshold for maximum linearity

Presentation Outline

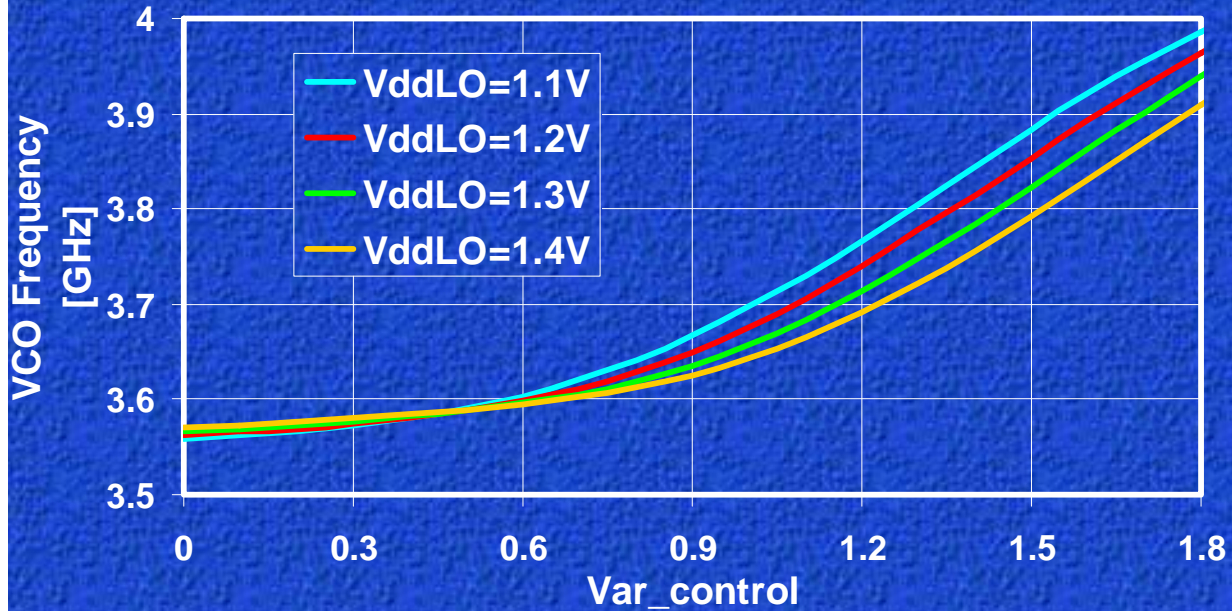
- Receiver Specifications
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Die Microphotograph



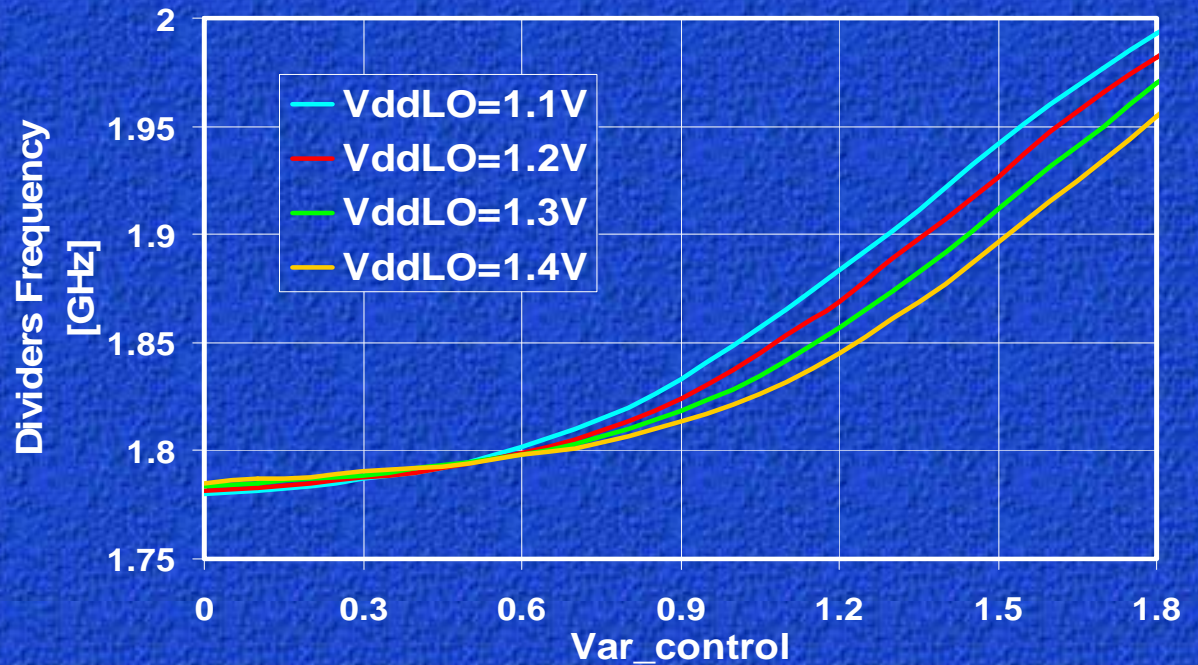
Total chip area = 16mm^2

VCO Tuning

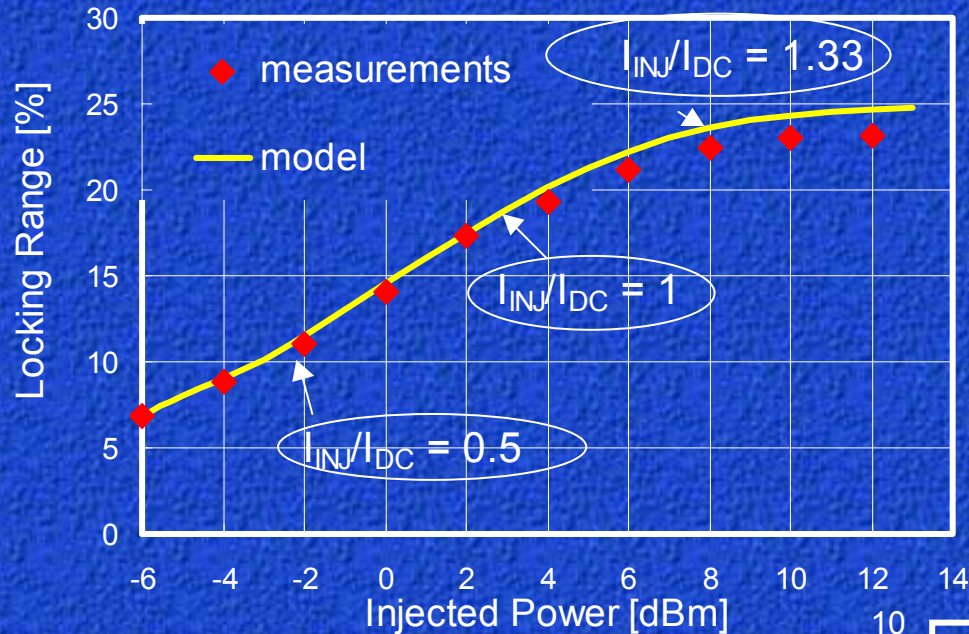


Lower
oscillation
frequency due
to LC load
variation

**Tuning Range
10.6%**

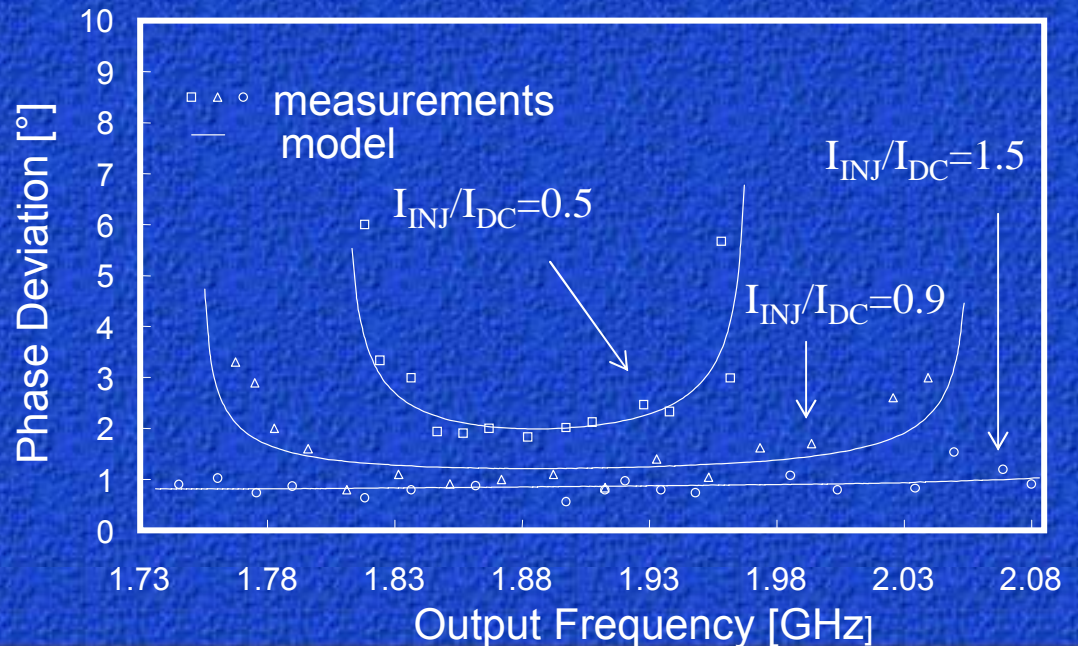


Locking range and Phase deviation

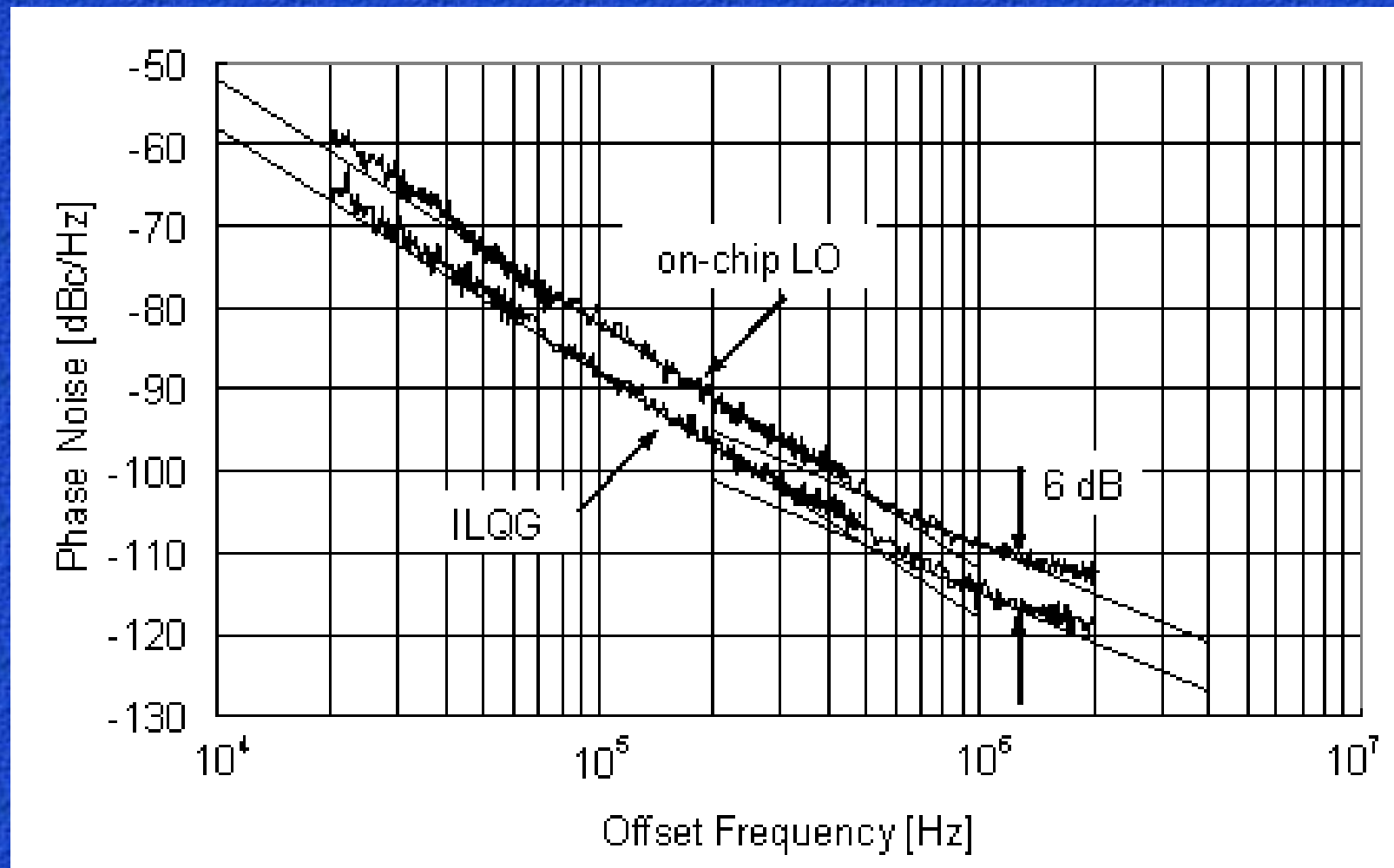


← Locking Range

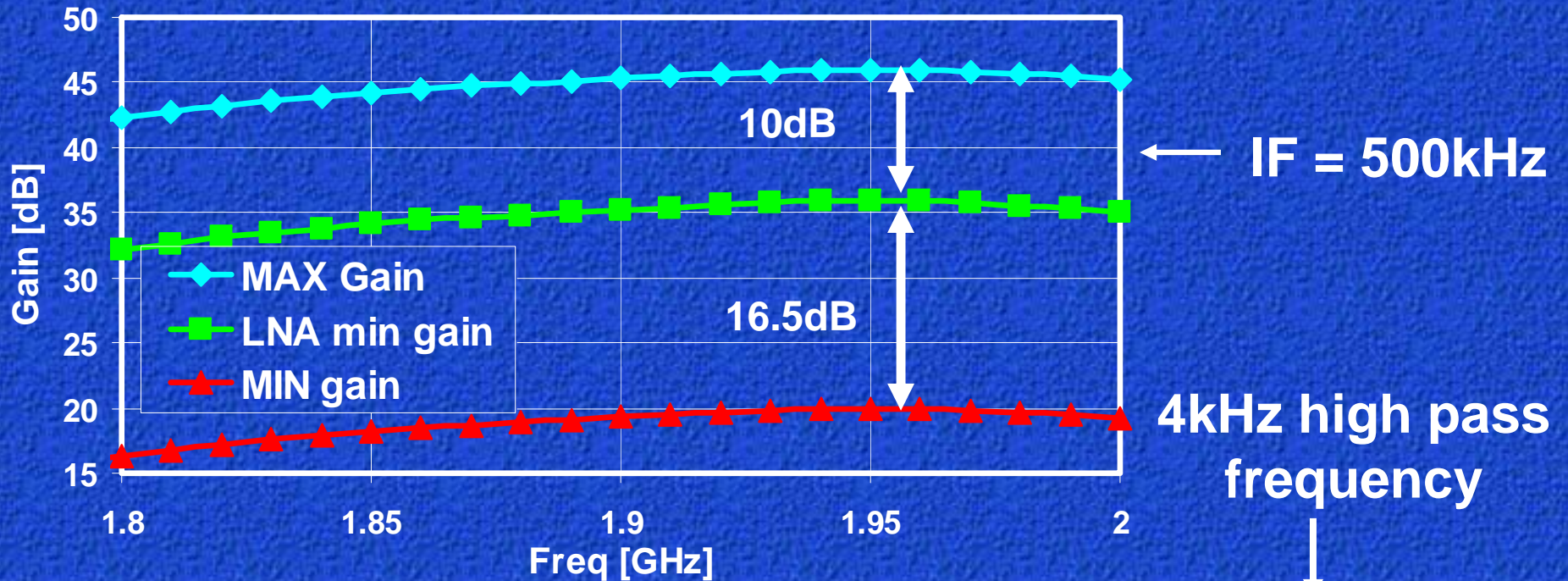
Phase Deviation →
(down-converted signals)



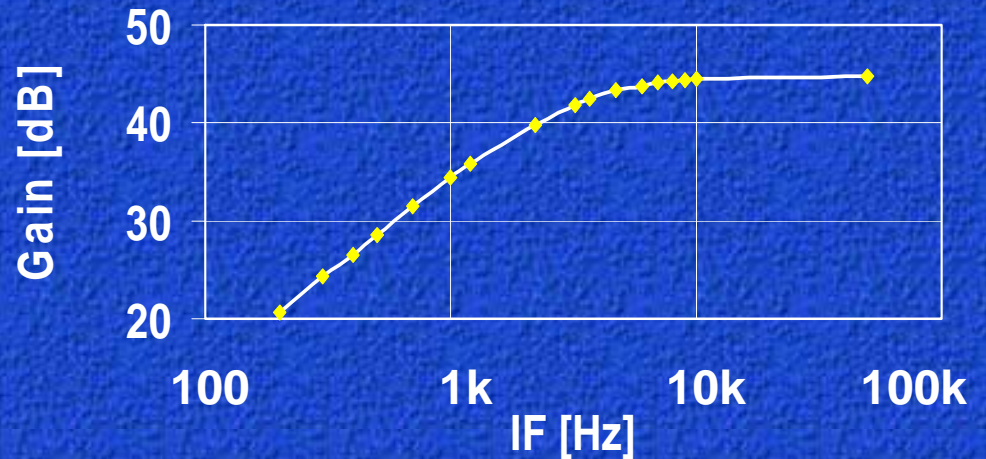
Phase Noise



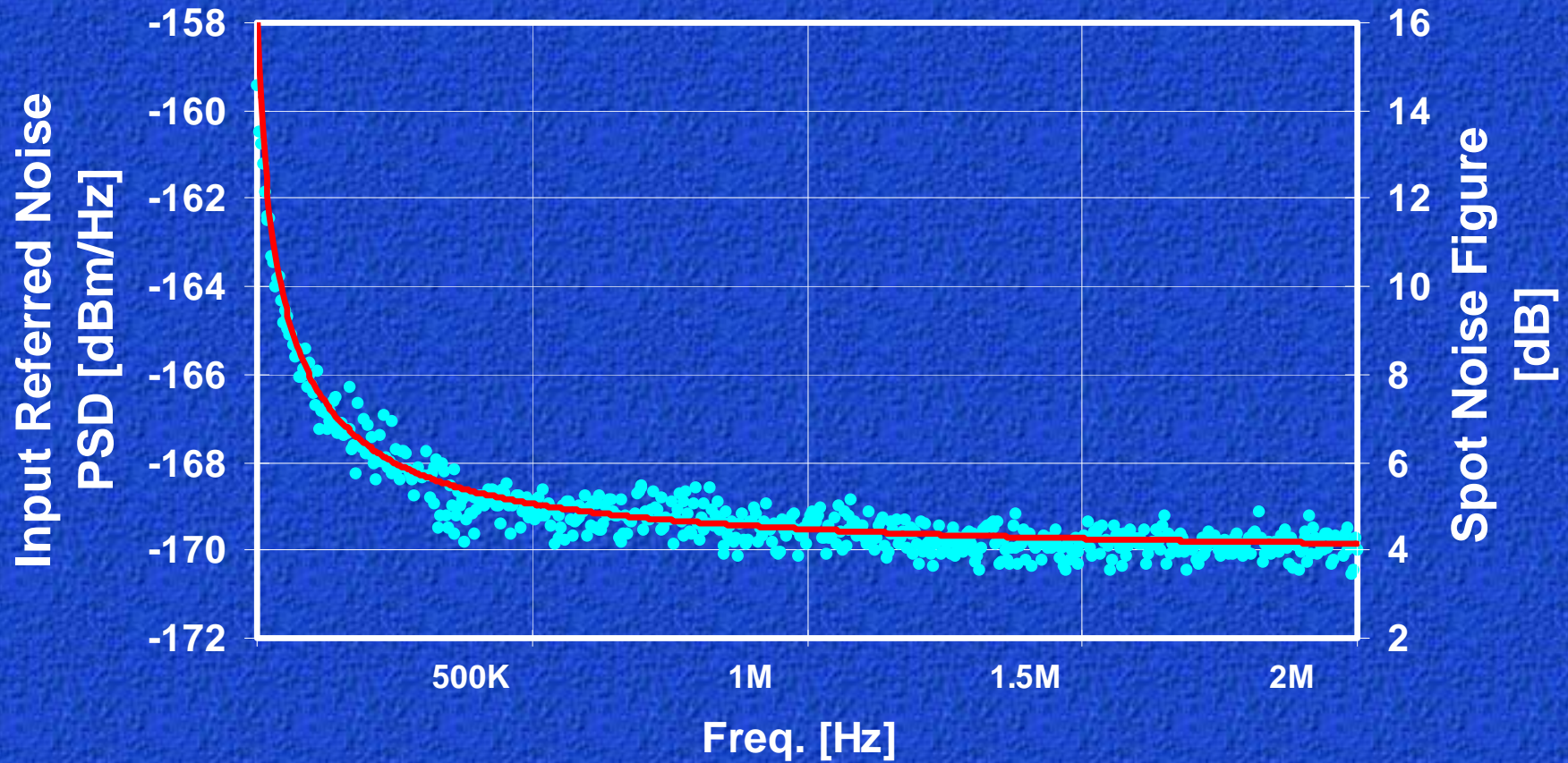
Receiver Gain Measurements



↑
Lower peak gain frequency due to LNA LC load variation (worst case condition)

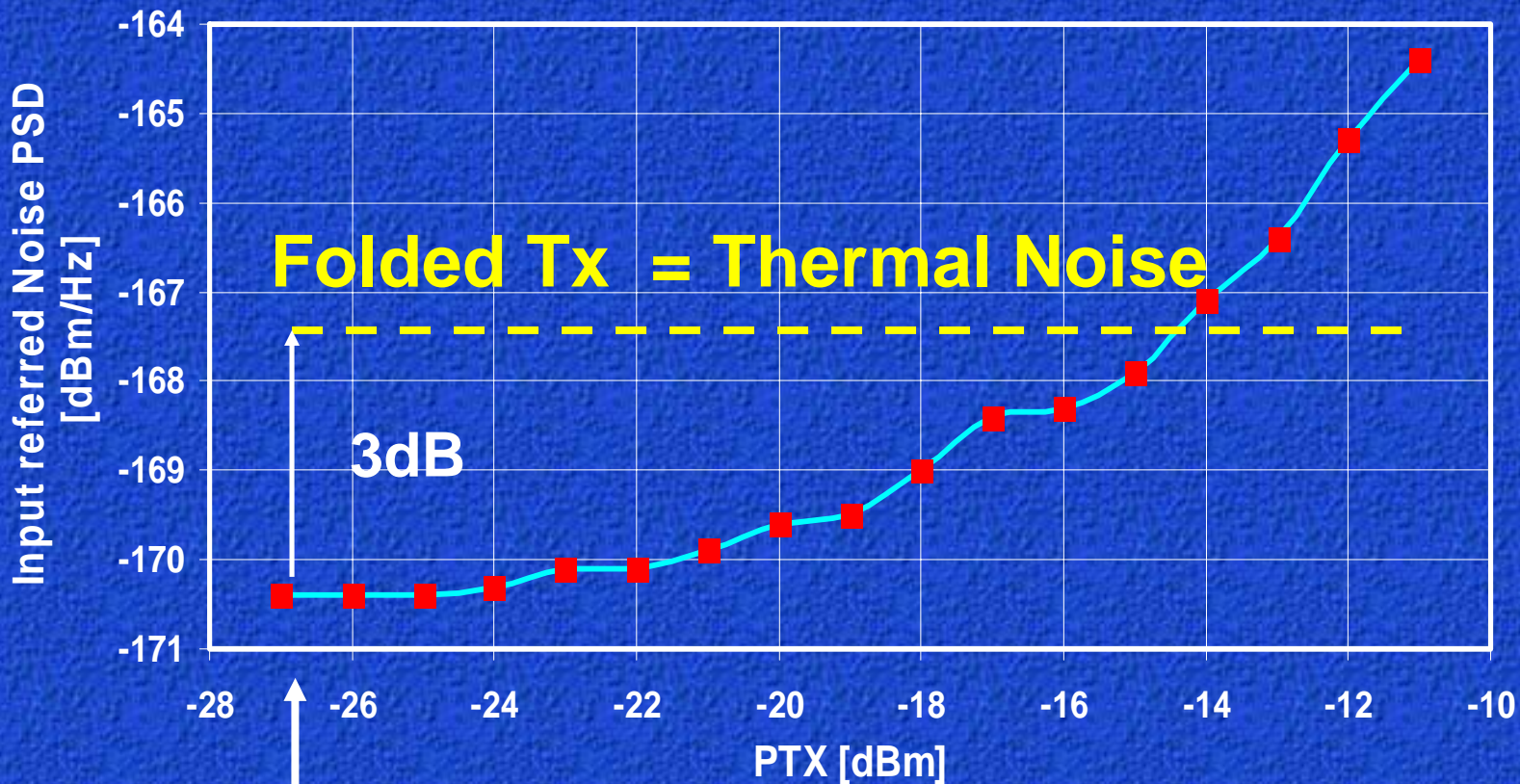


Noise



DSB-NF 5.6dB (10kHz-1.92MHz)

Reciprocal mixing

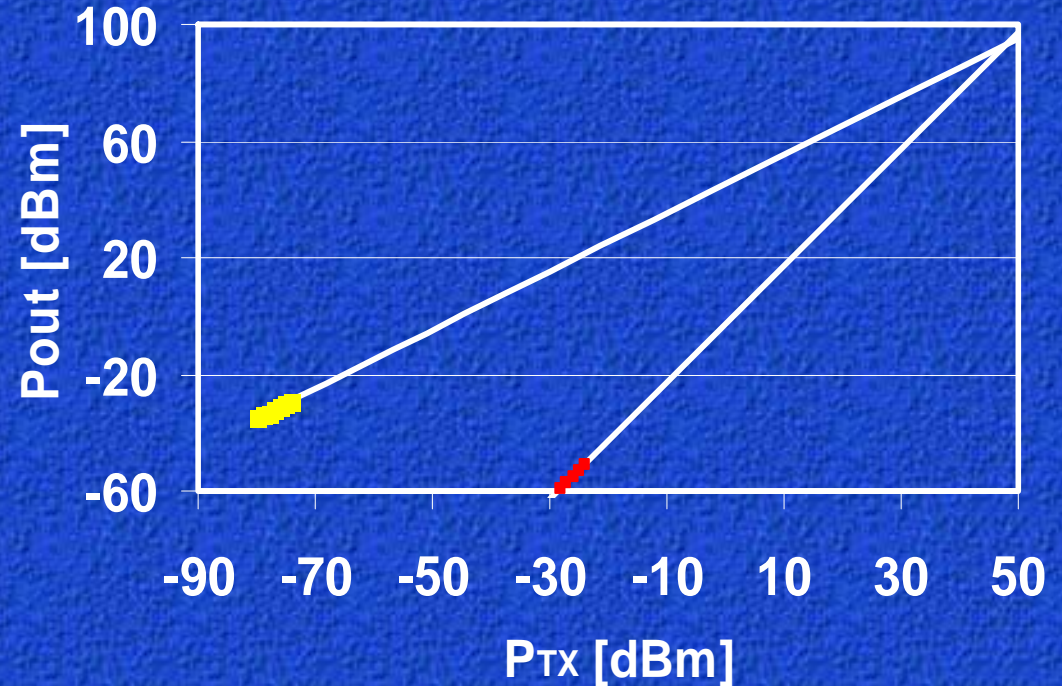
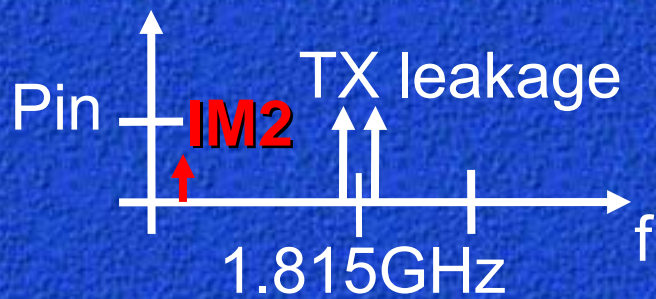
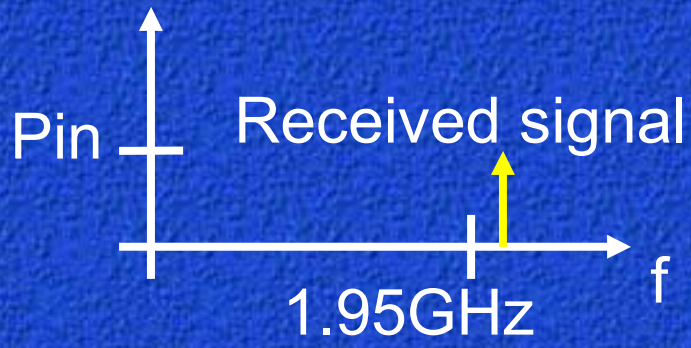


Nominal TX Power

$$PN_{135\text{MHz}} = \text{Noise} - P_{\text{TX}}$$

$$PN_{135\text{MHz}} = -155 \text{ dBc/Hz}$$

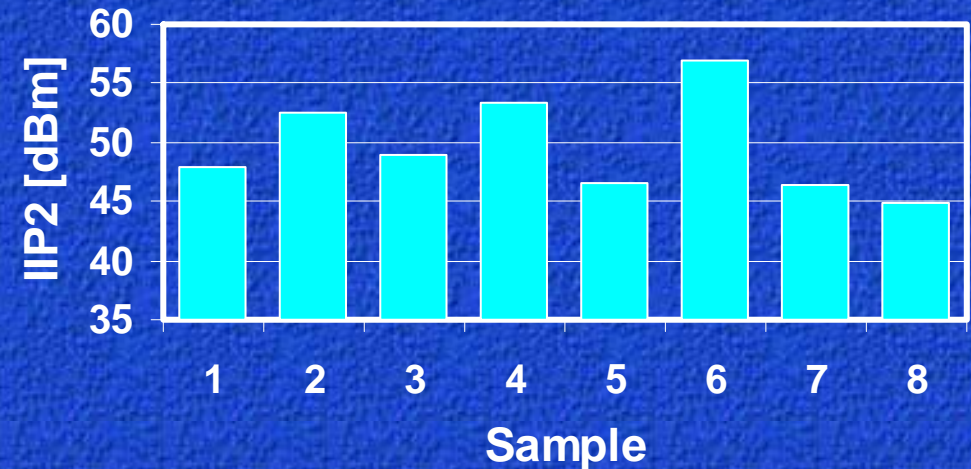
Out-of-band 2nd order intermodulation



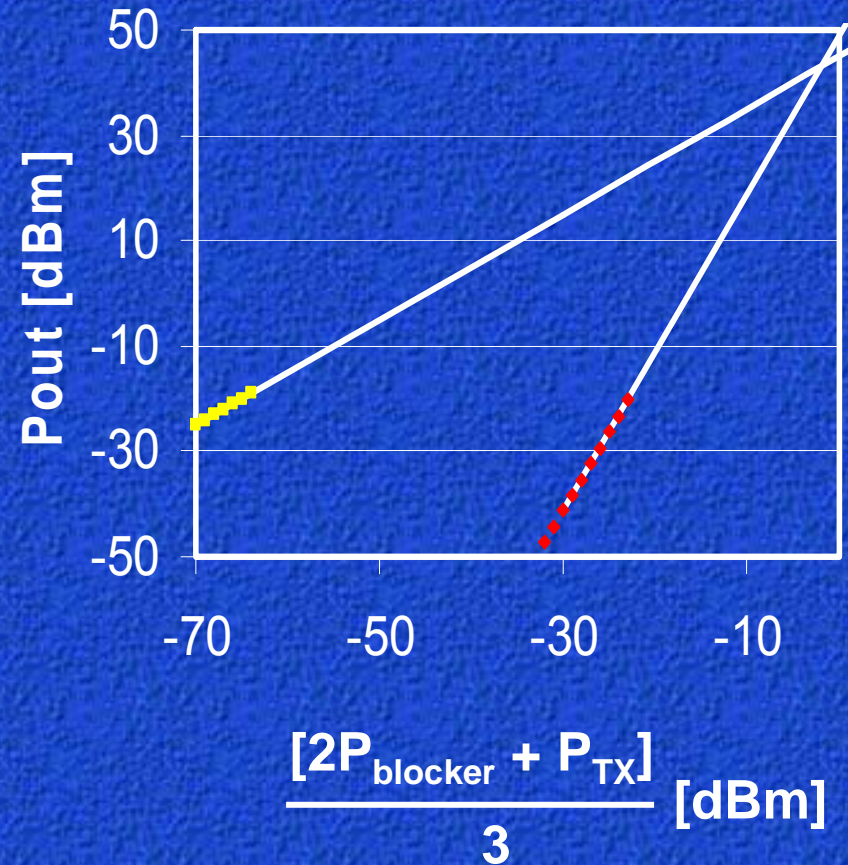
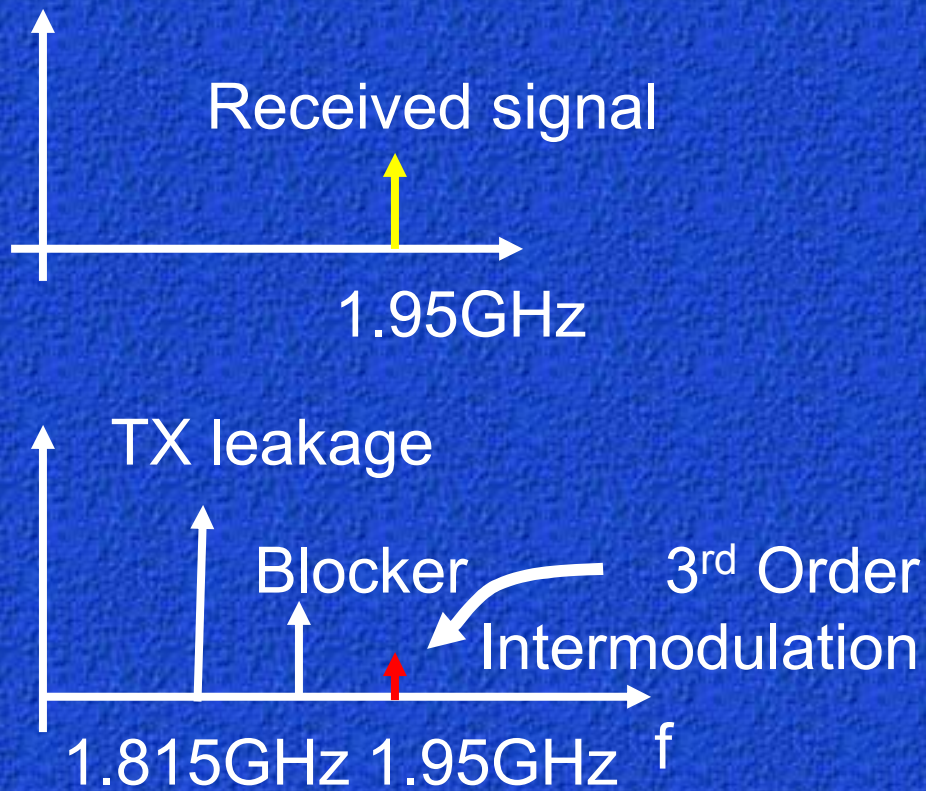
$$IM2 = 2P_{TX} - IIP2$$



$$IIP2 = 48dBm$$



Out-of-band 3rd order intermodulation

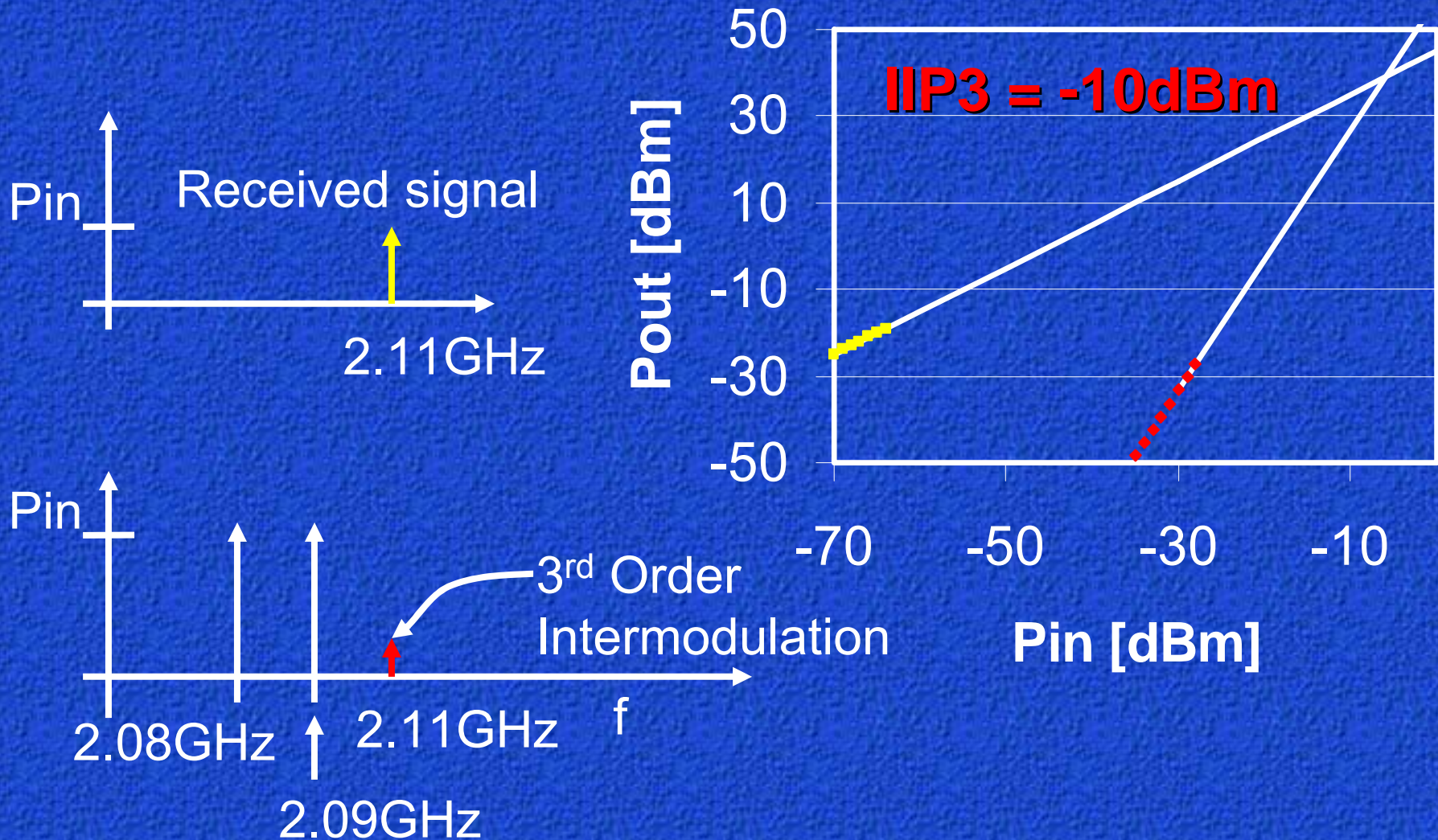


$$IM3 = 2P_{blocker} + P_{TX} - 2 IIP3$$



$$IIP3 = -2 \text{ dBm}$$

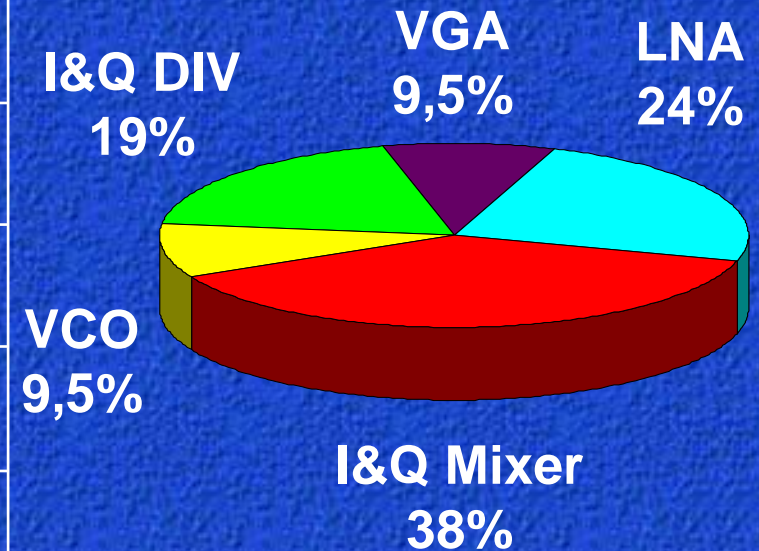
In-band 3rd order intermodulation



In-band IIP3 requirement = -18.8dBm

Performance Summary

NF	4.2dB * 5.6dB **
IIP3 out-of-band	-2dBm
Minimum IIP2	+44.8dBm
Gain	47dB
PN@135MHz	-155dBc/Hz
Power	38mW
Active Area	16mm ²
Technology	0.18μm 6M CMOS



Power consumption
breakdown

* Integrated between 200 kHz and 1.92 MHz

** Integrated between 10 kHz and 1.92 MHz

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Conclusion

- A 0.18 μm CMOS Receiver Front-End with on chip LO generation for UMTS has been demonstrated.
- Experimental measurements are 5.6dB NF, $\text{PN}_{135\text{MHz}} = -155\text{dBc/Hz}$, IIP3 = -2dBm, Minimum IIP2 = 44.8dBm, with 21mA Power Consumption.
- The Duplexer performance determines linearity and PN requirements

Acknowledgements

This work has been carried on by the following phd students : Francesco Gatta, Danilo Manstretta and Paolo Rossi.

I am indebted with them.