

University of Aberdeen



A Programmable Frequency Synthesiser

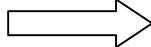

Roberta Cambio
r.cambio@eng.abdn.ac.uk



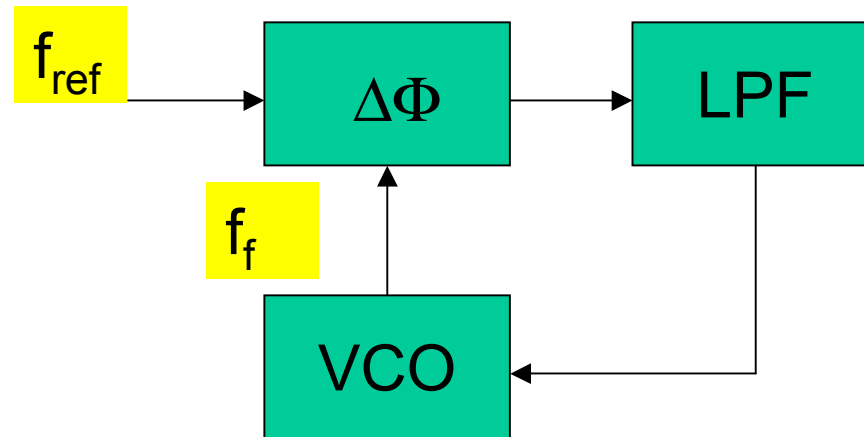
IST-2001-34561

24/09/2004

Introduction

- Conventional PLL  1975 Patent 
Hybrid Wide-band Re-configurable Synthesiser
- VHDL Simulation
- Mixed Signal Simulation (Verilog AMS)
- Hardware Tests
- Schematic of the RF board
- Comparison of an Integer-N PLL, a Fractional-N PLL and the Hybrid Synthesiser
- Insertion of a digital filter in the digital part of the synthesiser
- Channel hopping for UMTS
- Transfer function

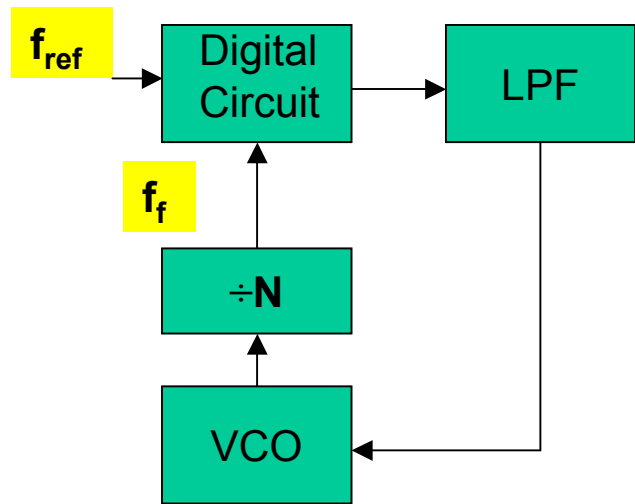
Conventional PLL



- At lock $f_f = f_{ref}$
- When f_{ref} changes to a new value, the PLL tracks f_{ref} adjusting the phase difference between f_{ref} and f_f
- The phase transfer function characterises the loop, with the VCO contributing a single pole to the transfer function

US Patent 3913028 (1975)

R.J. Bosselaers proposes a frequency synthesiser using both **digital** and **analogue** circuitry



$$\text{At lock } f_{\text{ref}} = \frac{N_2}{N_1} f_f$$

Features

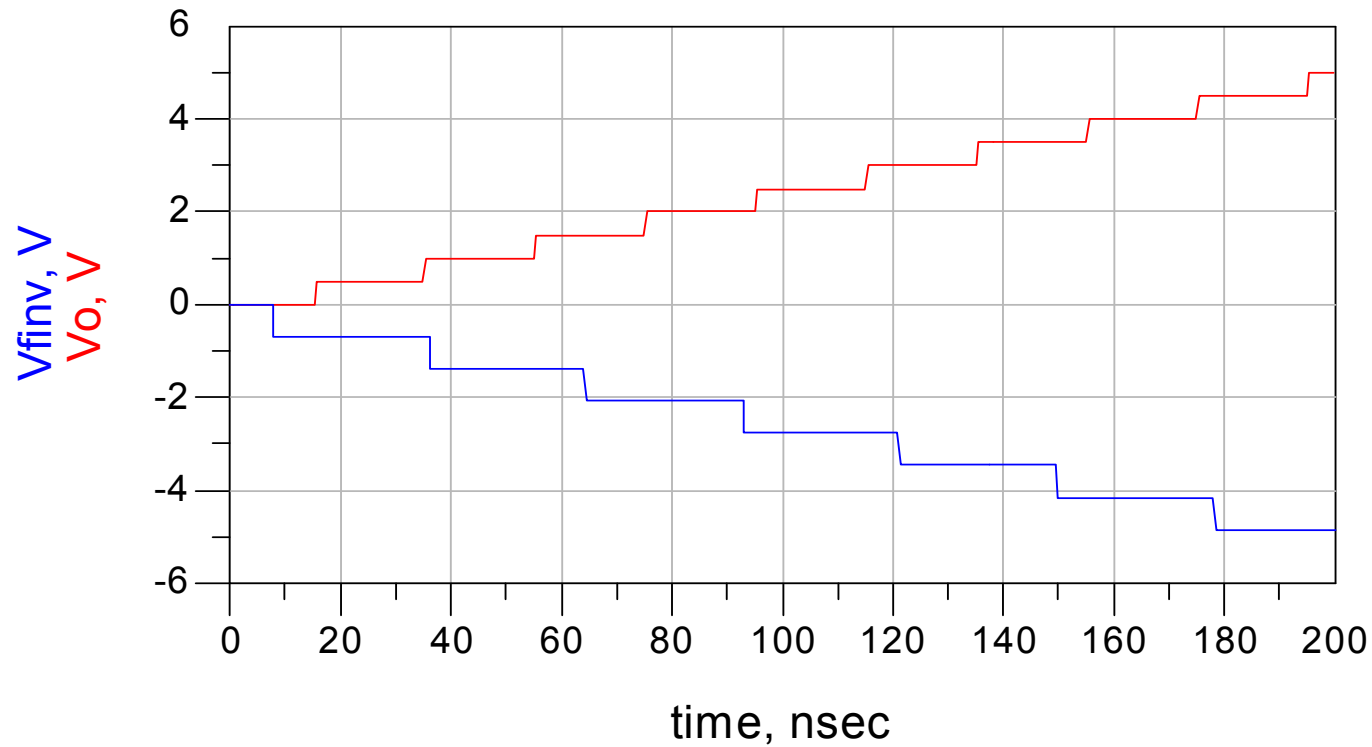
- Digital circuitry used 2 ALUs
- One ALU clocked by f_{ref}
- Other clocked by f_f
- Problem: 2 ALUs waste power
- Problem: Clock contention



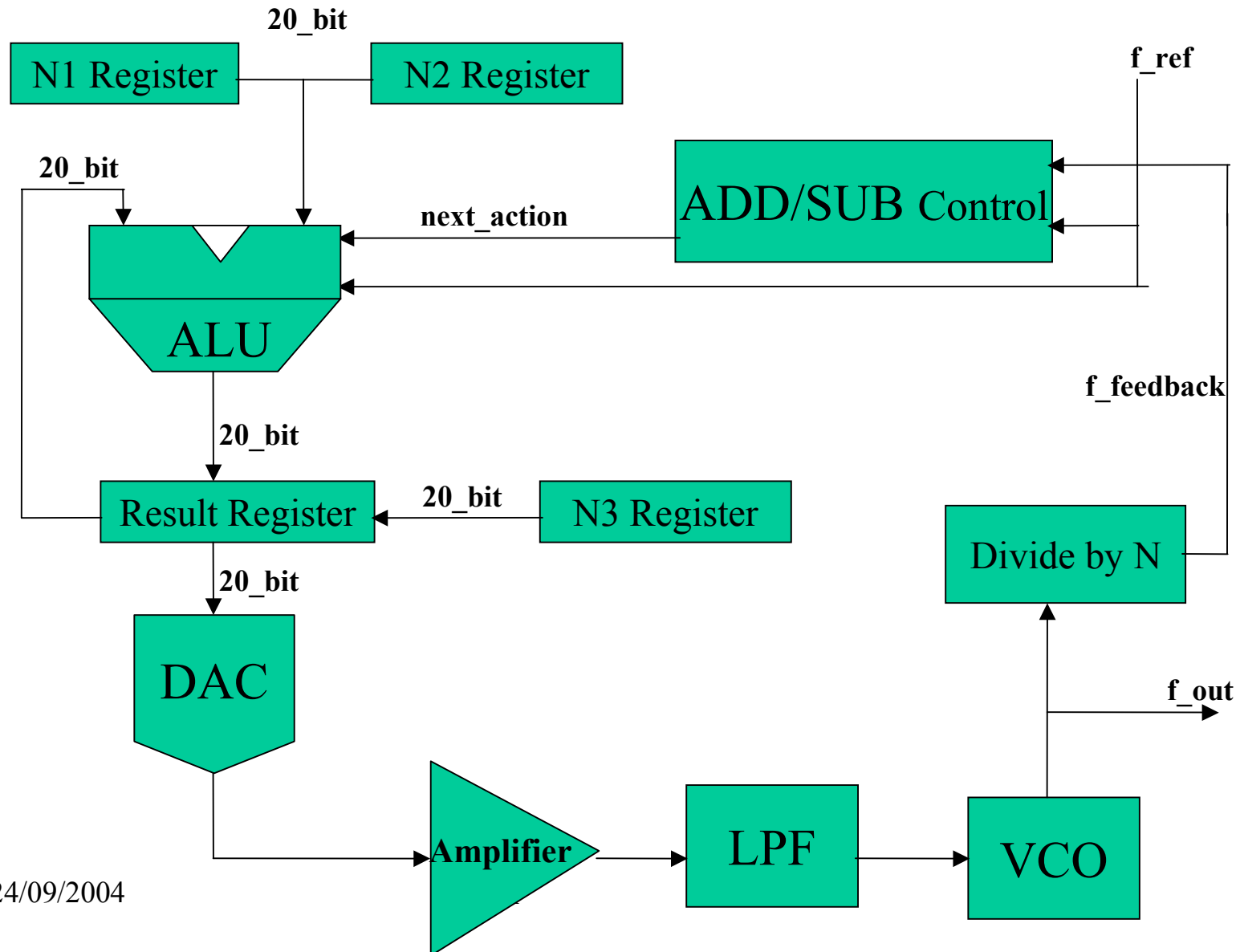
For the water level in the lake to remain constant the loss of water caused by evaporation must be compensated by the gain due to periods of rainfall.

Accumulation of Voltages Due to f_{ref} and f_f

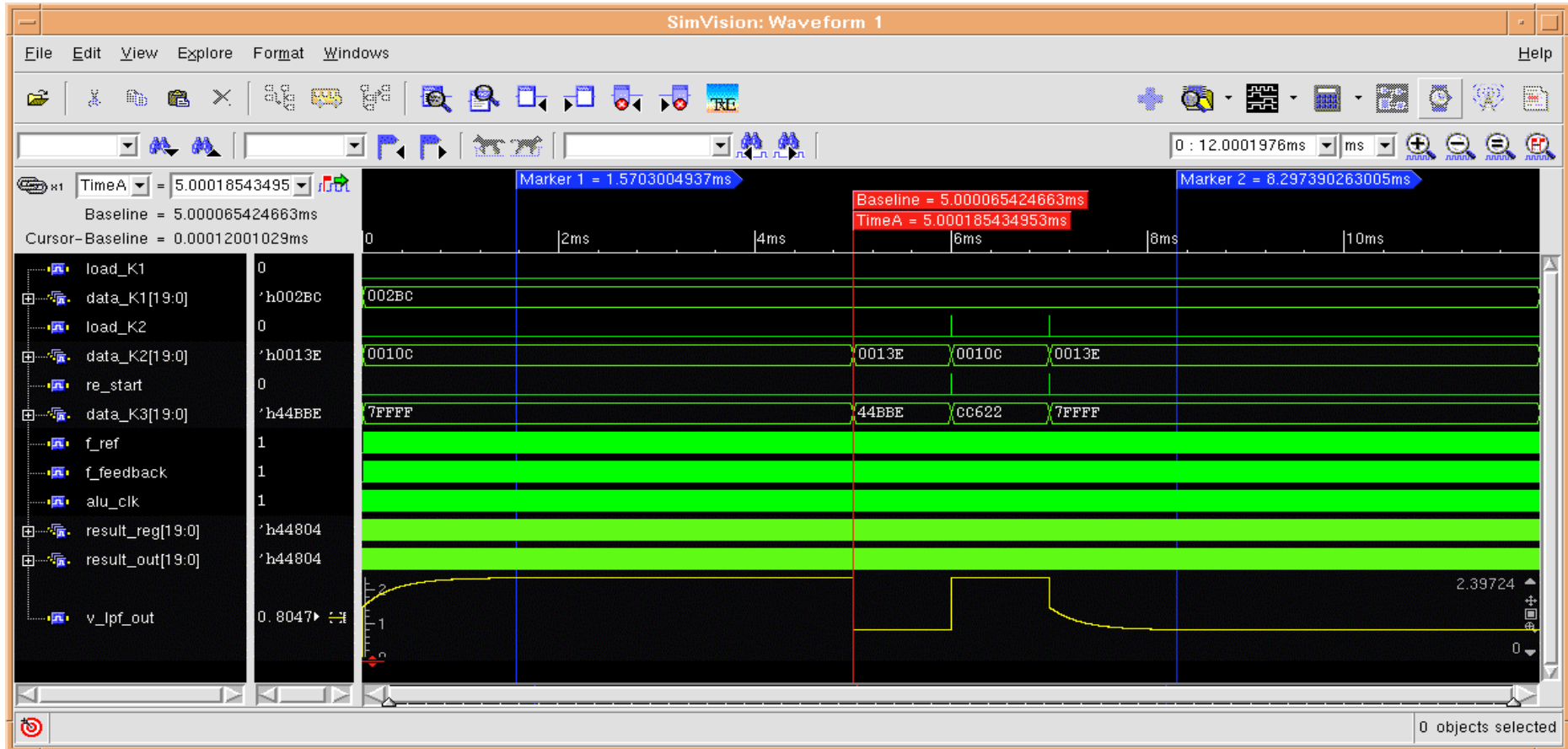
(ADS Behavioural Model)



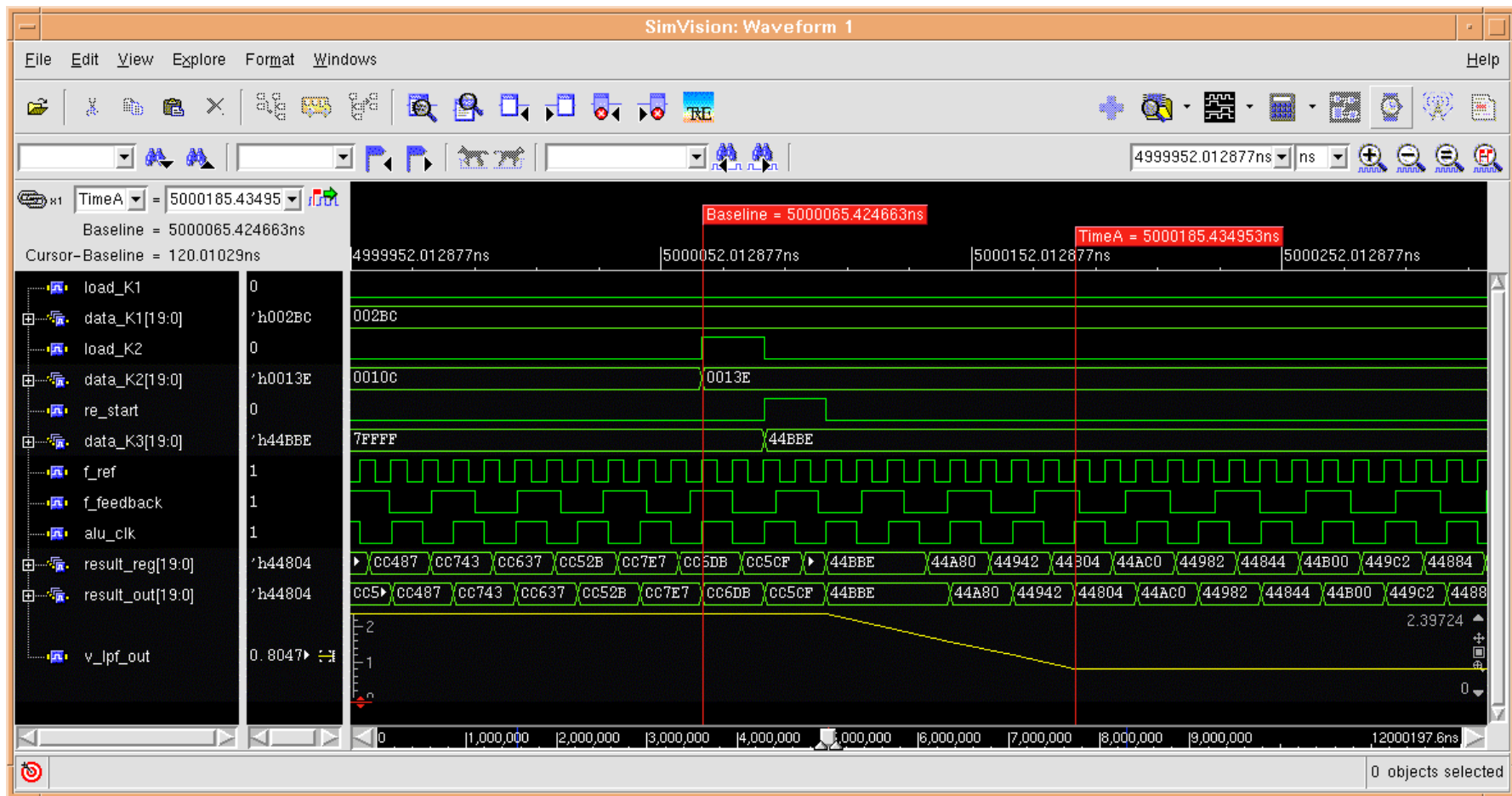
Block Diagram Of The VHDL Design Developed At Aberdeen



VHDL Simulation At 50 MHz Logic Clock



Expanded View Of The Falling Edge Of The LPF Output



Expanded View Of The Rising Edge Of The LPF Output

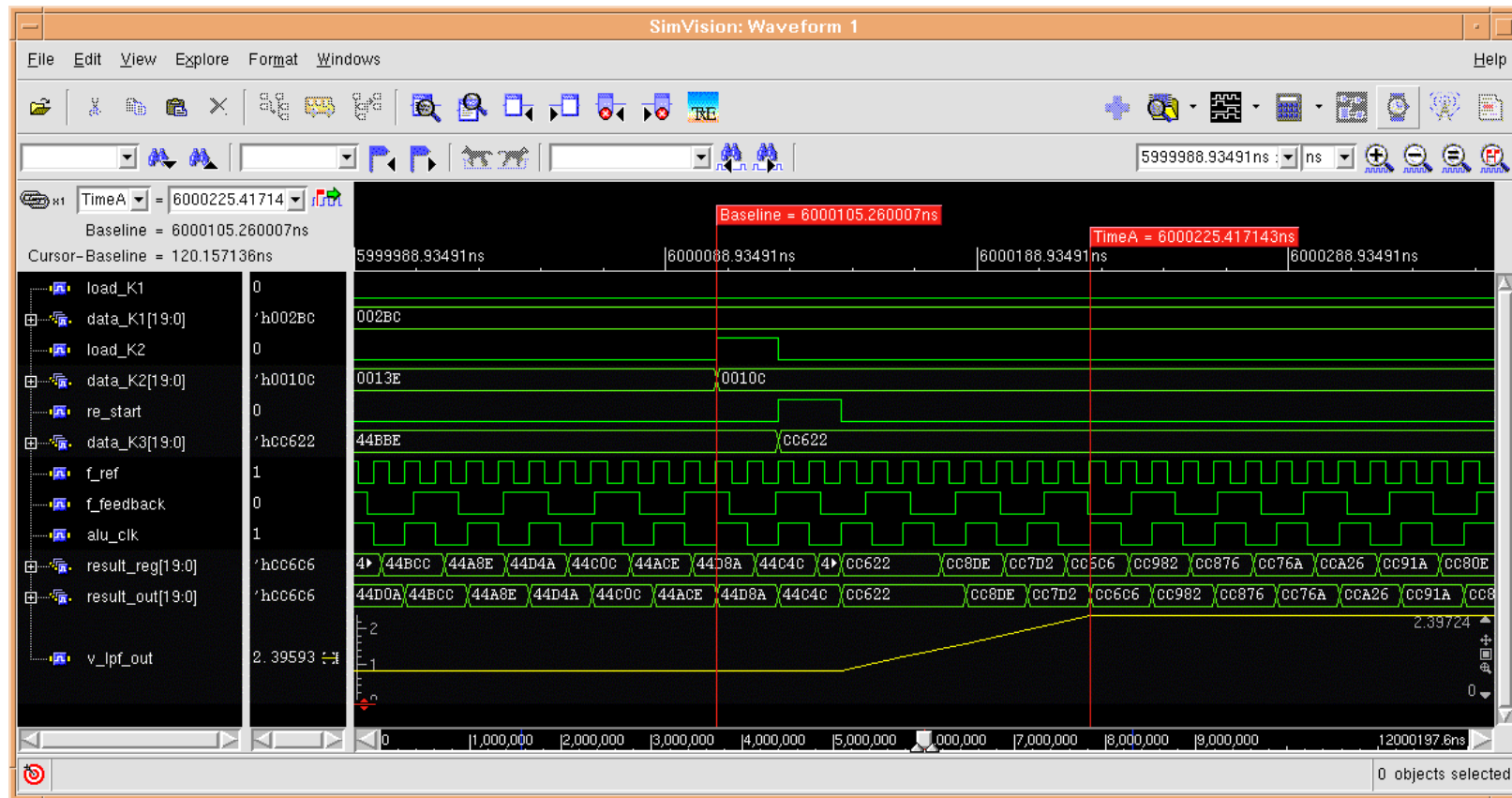


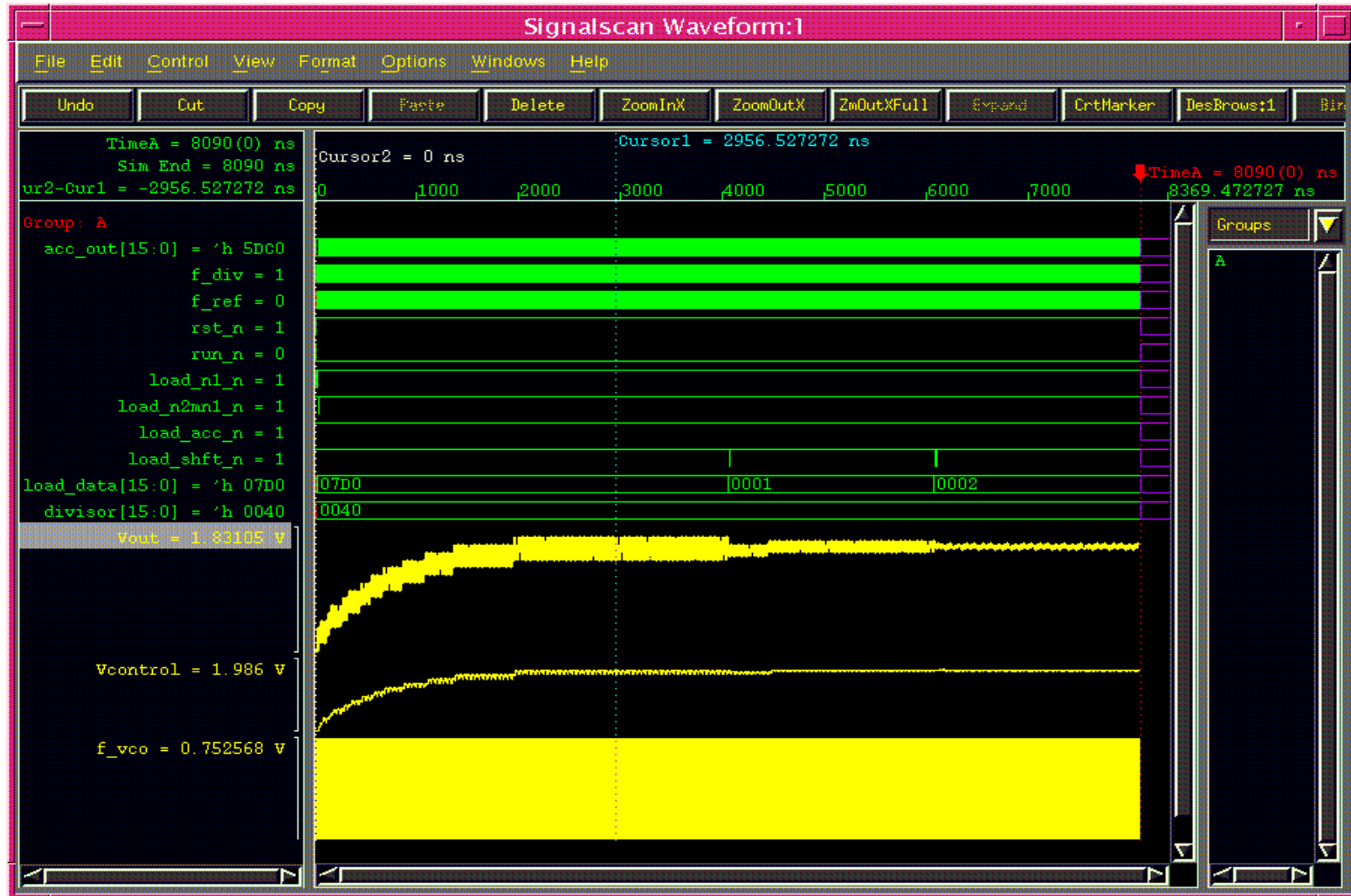
Table 1: Acquisition Time For The Frequency Ratio 7:5

N1	N2	N3	ACQUISITION TIME
50	70	MAX/2	> 10 mS
500	700	MAX/2	3.03 mS
5,000	7,000	MAX/2	202 uS
50,000	70,000	MAX/2	21 μS

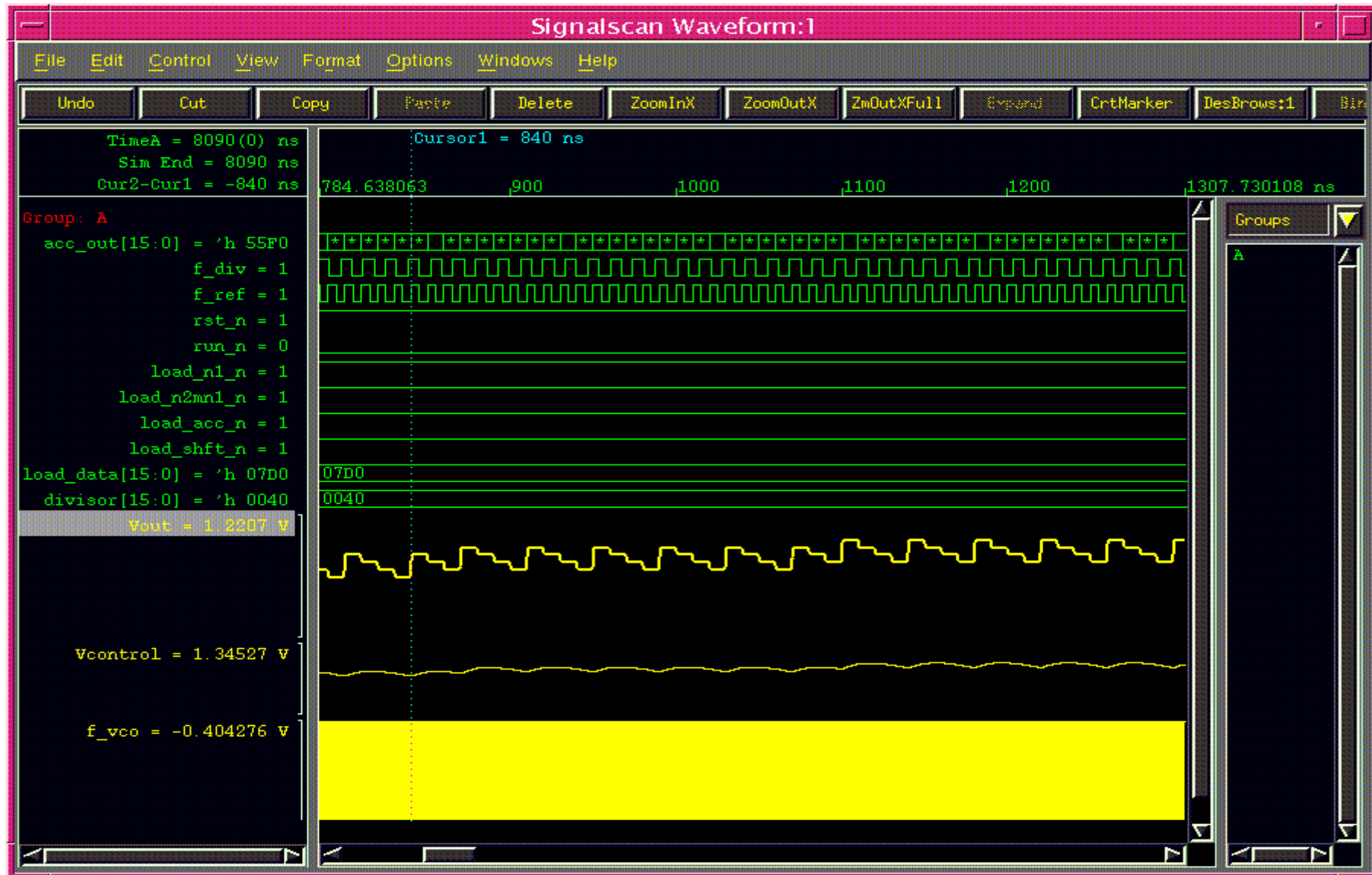
Table 2: Acquisition Time With The Predicted Value Of N3 At Switching

N1	N2	N3	ACQUISITION TIME
5	7	698638	120 nS
50	70	698638	120 nS
500	700	698638	120 nS

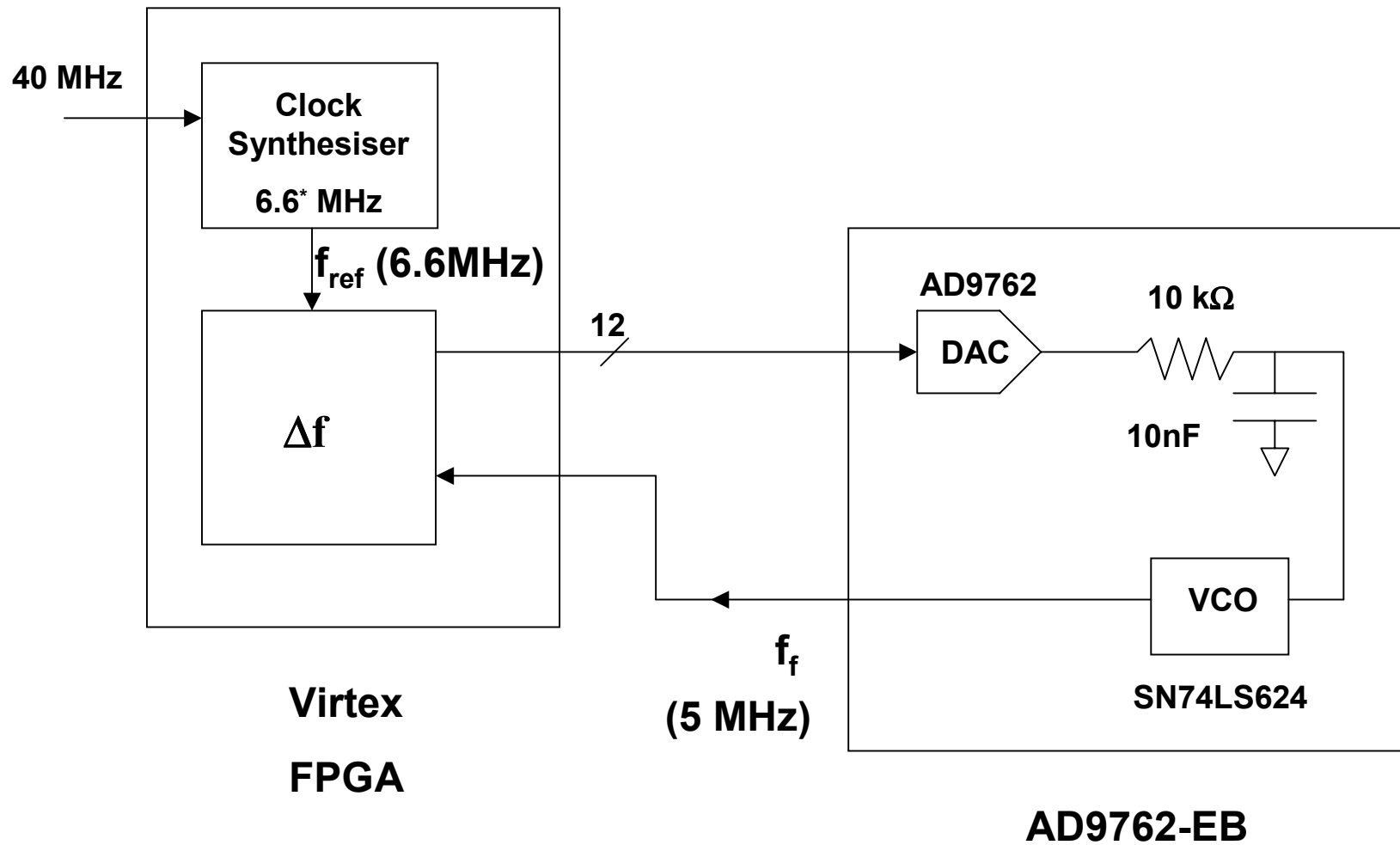
Verilog-AMS Simulation With Frequency Ratio 4:3 And $f_{VCO} = 4.8\text{GHz}$



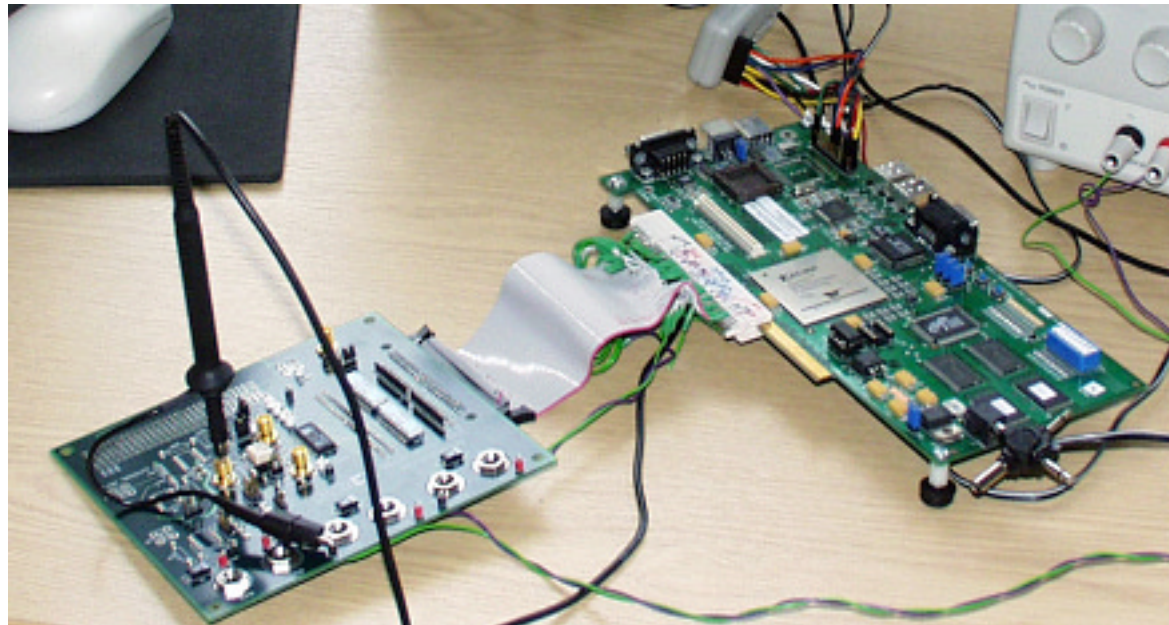
Expanded View



Hardware: Closed Loop Test Set-up



Interim Hardware Set-Up

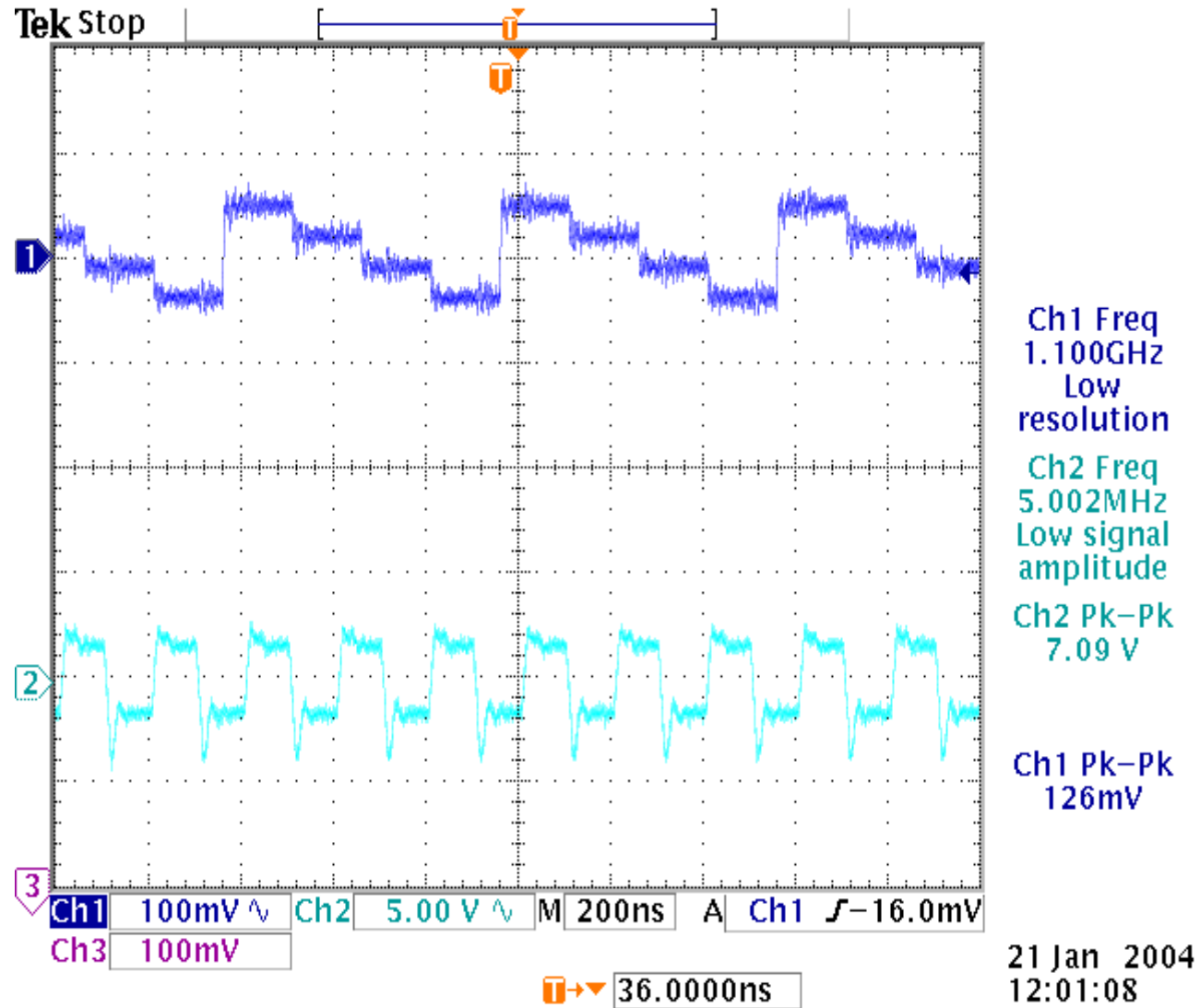


12-bit DAC development board donated by Analog Devices

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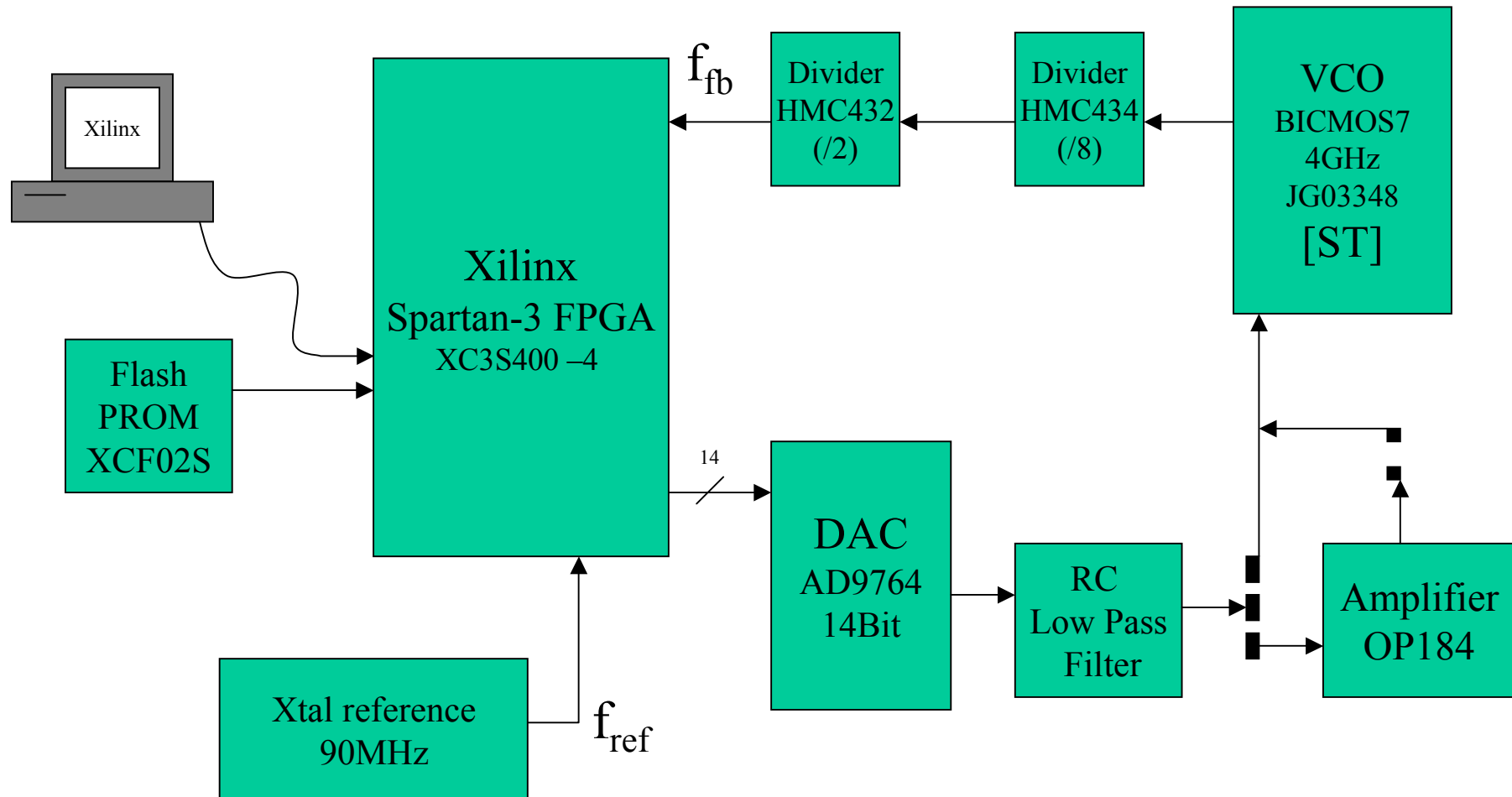
DAC Output For 4:3 Ratio



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Schematic Diagram Of The RF Board



Components Included In The RF Board

Digital Circuitry	Xilinx Spartan 3 XC3S400-4 maximum system clock rate: 326MHz
DAC	AD9764, 14 bit, 125MSPS No strict dynamic requirements
Analogue Filter	1 pole RC filter
VCO	BiCMOS7 4GHz VCO (ST Microelectronics) frequency range: 3.74-4.28GHz
Frequency Divider (÷64)	High Freq.: divide by 8 (HMC434) divide by 2 (HMC432) Low Freq.: divide by 4 (asynchronous in Spartan 3)
Loop Amplifier	OP184, gain=2

Comparison Of An Integer-N PLL, A Fractional-N PLL & The Hybrid Synthesiser

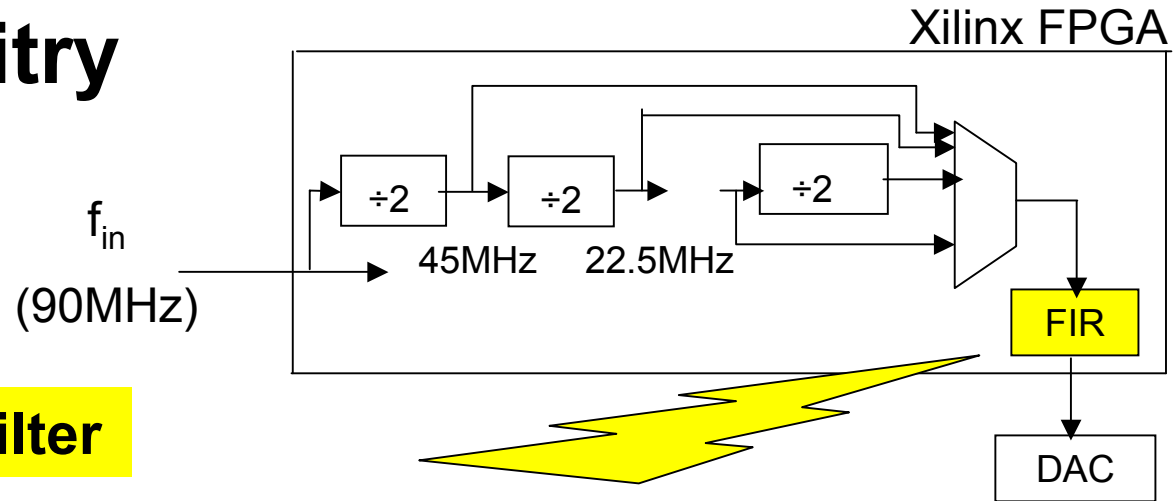
	INTEGER-N PLL	FRACTIONAL-N PLL	HYBRID SYNTHESISER
INPUT FREQUENCY	200kHz (UMTS)	20MHz (UMTS)	90MHz
BANDWIDTH	$f_{ref}/10=20\text{kHz}$	$f_{ref}/100=200\text{kHz}$	80MHz
ACQUISITION TIME	~0.1ms (depending on the implementation)	~0.1ms (depending on the implementation)	10 μs (Verilog-AMS simulation) 800 μs (measured in lab for 6.6MHz)

Comparison With TI TRF3750 & Philips SA8028

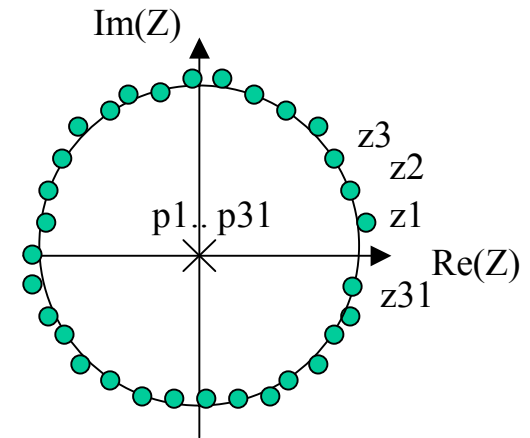
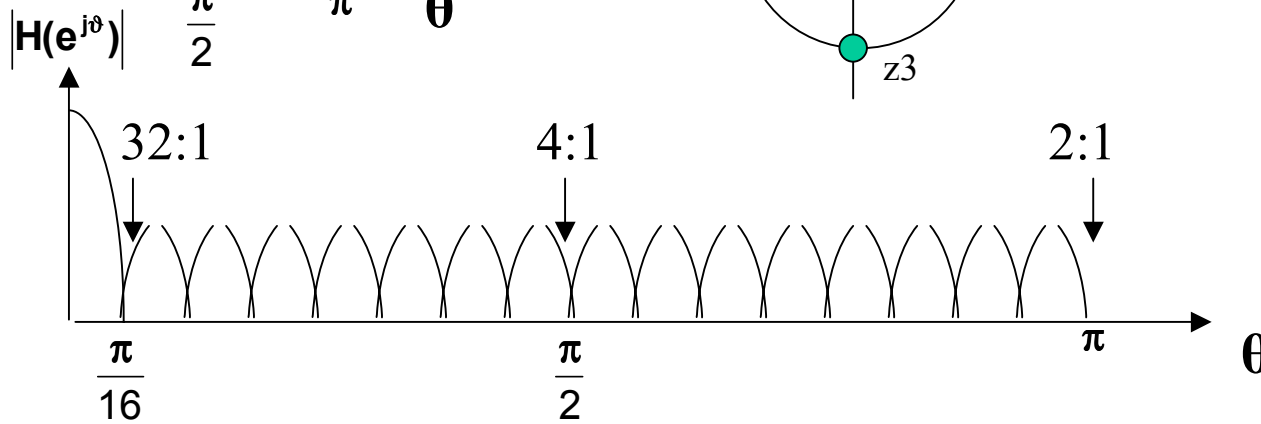
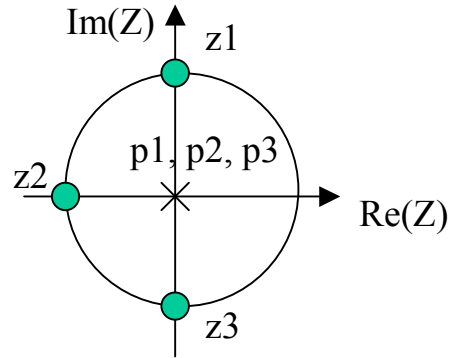
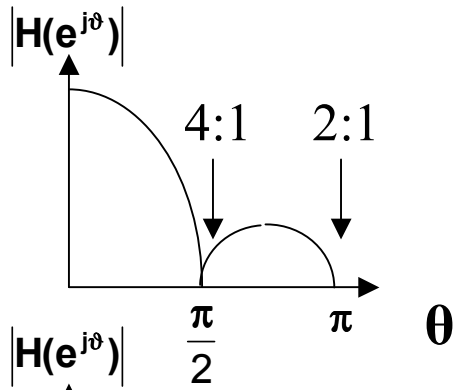
	TI TRF3750 [Integer-N]	Philips SA8028 [Fractional-N]	Hybrid Synthesiser
Frequency Discriminator			4mW @ 2.5V
DAC			190mW @ 100MHz
Frequency Divider			104mA*3V =312mW
Total Power (*)	13mA*3.3V =43mW	7.6mA*3V =22.8mW	506mW

(*) = filter and VCO excluded

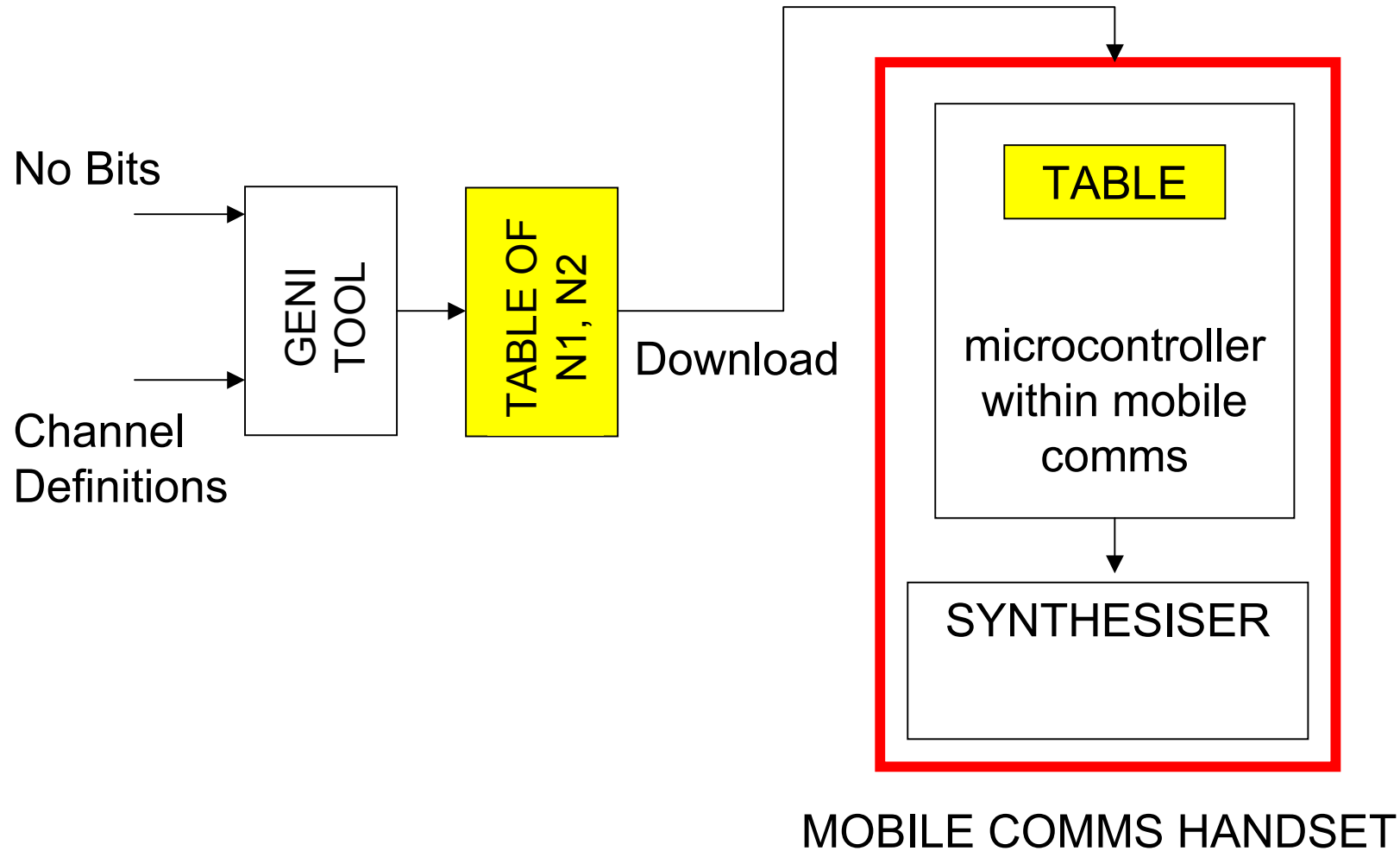
Digital Circuitry



Moving Average Filter



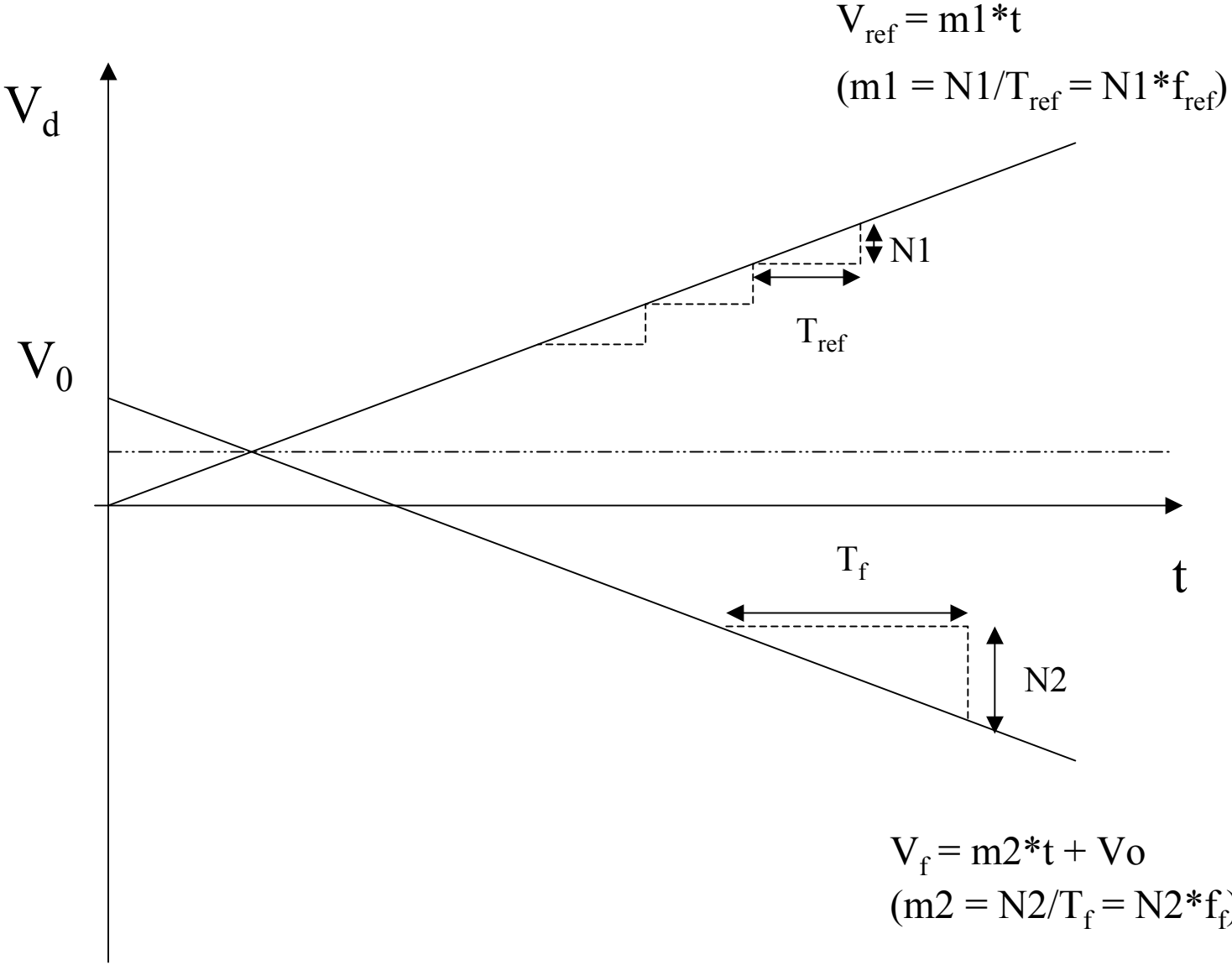
Practical Application Of The Synthesiser



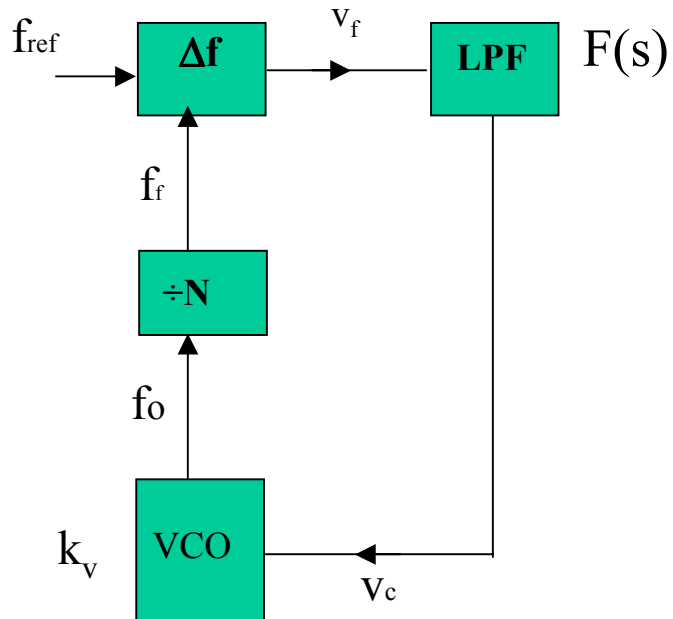
Parameters For The Digital Block

CARRIER FREQ. [MHz]	INPUT FREQ. [MHz]	FEEDBACK FREQ. [MHz]	N1	N2	NOTCH DIGITAL FILTER [MHz] (repetition freq.)	SAMPLING FREQ. [MHz]
1900.000	90.000	59.375	95	144	0.625	2.500
1900.200	90.000	59.381	3167	4800	0.019	0.075
1900.400	90.000	59.388	4751	7200	0.013	0.050
1900.600	90.000	59.394	2090	3167	0.028	0.114
1900.800	90.000	59.400	33	50	1.800	7.200
1901.000	90.000	59.406	1901	2880	0.031	0.125
1901.200	90.000	59.413	3708	5617	0.016	0.064
1901.400	90.000	59.419	3169	4800	0.019	0.075
1901.600	90.000	59.425	2377	3600	0.025	0.100

Output Of The Digital Circuit



Loop Transfer Function



$$\begin{cases} \mathbf{v}_1(\mathbf{t}) = \int \frac{\mathbf{N}_1}{\mathbf{T}_{\text{ref}}} \mathbf{d}\mathbf{t} + \mathbf{c}_1 = \int \mathbf{N}_1 \mathbf{f}_1 \mathbf{d}\mathbf{t} + \mathbf{c}_1 \\ \mathbf{v}_2(\mathbf{t}) = \int \frac{\mathbf{N}_2}{\mathbf{T}_f} \mathbf{d}\mathbf{t} + \mathbf{c}_2 = \int \mathbf{N}_2 \mathbf{f}_2 \mathbf{d}\mathbf{t} + \mathbf{c}_2 \end{cases}$$

$$\mathbf{v}_f(\mathbf{t}) = \mathbf{v}_1(\mathbf{t}) - \mathbf{v}_2(\mathbf{t}) = \mathbf{N}_1 \int \mathbf{f}_1 \mathbf{d}\mathbf{t} - \mathbf{N}_2 \int \mathbf{f}_2 \mathbf{d}\mathbf{t}$$

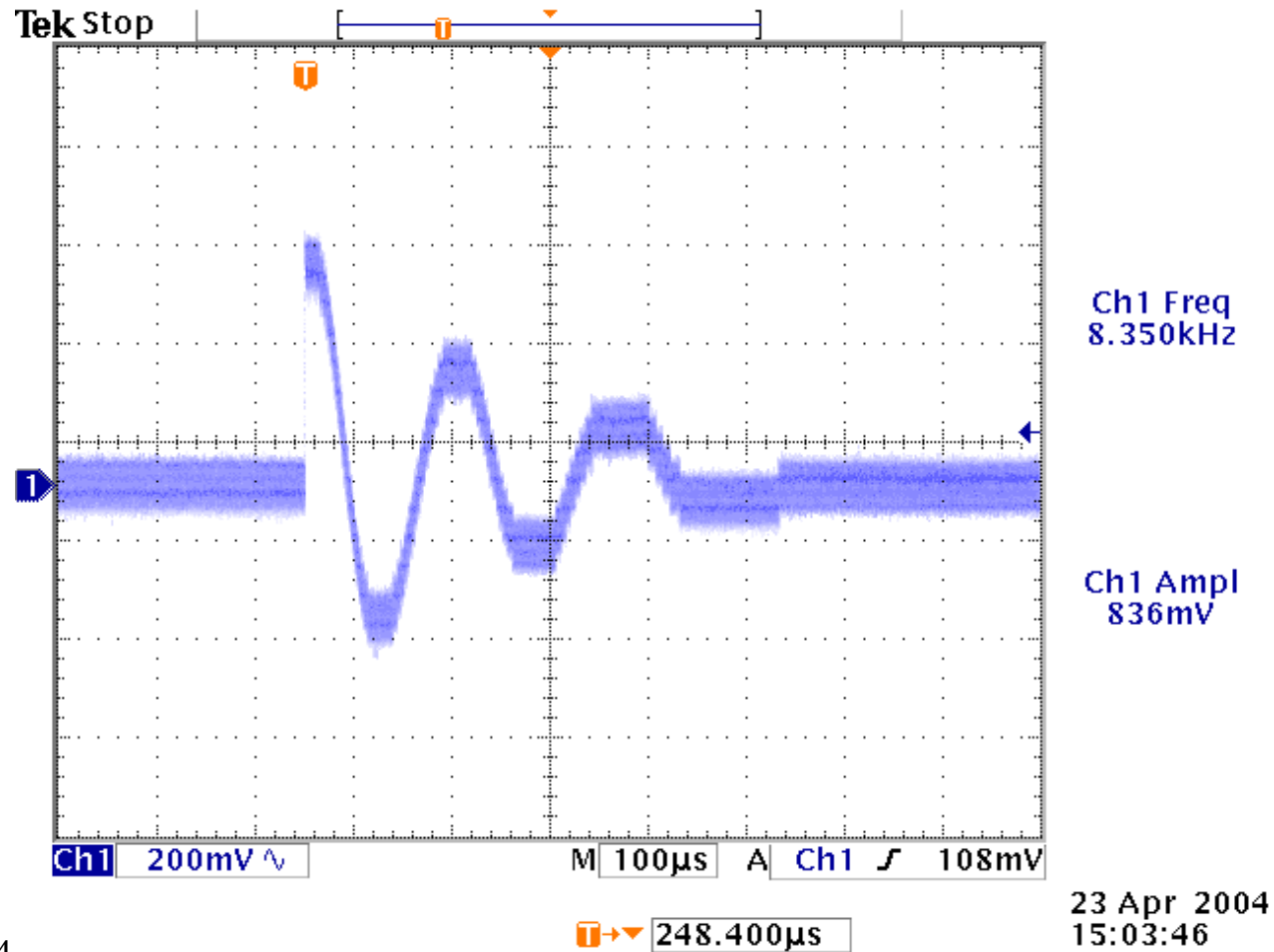
$$\mathbf{H}(\mathbf{s}) = \frac{\mathbf{c} \omega_n^2}{\mathbf{s}^2 + 2\zeta \omega_n \mathbf{s} + \omega_n^2}$$

$$\mathbf{c} = \frac{\mathbf{k}_v \mathbf{N}_1}{\mathbf{T} \omega_n^2}$$

$$\zeta = \frac{1}{2\mathbf{T} \omega_n}$$

$$\omega_n = \sqrt{\frac{\mathbf{k}_v \mathbf{N}_2}{\mathbf{T}}}$$

Damped Oscillations For A Start-up Transient (HW Implementation)

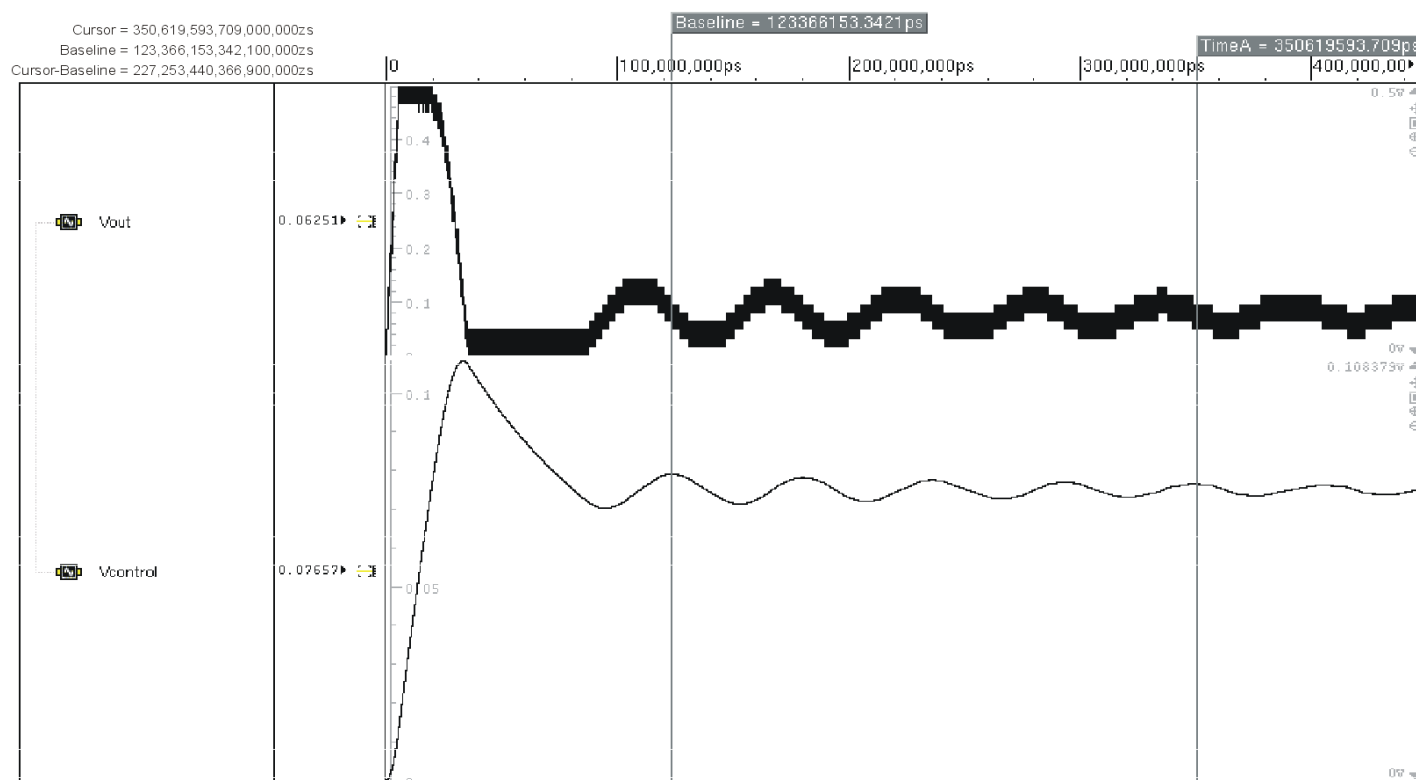


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Start-up Transient Of The Synthesiser In The Verilog-AMS Model

SimVision: Waveform 1

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Summary

- Hybrid Synthesiser guarantees $f_{\text{ref}} = \frac{N_2}{N_1} f_f$ at lock.
- Acquisition of the desired output frequency can be speeded up with application of the correct initial conditions.
- The low frequency waveform, predicted by theory, output by the DAC has been confirmed by observations via the interim HW setup.
- Higher input frequency implies better frequency divider phase noise for the RF board.
- Accurate definition of UMTS channels is possible.
- The Laplace-transform analysis has identified a second order system.