

New approach for frequency synthesizers in multi-mode radio applications

Stephan Böcker, Markus Müller, Ralf Kakerow

Nokia Research Center
Bochum, Germany



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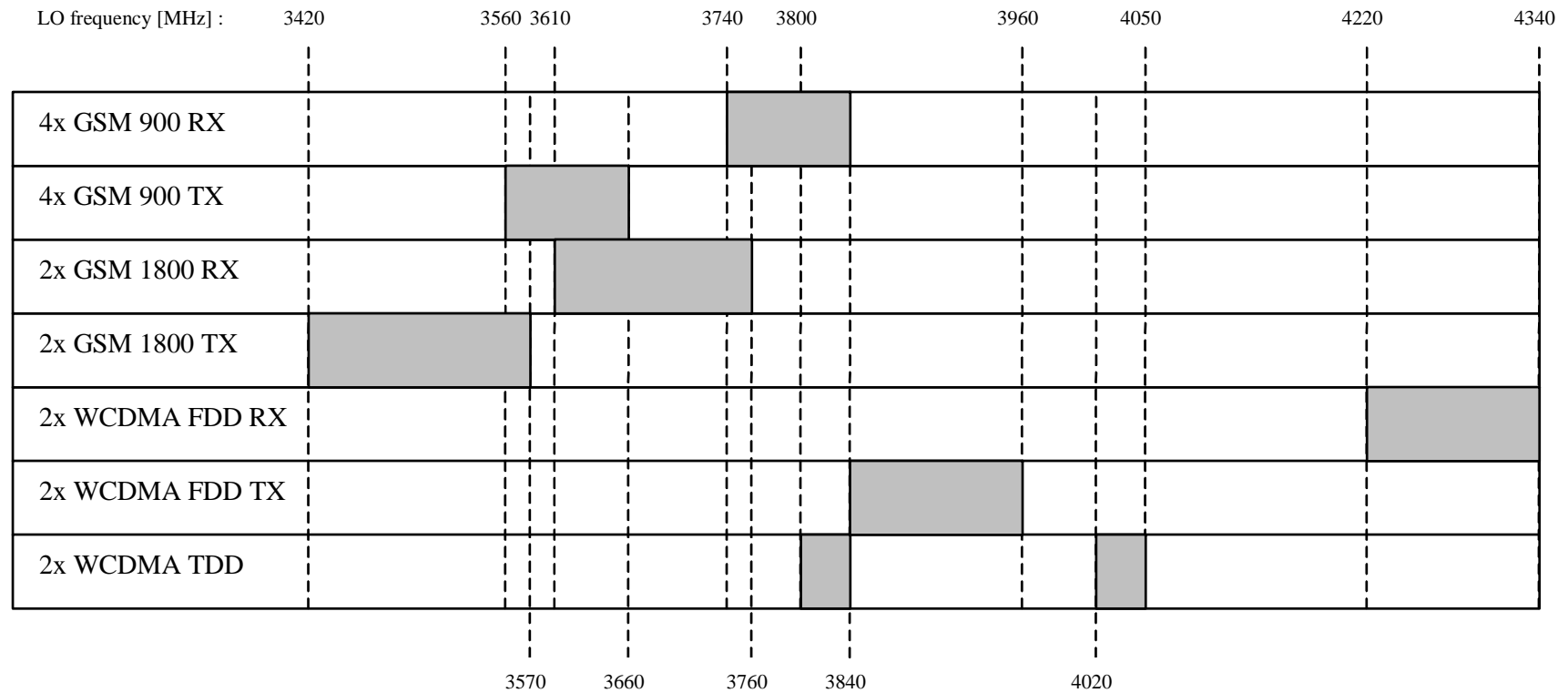
Outline

- Frequency synthesizers for multi-mode transceivers
- Description of the target application
- Comparison of synthesizer architectures
- Description of the demonstrator design
- Conclusion

Requirements to multi-mode frequency synthesizers

- In transceiver frontends, multi-mode operation concerns the frequency synthesizer mainly in terms of...
 - frequency bands
 - phase noise / spurious performance
 - settling times
- Combining hardest spec from each mode into a single "all-purpose synthesizer" often results in an over-designed system
=> cost, power
- Building separate synthesizers for each mode is straightforward, but needs additional silicon area and board space
=> cost
- A multi-mode synthesizer combines low area and low power by sharing reconfigurable components for multiple modes

Frequency plan



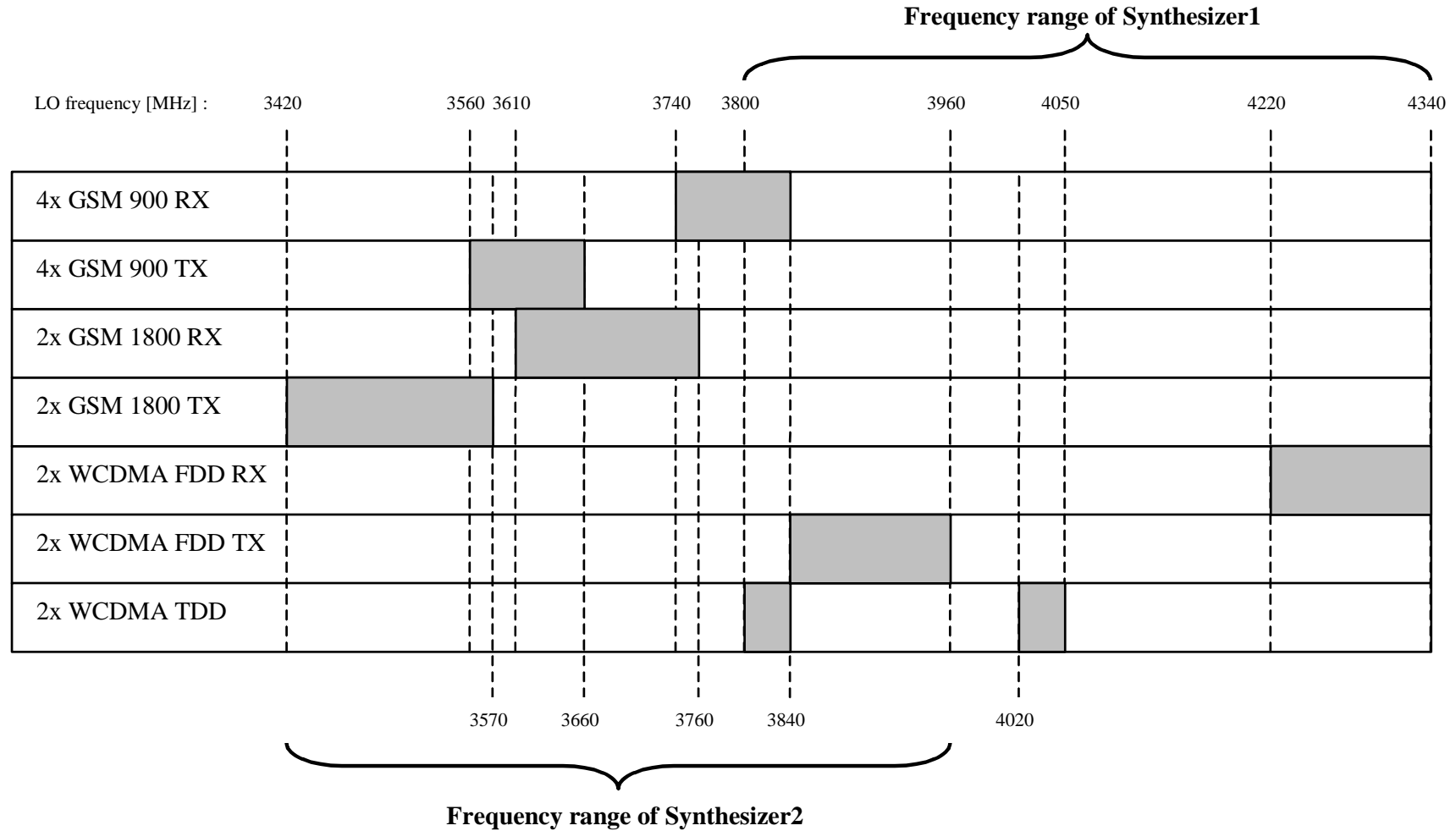
Target application

- Direct conversion frontend supporting WCDMA / HSDPA and GSM 900 / 1800 modes

	WCDMA-FDD	
	WCDMA Mode	GSM Mode
Synthesizer1:	WCDMA RX	monitoring WCDMA
Synthesizer2:	WCDMA TX, monitoring GSM	GSM RX & TX
	WCDMA-TDD	
	WCDMA Mode	GSM Mode
Synthesizer1:	WCDMA RX & TX	monitoring WCDMA
Synthesizer2:	monitoring GSM	GSM RX & TX

Proposed two-synthesizer architecture

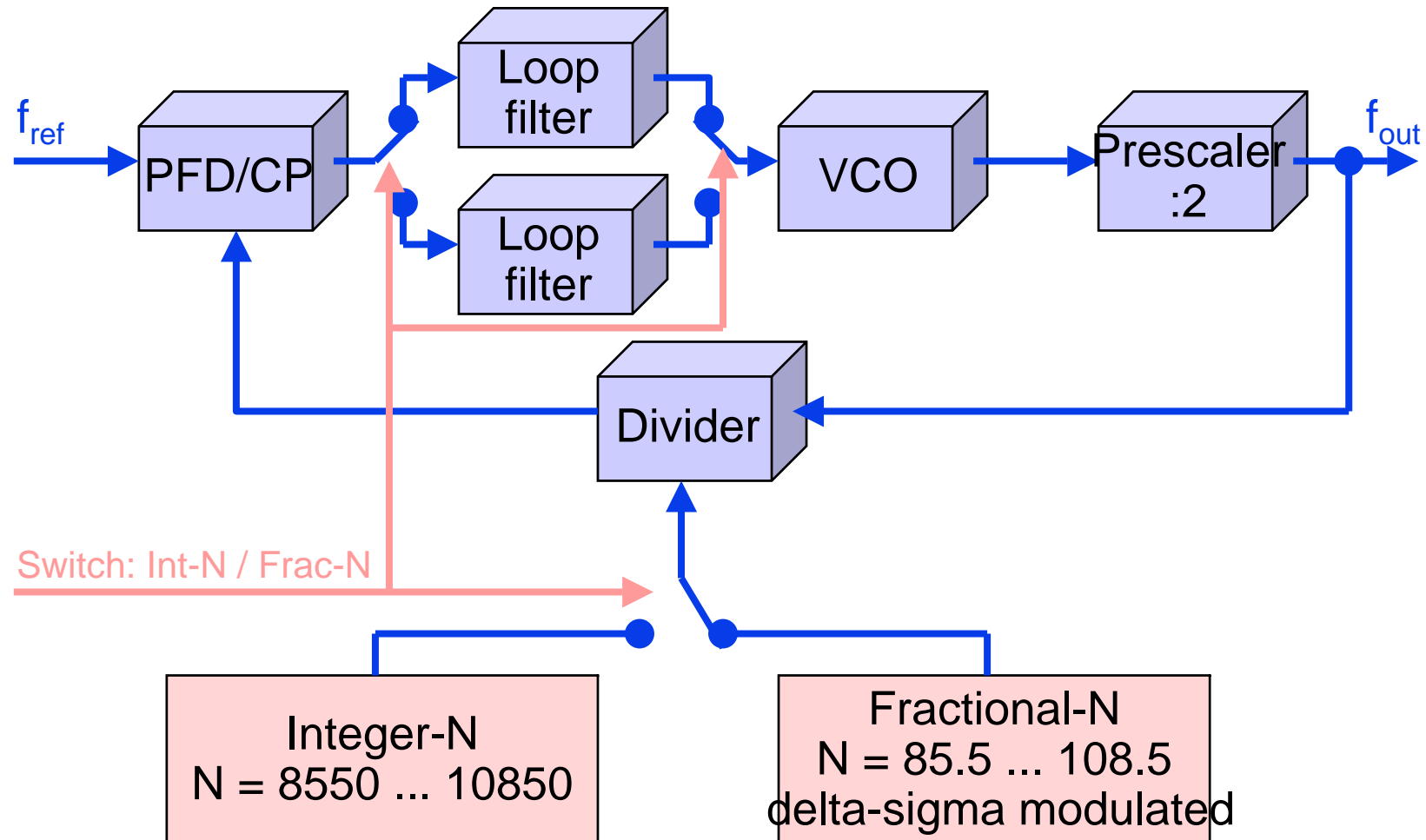
Frequency plan



Comparison of PLL architectures

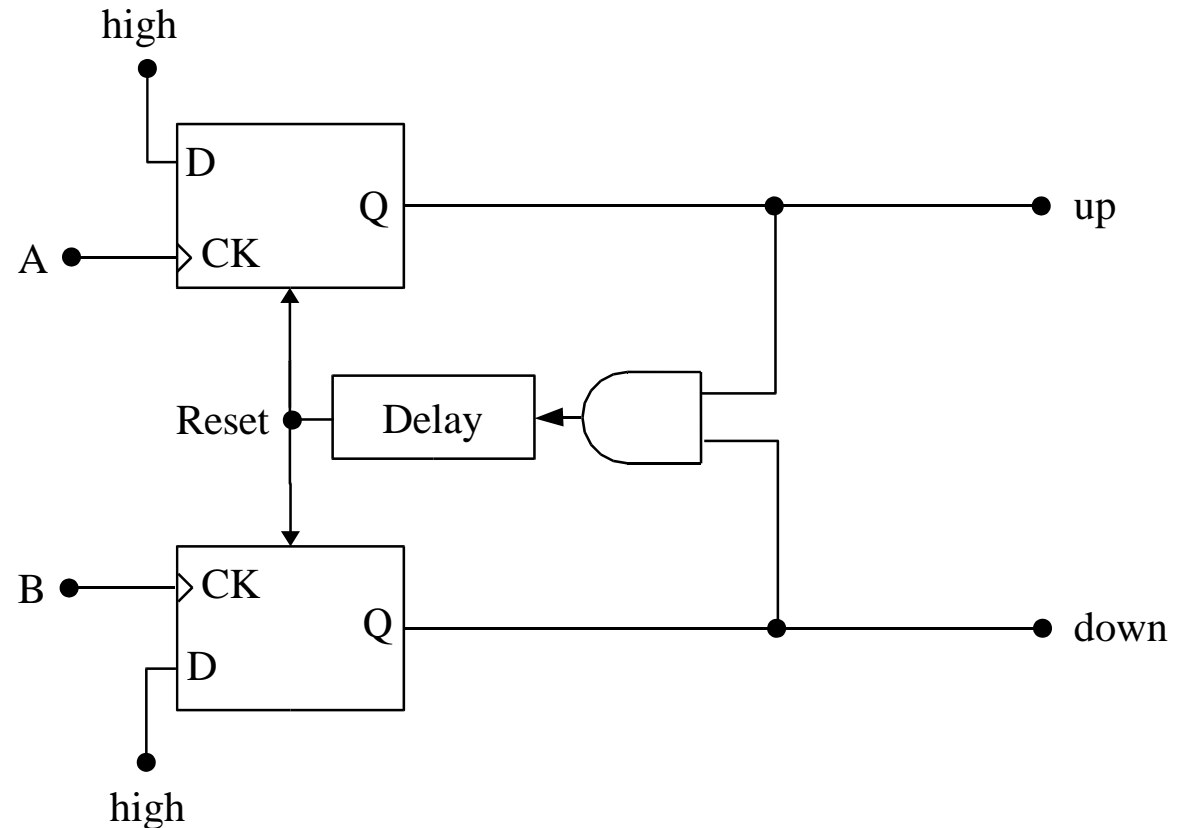
	Integer-N PLL	$\Delta\Sigma$ Frac. N PLL	Dual Loop PLL	SO + Frac-N PLL	DDS & Int-N PLL
Loop bandwidth	↓	→	↑ / ↓	→	→
Settling time	↑	↓	↑	↓	↓
Required VCO phase noise performance	↑	→	→ / →	→ / ↓	→
Created noise level	→	↑	↑	↑	↑
Design complexity	→	↑	↑	↑	↑
Area consumption	↓	→	↑	→	↑
Power consumption	↓	→	↑	→	↑

Synthesizer block diagram



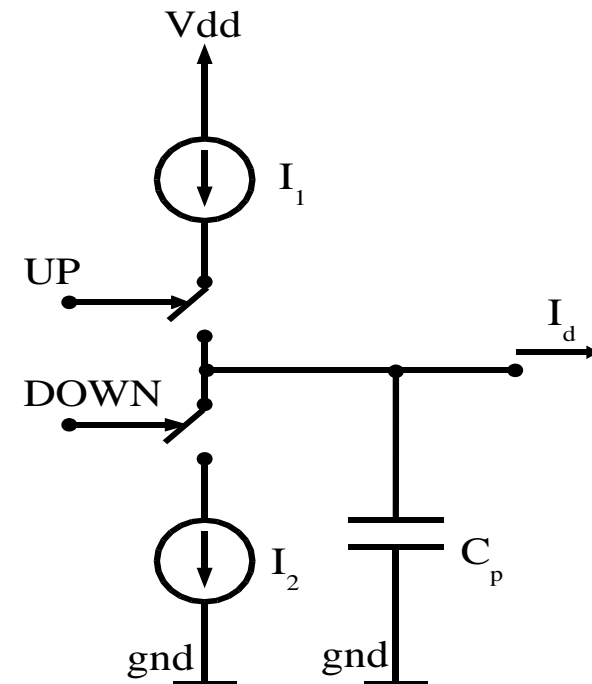
Phase and frequency detector

- Implemented with CMOS standard cells
- No dead-zone
- Minimum CP pulse width programmable via delay cell in reset path



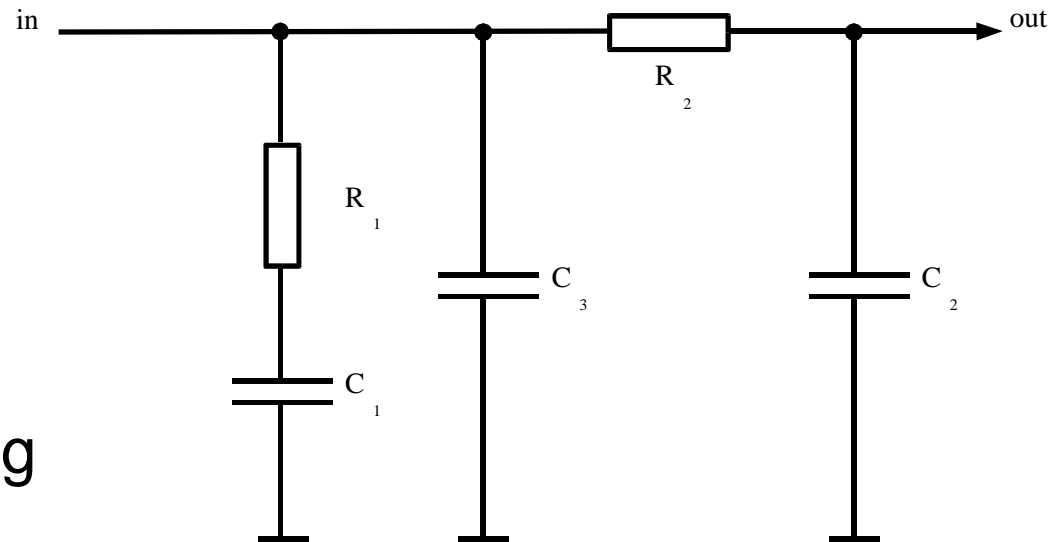
Charge pump

- Standard CMOS implementation
- UP / DOWN current mismatch is critical for spurious performance => especially in Fractional-N mode
- UP / DOWN currents can be adjusted independently
- Same charge pump current used for Integer-N and Fractional-N modes



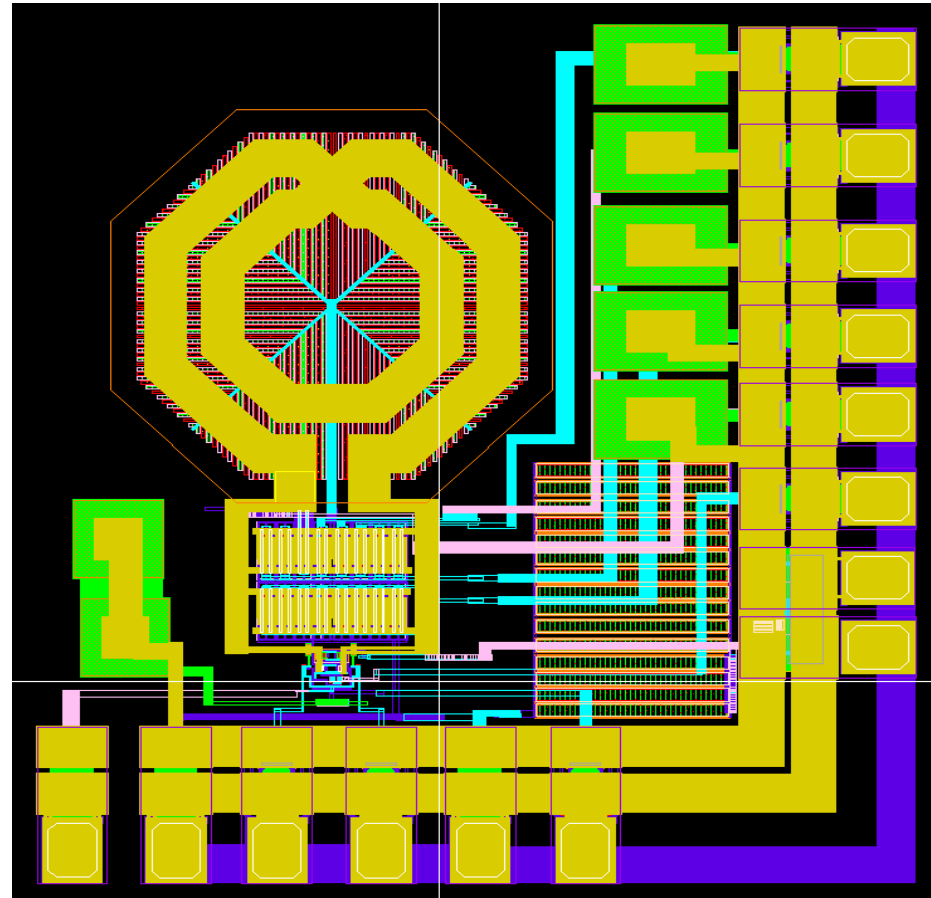
Loop filter

- 3rd order passive RC loop filter
- Current-to-voltage conversion
- Support of different PLL architectures by switching single components or whole filter
- Left off-(test)chip for extended flexibility



Voltage controlled oscillator

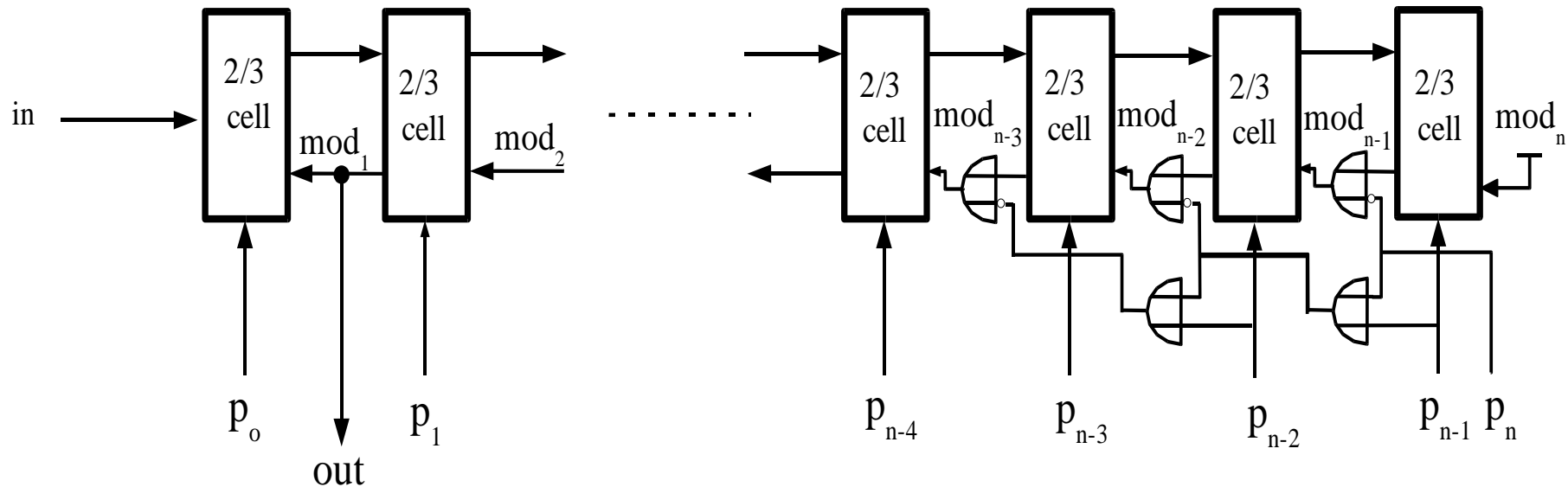
- Multi band VCO with switched capacitor network
- Phase noise optimized design
- Low power consumption
- Developed by EPFL



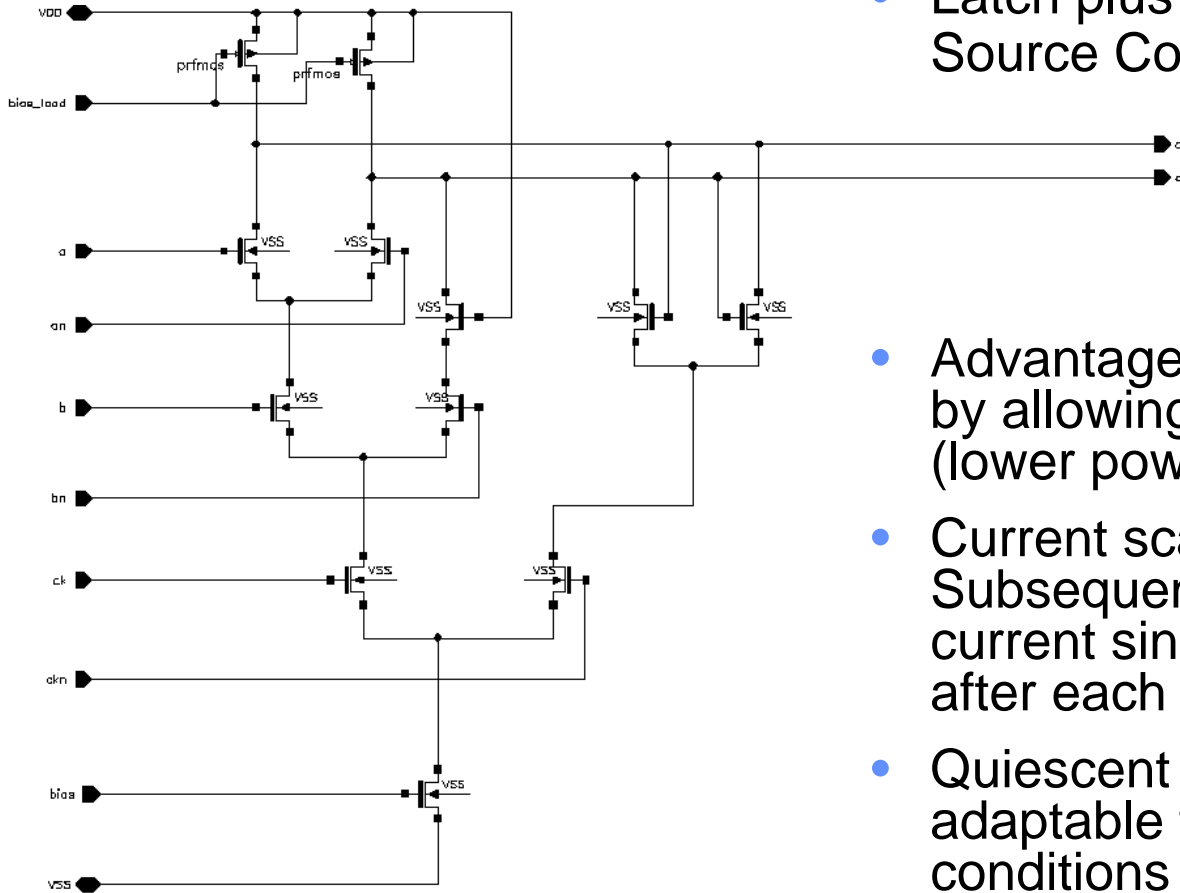
Adil Koukab (EPFL, Electronics Laboratories, Lausanne, Switzerland): "IST European project MuMoR - A multi-mode multi-band voltage controlled oscillator for 3G enhanced mobile phones", Workshop on low-power integrated circuits dedicated to 3G mobile phones, February 25-26, 2004, Lausanne, Switzerland.

Frequency divider

- Non-standard asynchronous divider utilizing concatenated 2/3 cells
- Divider cells can be enabled or disabled to obtain the desired division ratio
- Achieves ultra wide division range ($N = 64 \dots 16384$) and good scalability to support both Integer-N and Fractional-N operation



Frequency divider (contd.)



- Latch plus NAND gate in Source Coupled Logic
- Advantage of SCL against bipolar logic by allowing stacked logic (lower power consumption)
- Current scaling in SCL gates: Subsequent stages need less tail current since frequency is decreased after each stage
- Quiescent current and load impedance adaptable to process and temperature conditions

SCL latch with integrated AND gate

Frequency synthesizer summary

Parameter	Value	Unit	Notes
DC supply voltage	2.5	V	
DC supply current	2.2	mA	excl. VCO, DSM
VCO frequencies	3420 .. 4340	MHz	modulo-2 prescaler provides LO for IQ mixing
Divider ratio N	8550 .. 10850 85.5 .. 108.5		Integer-N mode Fractional-N mode
Reference frequency	200 20	kHz MHz	Integer-N mode Fractional-N mode
Phase noise	-119 -139 -150	dBc/Hz @ 600 kHz dBc/Hz @ 5 MHz dBc/Hz @ 20 MHz	based on VCO simulations (EPFL)
Silicon area	0.08	mm ²	PLL core
Process	BiCMOS7 (STM)		0.25μm BiCMOS

Conclusion

- Multi-architecture multi-mode frequency synthesizer
 - Covers wireless standards that show totally different requirements
 - Integer-N and Fractional-N operation
 - Switchable loop filter
 - Widely configurable frequency divider
- Implementation of a multi mode synthesizer for a direct-conversion RF front-end, supporting WCDMA / HSDPA and GSM 900 / 1800
- Multi-band Voltage Controlled Oscillator (VCO)
- Parametrizable asynchronous frequency divider
 - high modularity by cascaded chain of 2/3 divider cells
 - power optimization by combining different logic styles
- The design has been performed in close cooperation between EPFL (VCO) and Nokia (PLL)