# *Dynamic Supply RF PA (DSPA)*

Nicolas Schlumpf

`nicolas.schlumpf@epfl.ch`

Electronics Laboratory (LEG), Swiss Federal Institute of Technology, Lausanne (EPFL)

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# *Outline*

- Introduction
- RF DSPA Principle
- Impact of PA class on the DSPA
- Impact of modulator on the DSPA
- Modulator design
- System measurement
- RF DSPA simulation
- Conclusion

# *Introduction: RF PA constraints?*

- GSM (constant envelope)
  ⇒High efficiency RF PA
- UMTS (varying envelope)
  ⇒High efficiency & linearity RF PA
  - High linearity ⇒ Low IMs
  - High efficiency ⇒ Longer talk time
- **However** high efficiency & linearity not achievable with conventional PA.

## *Introduction: getting round the linearity-efficiency tradeoff*

1. Linearization (Feed-back, Polar & Cartesian loop, predistorsion, Feedforward...) ⇒ Mainly used when linearity is of first concern (base sation)
2. Efficiency improvement (Doherty, Kahn, EER & **DSPA**) ⇒ Mainly used to increase talk time and battery life time

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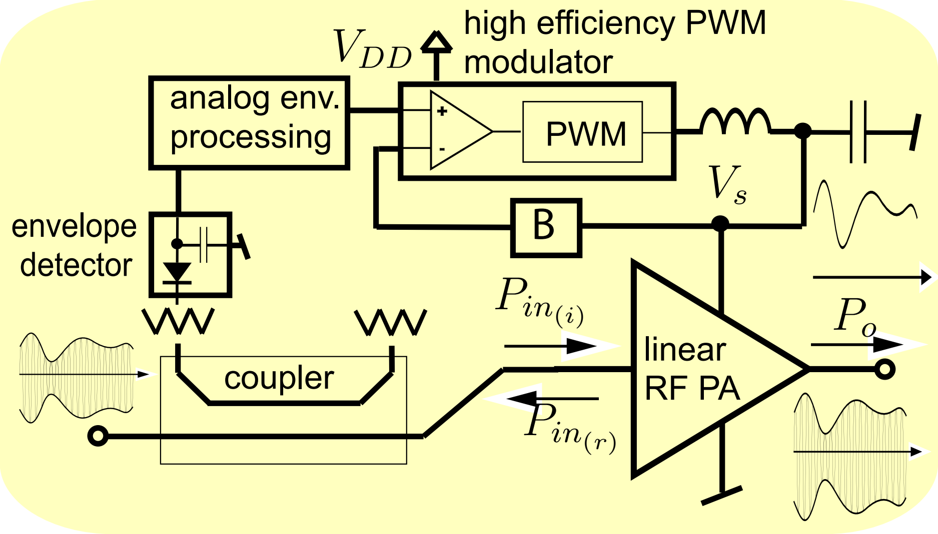
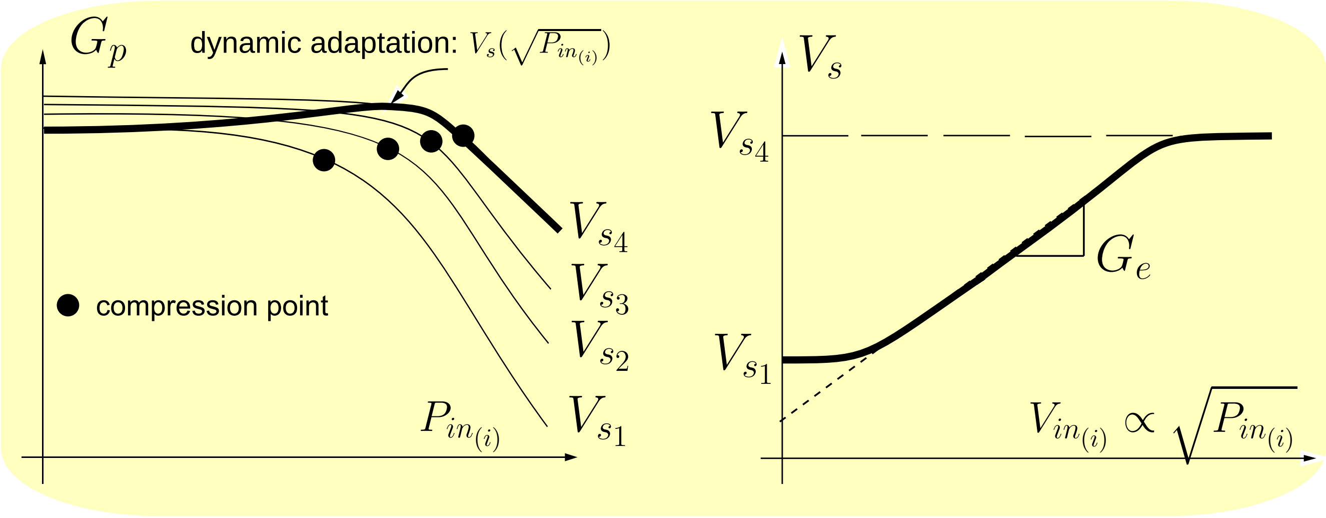
# *DSPA Principle: Schematic*

1. Assumption: RF PA output behaves like a current source⇒ compression is controlled with $V_s$
2. $P_o = P_{in_{(i)}} \cdot G_p$
3. Coupler & envelope detector $\propto \sqrt{P_{in_{(i)}}}$
4. Enveloppe amplification
5. High efficiency conversion into a PA varying supply ($V_s$)



# **DSPA principle:** $G_p(P_{in_{(i)}})$ **&** $V_s(\sqrt{P_{in_{(i)}}})$



- PA does not behave like an ideal current source $\Rightarrow \partial G_p / \partial V_s$
- Compression point $= f(V_s)$
- Dynamique adaptation $\Rightarrow V_s(\sqrt{P_{in_{(i)}}})$
- efficiency improvement: $\Delta_\eta \geq \frac{V_{s4}}{V_{s1}}$

- $V_{s_1} \geq V_{knee}$
- $V_{s_4} \leq V_{DD}$
- $V_s = G_e \cdot V_{in_{(i)}} + V_{knee}$

# DSPA Principle: Performances

1. Linked to the PA, its class acts on:
   - linearity
   - efficiency
   - power gain
   - DC or base-band current function of $P_{in_{(i)}}$
   - input impedance
   - output impedance
2. Linked to the modulator
   - its speed determines the maximum envelope BW
   - its efficiency determines the PA efficiency improvement

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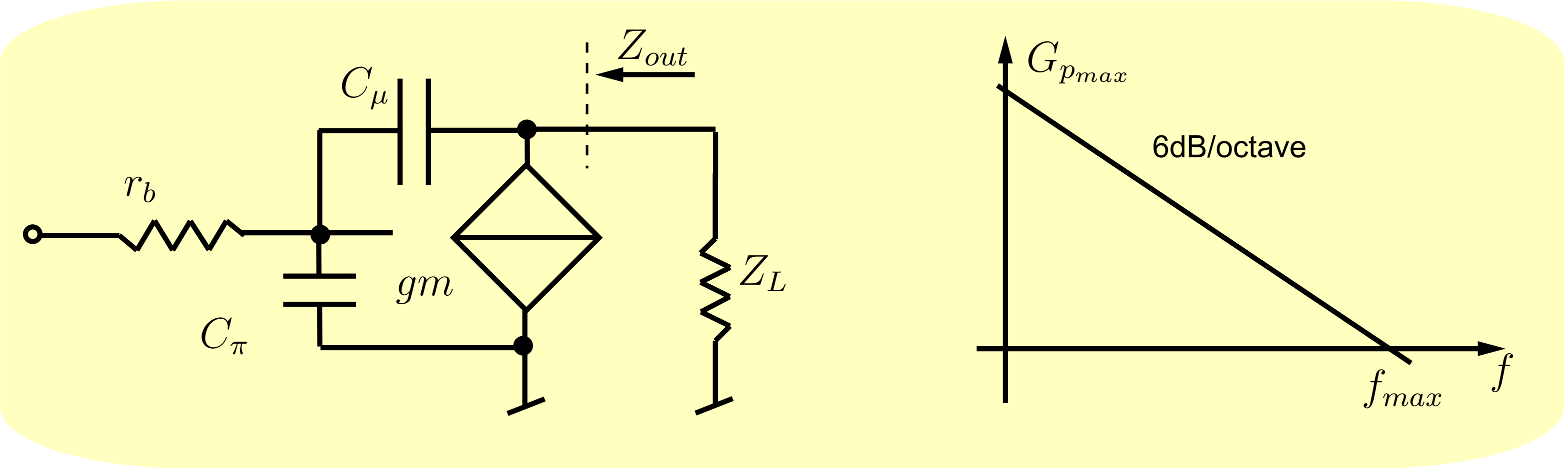
# *RF PA: RF PA classes*

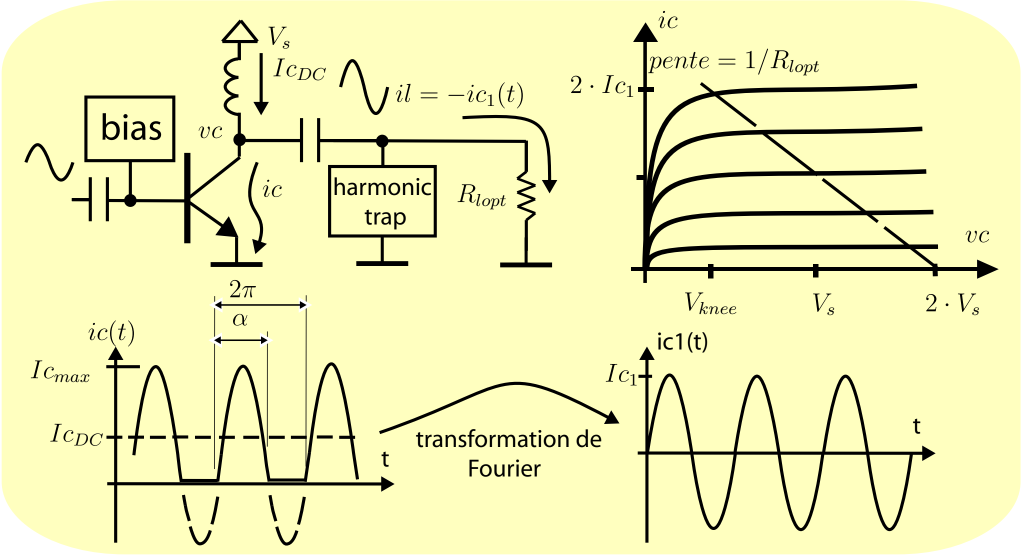
**goal:** determine which RF PA class is most appropiate for the DSPA

# RF PA: $G_p$ dependence versus $f$



- Miller Cap. $C_\mu \Rightarrow$ -6dB/oct
- $f_{max}$ technology dependent

# RF PA: $G_p$ at $P_{max}$ (load line)

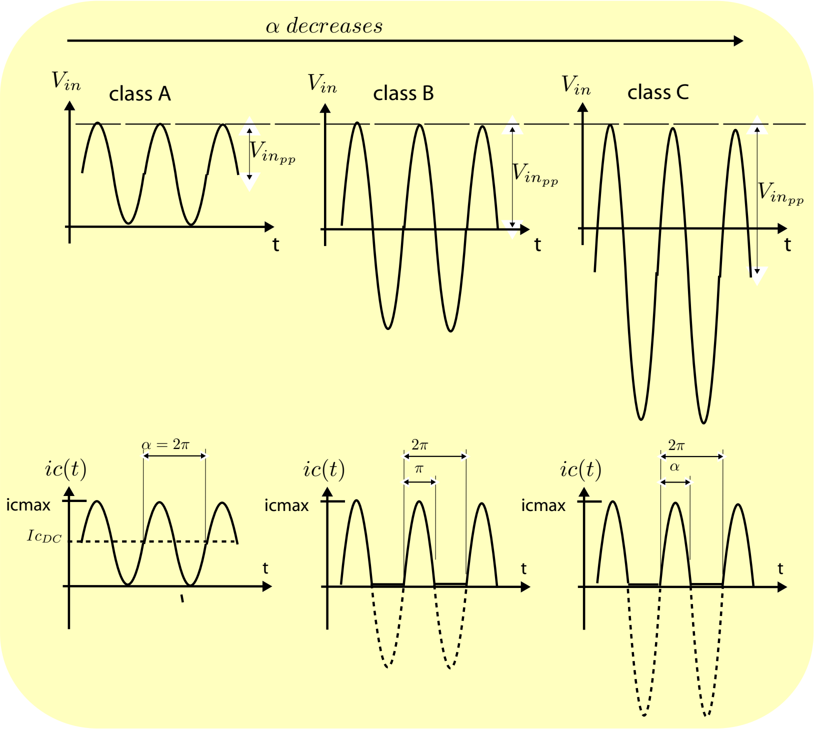


- Load line ⇒ Maximum fundamental swing:
  - voltage drain/collector: $2 \cdot V_s - V_{knee}$
  - current drain/collector: $Ic_{max}$ for any $\alpha$
- $Ic_1$ obtained by the mean of a filter
- $G_p = \frac{P_{out_1}}{P_{in_1}}$ only the fundamental is taken into account

# ***RF PA:*** $G_p$ ***dependence versus*** $\alpha$

PA assumptions:

- $$i_c = f(V_{in}) : \begin{cases} i_c = gm \cdot V_{in} & \text{if } V_{in} \geq 0 \\ i_c = 0 & \text{if } V_{in} < 0 \end{cases}$$
- PA RF input impedance constant over an RF cycle

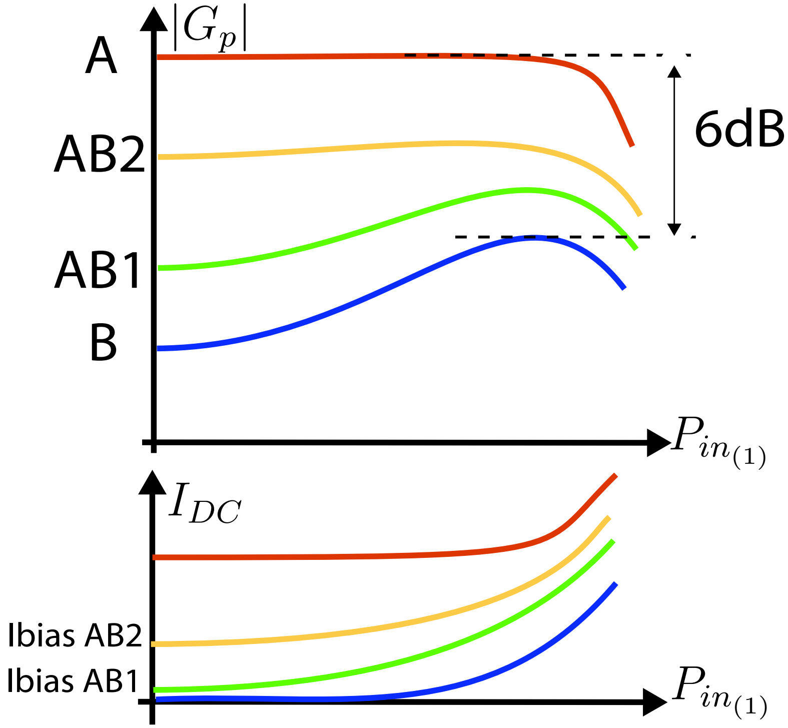


- $G_p$(class A)=$G_p$(class B)+$6dB$
- Class B & C barely used when $f$ approaches $f_{max}$

# RF PA: linearity vs $\alpha$

PA linearity linked to $\frac{\partial |G_p|}{\partial P_{in_{(1)}}}$ & $\frac{\partial \varphi(|G_p|)}{\partial P_{in_{(1)}}}$

(AM-AM) (AM-PM)



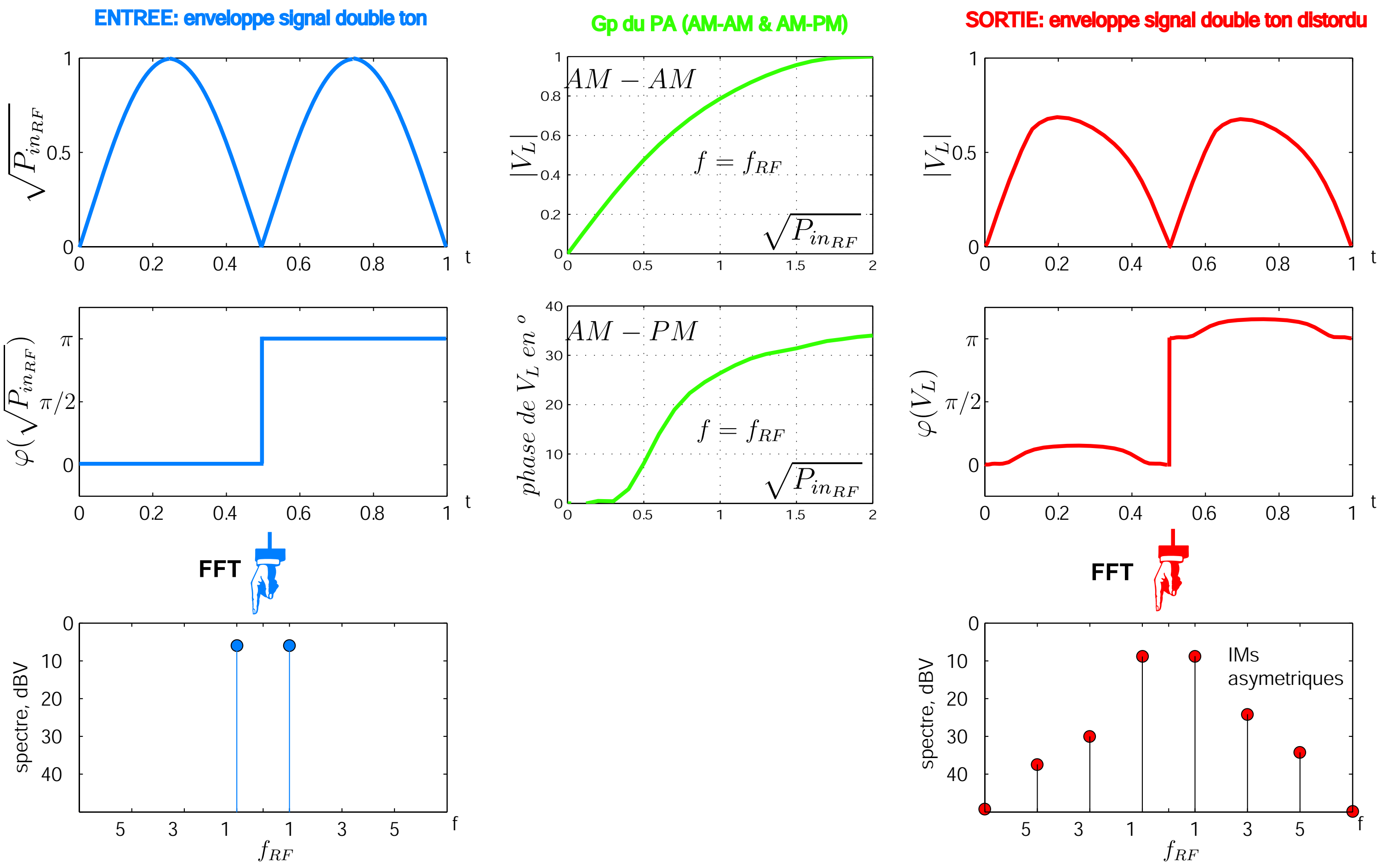
- classes A & AB-2 are considered linear, $G_p$ independent of $P_{in}$
- **linear class AB: example AB-2**
  - gain drops due to conduction angle reduction
  - gain increases due to an increase of current drawn by the PA
  - **compensation** $\Rightarrow$**linear class AB**

# *RF PA: linearity degradation from bias point modulation*

PA assumptions: input & output impedance normalized to $1\Omega$

bias point modulation $\rightarrow G_p$ power gain modulation $(20\%, \varphi = 45^o)$

$$V_L = \sqrt{P_{in_{RF}}} \cdot G_p \cdot (1 - 0.2|\sin(2\pi t + \pi/4)|)$$



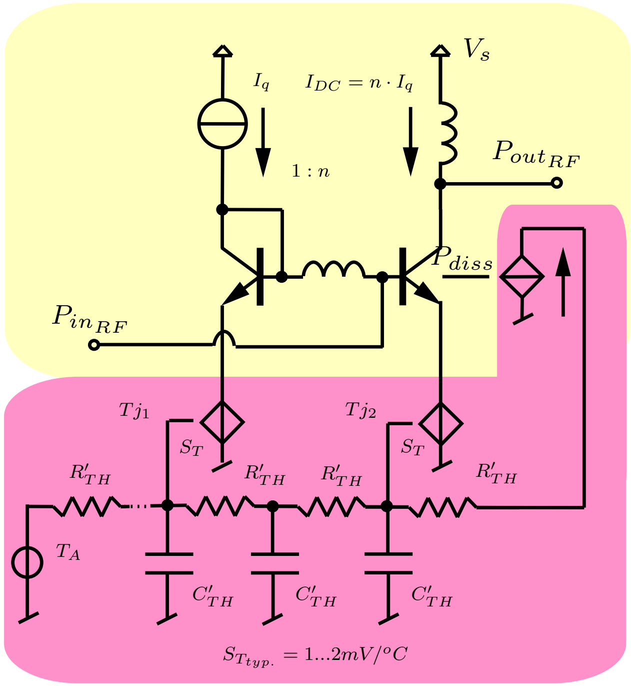
# *RF PA: bias point modulation and linearity degradation*

**Origin: power supply fluctuations & dynamic variations of $Tj$**

efficiency improvement ⇒ $P_{DC}(PA) = f(P_{in_{RF}})$

&

varying RF envelope ⇒ variations of $P_{in_{RF}}$



## Current mirror biasing scheme

$$P_{diss_{DSPA}} \approx V_s(P_{in_{RF}}) \cdot I_{DC}(P_{in_{RF}}) - P_{out_{RF}}$$

⇒ $P_{diss}$ dependent and in phase with RF enveloppe

## Electrothermal model & thermal flow

⇒ bias point modulation $\propto |\Delta Tj_1 - \Delta Tj_2|$

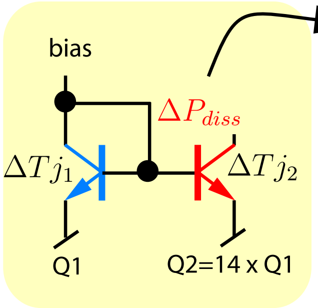
⇒ Transfer function $\frac{\Delta Tj_1}{\Delta P_{diss}}$? & $\frac{\Delta Tj_2}{\Delta P_{diss}}$?

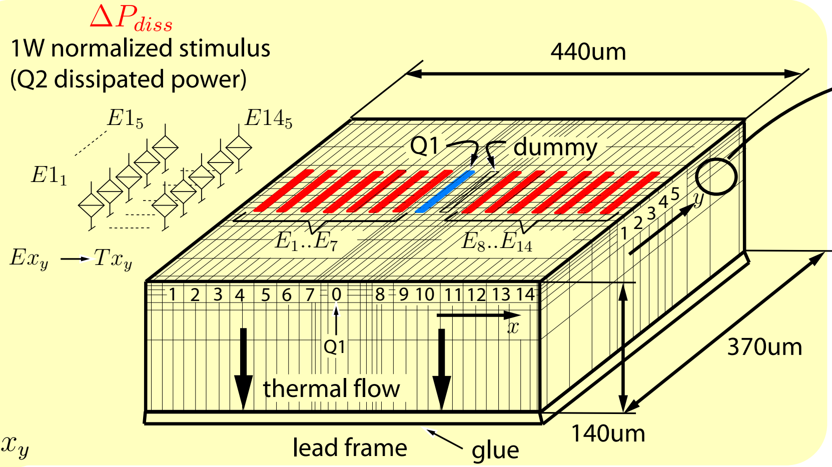
## How to minimize bias point thermal modulation

⇒ Thermal impedance as low as possible

⇒ Increase thermal coupling

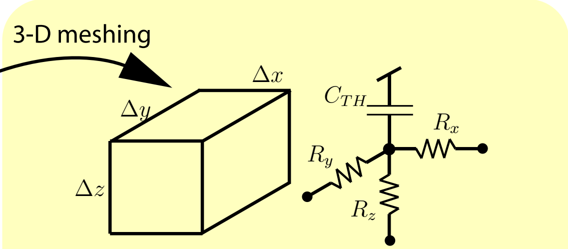
# *PA RF: Current mirror bias & thermal modulation ($\Delta Tj_2 - \Delta Tj_1$): transfer function $\frac{\Delta Tj_1}{\Delta P_{diss}}$ & $\frac{\Delta Tj_2}{\Delta P_{diss}}$*





$$\Delta Tj_1 = \frac{1}{5}\sum_{y=1}^{5} \Delta T0_y$$

$$\Delta Tj_2 = \frac{1}{14\times 5}\sum_{x=1}^{14}\sum_{y=1}^{5} \Delta Tx_y$$

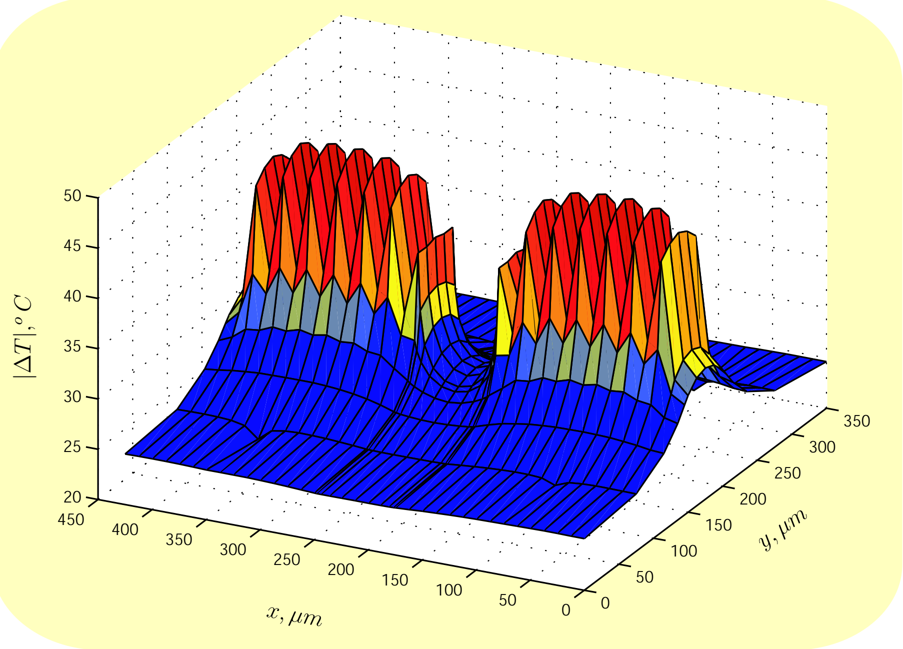


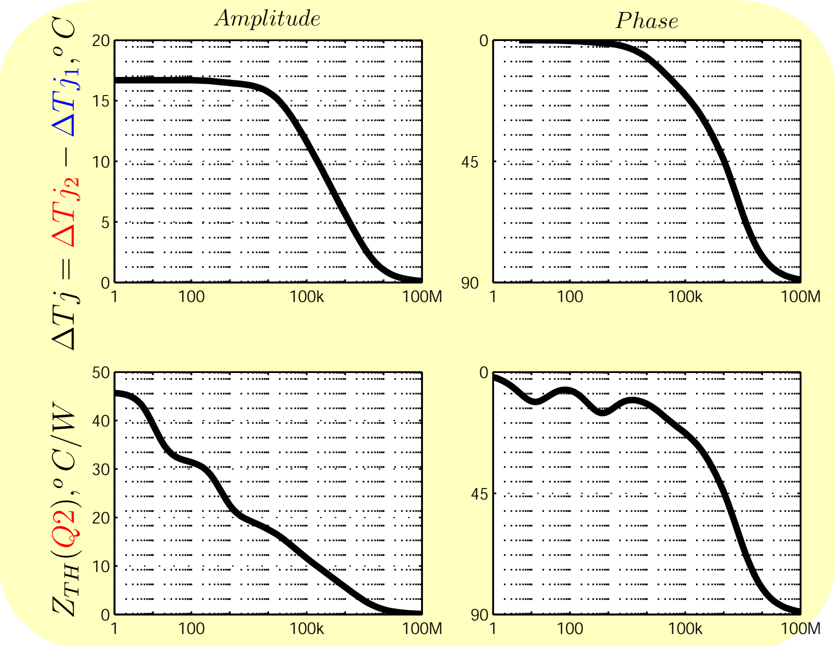
$$C_{TH} = c_{Si}\rho_{Si}\Delta x\Delta y\Delta z$$

$$R_x = \frac{\Delta x}{\lambda_{Si}\Delta y\Delta z}$$

$$R_y = \frac{\Delta y}{\lambda_{Si}\Delta x\Delta z}$$

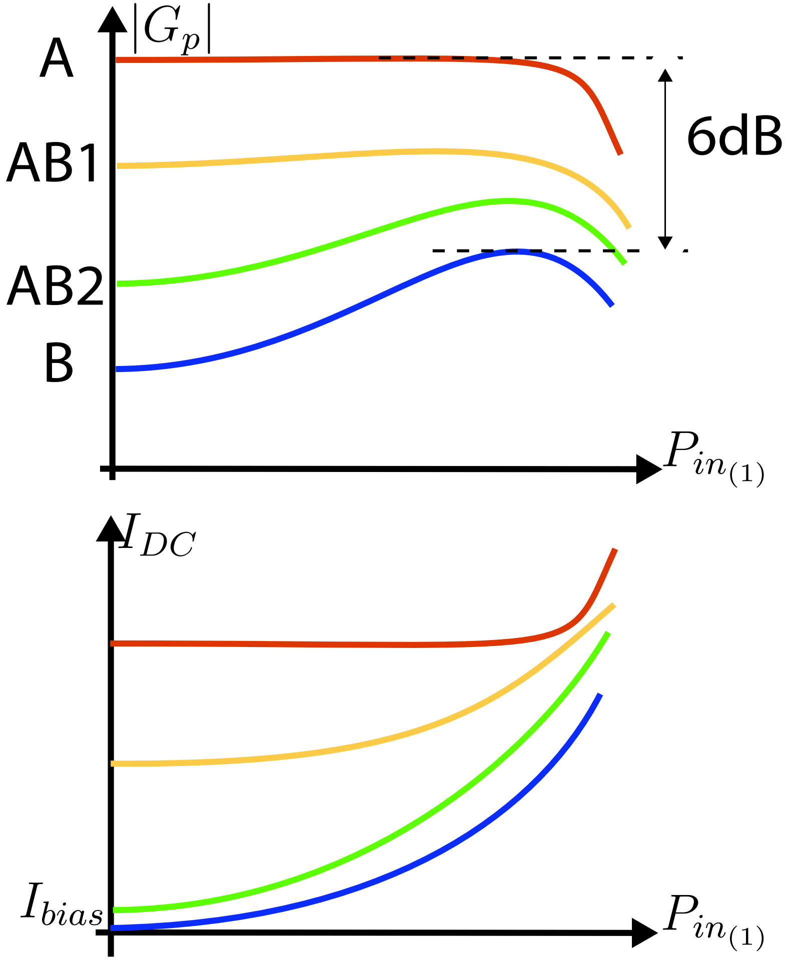
$$R_z = \frac{\Delta z}{\lambda_{Si}\Delta x\Delta y}$$





# RF PA: PA as load for the modulator

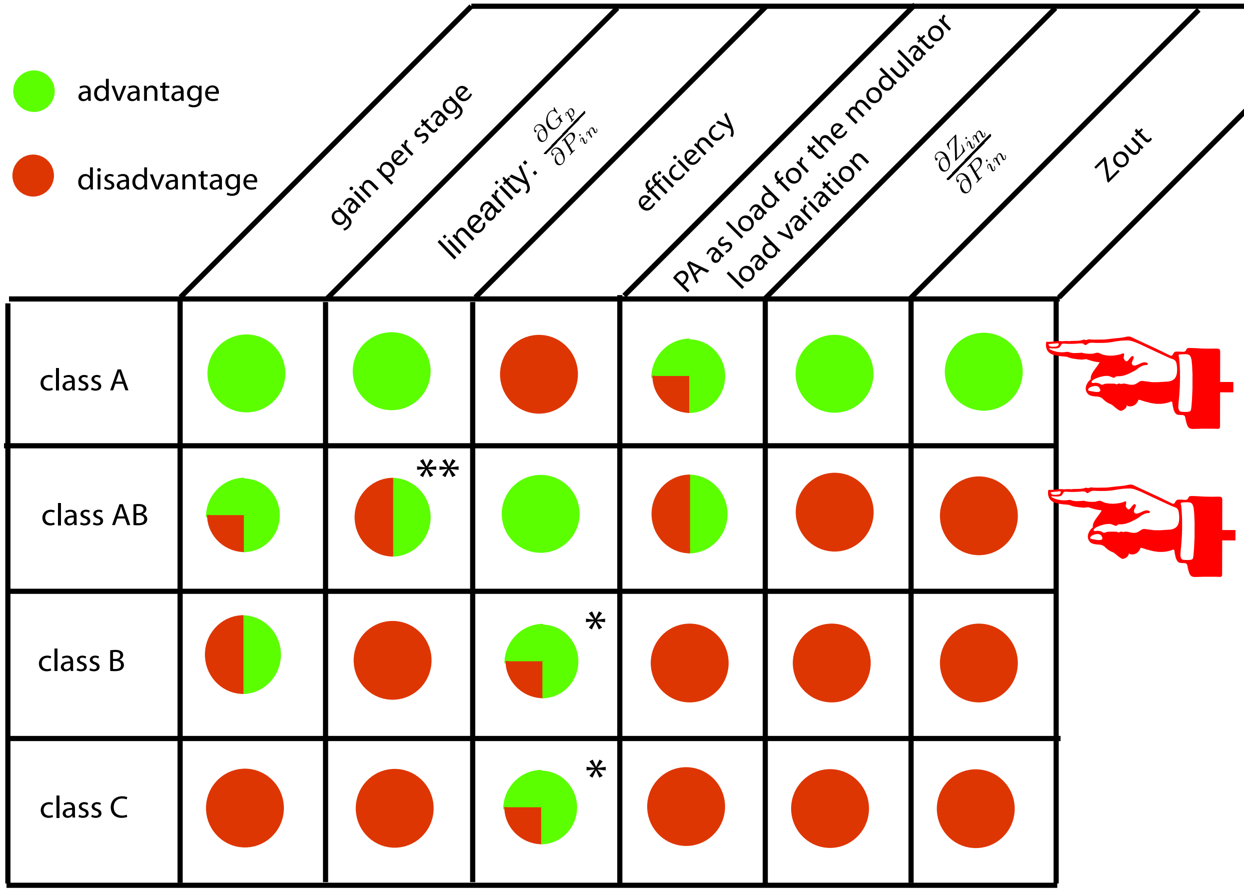
Important criteria for modulator speed



- **DSPA Principle:** $\sqrt{P_{in}} \nearrow \Rightarrow V_s \nearrow$
- $\Rightarrow$ **PA as load for the modulator:**

  $\frac{\partial V_s}{\partial I_{DC}}$ non linear, especially when $\alpha < 2\pi$

# *RF PA: appropriate PA class for the DSPA*



🟢 advantage

🔴 disadvantage

| | gain per stage | linearity: $\frac{\partial G_p}{\partial P_{in}}$ | efficiency | PA as load for the modulator<br>load variation | $\frac{\partial Z_{in}}{\partial P_{in}}$ | Zout |
|---|---|---|---|---|---|---|
| class A | 🟢 | 🟢 | 🔴 | 🟢🟢🟢🔴 | 🟢 | 🟢 |
| class AB | 🟢🟢🟢🔴 | 🔴🟢 ** | 🟢 | 🔴🟢 | 🔴 | 🔴 |
| class B | 🔴🟢 | 🔴 | 🟢🟢🟢🔴 * | 🔴 | 🔴 | 🔴 |
| class C | 🔴 | 🔴 | 🟢🟢🟢🔴 * | 🔴 | 🔴 | 🔴 |

Better properties except efficiency
**DSPA Goal:** increase efficiency without linearity degradation

**Major drawback of Class AB & DSPA:** envelope BW limitation due to non linear load variation s

* efficiency depends on $G_p$: $PAE = \frac{P_{out}}{P_{DC}+P_{in}} = \frac{1}{\frac{1}{\eta_C}+\frac{1}{G_p}}$

** depends on bias point scheme and PA thermal properties

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# *Modulator: constraints*

## Speed constraints

- *Envelope BW:* $f_{env}$ typ. 1 to 4MHz (W-CDMA)
- *Modulator switching frequency:* $f_s \geq 10 \times f_{env}$ (residual ripple)

## PA as load constraints

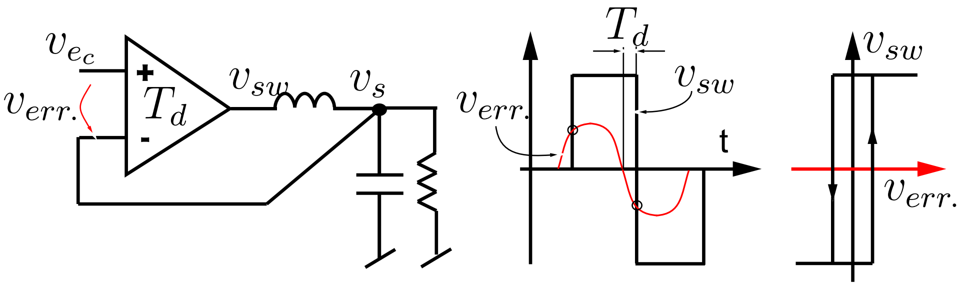
- *PA as load for the modulator depends on* $f_{env}$
- *PA as load for the modulator depends on* $P_{in_{RF}}$ *even when* $\alpha = 2 \cdot \pi$

  $\Rightarrow$ exponential or quadratic laws non-linearity

  $\Rightarrow$ output power compression

# *Modulator: solutions to the constraints(1)*

## Speed: sliding mode regulator



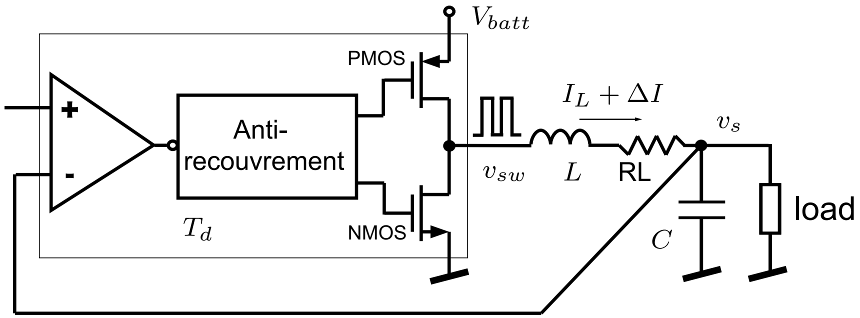
- ✓ self oscillating system: $T_d$ & LC filter determine $f_s$
- ✓ $t_{r_{syst.}} = t_{r_{LC}}$
- ✓ step response requires critical damping $\delta_{LC} \approx 0.7$
- ✓ No limitation of the Duty Cycle (DC)

## Sliding mode $\rightarrow$ bounded error

- ✓ $T_d$ acts as an hysteresis

# Modulator: solutions to the constraints(2)

**non linear load: inductor limits the current supplied to the load**



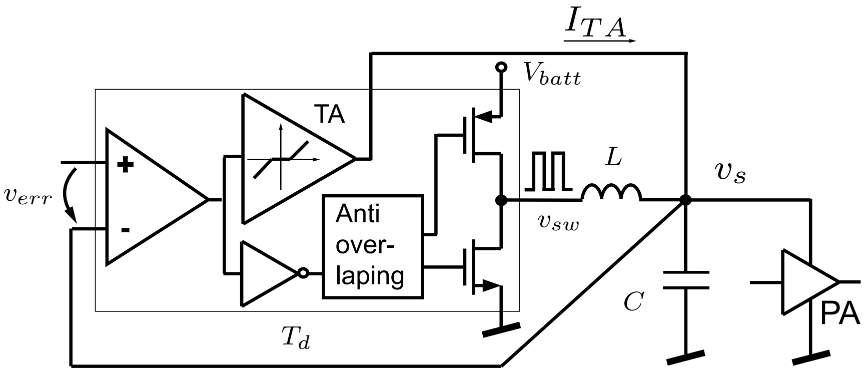
**Limitation:** $\frac{\Delta I}{\Delta t} \leq \frac{v_{sw} - v_s}{L}$

**Increasing** $\frac{\Delta I}{\Delta t}$

- ▷ $\Delta t \searrow \Rightarrow f_s \nearrow$ then $T_d \searrow$
- ▷ $\Delta I \nearrow \Rightarrow L \searrow$ Increase of losses ($\Delta I^2$)

**Decreasing $L$ is not the right solution**

**non linear load: TA supplied compensating current**



- $I_{TA} = G_m \cdot v_{err}$ if $v_{err} > v_{s_{ripple}}$
- $I_{TA} = 0$ if $v_{err} \leq v_{s_{ripple}}$
- For a linear PA → $\eta$ almost not affected

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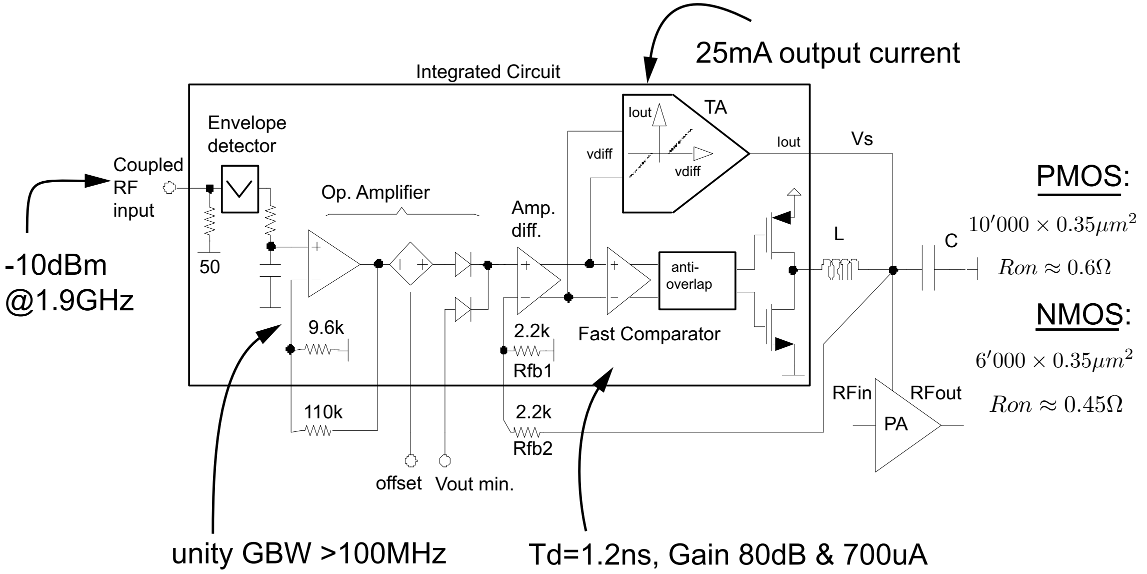
# *Modulator design*

## RF PA off-chip

- Noisy environnement (switching supply)
- RF PA die & package optimized:
  - Die made thinner ($140\mu m$): $Z_{th} \searrow$ & parasitic connection inductance $\searrow$
  - Optimized package (parasitic inductance $\searrow$ & thermal impedance $\searrow$)

## 0.35$um$ CMOS modulator



25mA output current

-10dBm @1.9GHz

unity GBW >100MHz

Td=1.2ns, Gain 80dB & 700uA

PMOS:

$10'000 \times 0.35\mu m^2$

$Ron \approx 0.6\Omega$

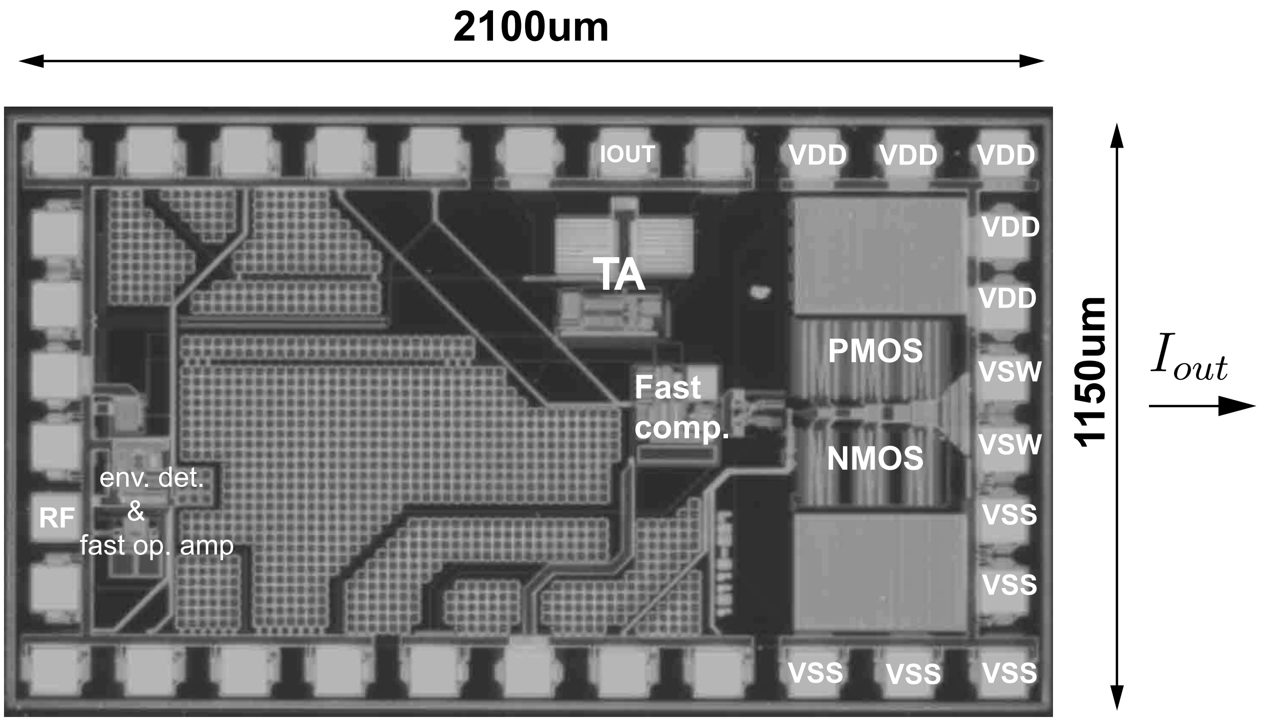
NMOS:

$6'000 \times 0.35\mu m^2$

$Ron \approx 0.45\Omega$

- supply voltage: 3.3V
- overall delay: $T_d \approx 4ns$
- efficiency$\approx 85\%$ $(100mA, 1.25V \& f_s = 20MHz)$

# 0.35$um$ CMOS modulator Photo



- Large number of pads (internal nodes verification)
- Die size can be halved
- $\Delta V_{DD},\ \Delta V_{SS} \approx L_{bond} \cdot \frac{\Delta I_{out}}{\Delta t} \approx 1nH/5 \cdot \frac{100mA}{500ps} \approx 50mV$

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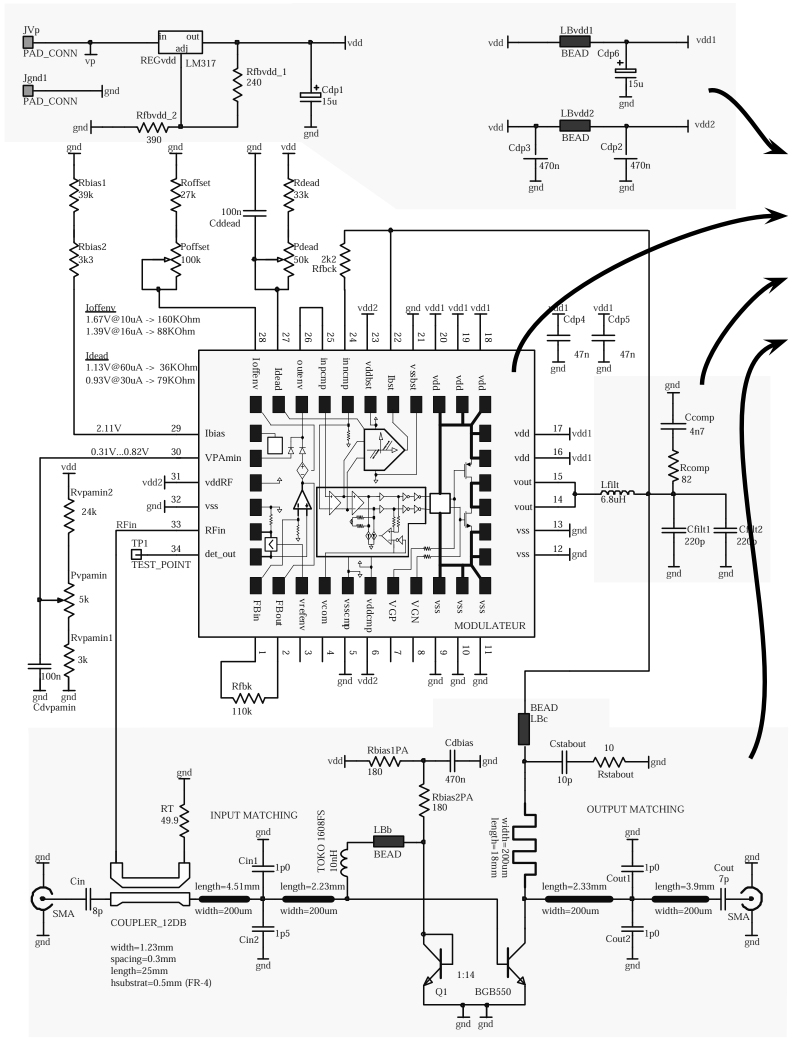
# System measurement: evaluation circuit



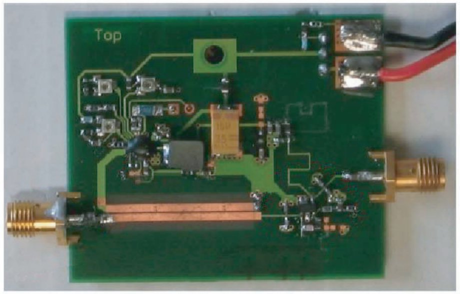
Power supply

Modulator

LC output filter

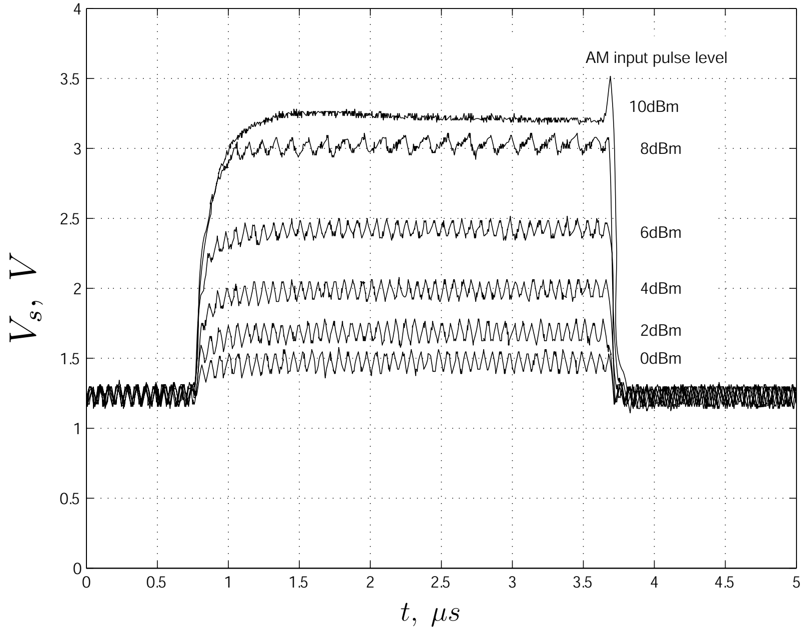
RF PA

- test frequency: 1.9GHz
- modulator supply voltage: 3.3V
- comparative measurements of DSPA with constant supply PA (3.3V)



# System measurement: pulsed AM

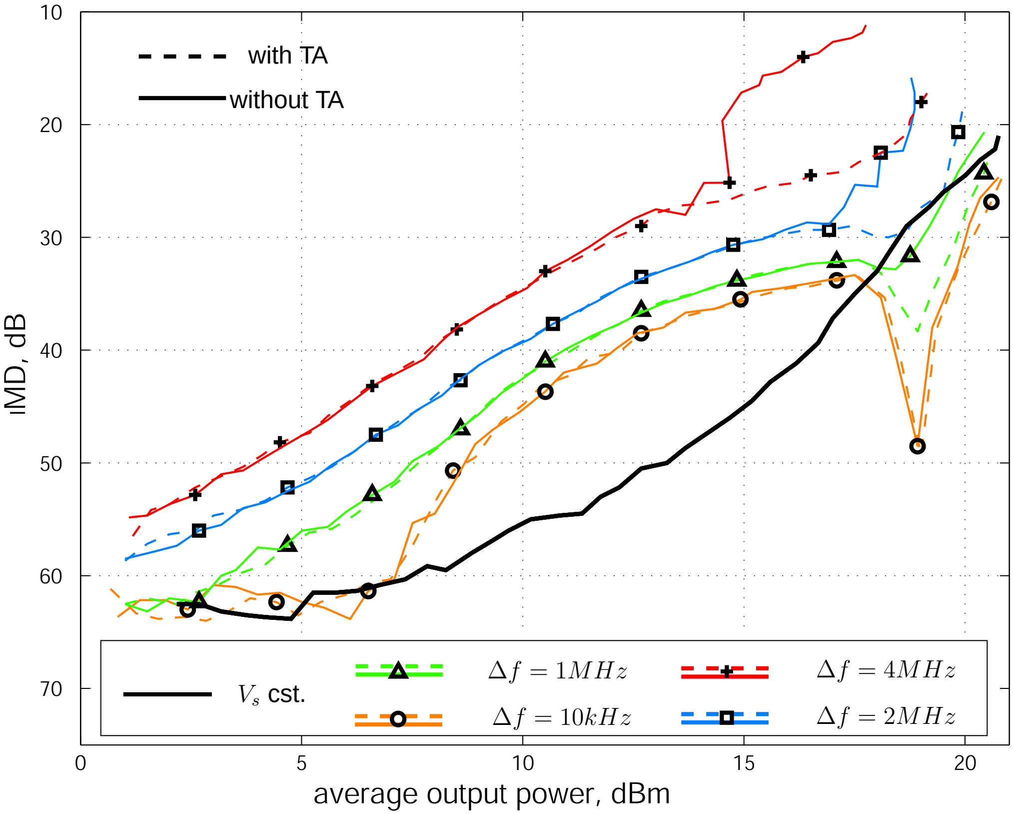
**objective**: determine the step response of the PA supply ($V_s$)



- $V_{s_{min.}}$: $1.25V$
- typical residual ripple: $180mVpp$
- switching frequency (DC=50%): $16MHz$
- test frequency: $1.9GHz$
- RF envelope rise time: $30ns$
- average $V_s$ rise time: $t_{r_{V_s}} < 200ns$
- $BW_{modulator} \approx \frac{0.35}{t_{r_{V_s}}} \approx 2MHz$

# System measurement: double tone linearity test

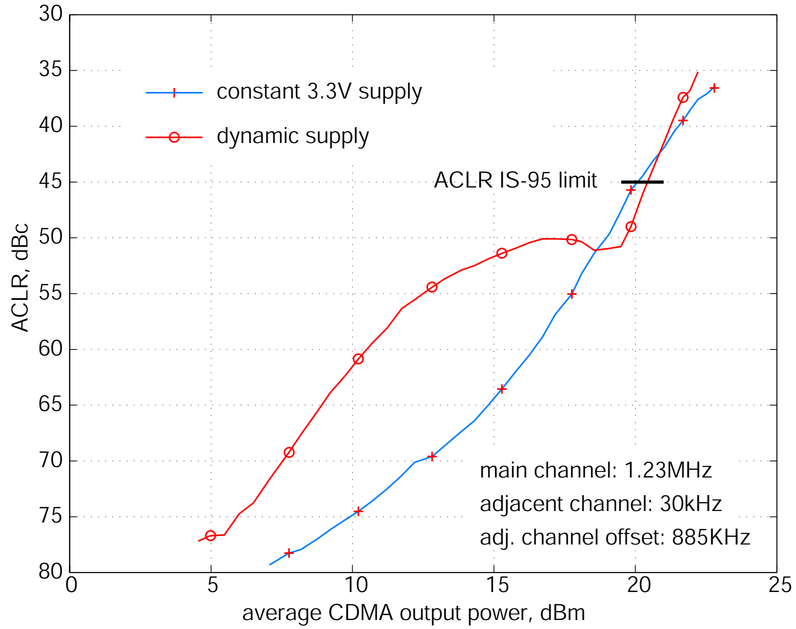
**objective:** highlight linearity degradation with RF envelope frequency

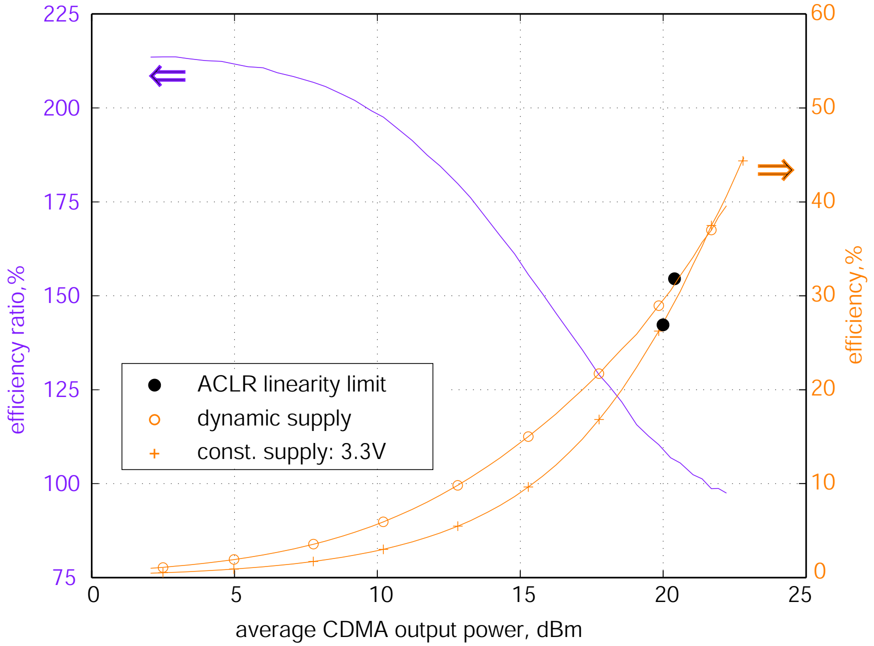


- $\Delta f \approx$ envelope BW
- tone frequencies: $1.9GHz \pm \frac{\Delta f}{2}$
- linearity=f($\Delta f$, $P_{out}$)
- degraded linearity $f > 2MHz$
- TA useful for high output power levels
- TA useful for $\Delta f > 10kHz$

# *System measurement: IS-95 CDMA signal*

**objectives**: DSPA linearity (ACLR) & efficiency with respect to constant supply PA





- Maximum power @ ACLR limit:
  - DSPA: 21dBm
  - PA 3.3V: 20dBm
- DSPA: max. efficiency improvement 210%

- maximum efficiency @ ACLR limit:
  - DSPA: 32%
  - PA 3.3V: 27%
- DSPA: better efficiency & linearity at high output power

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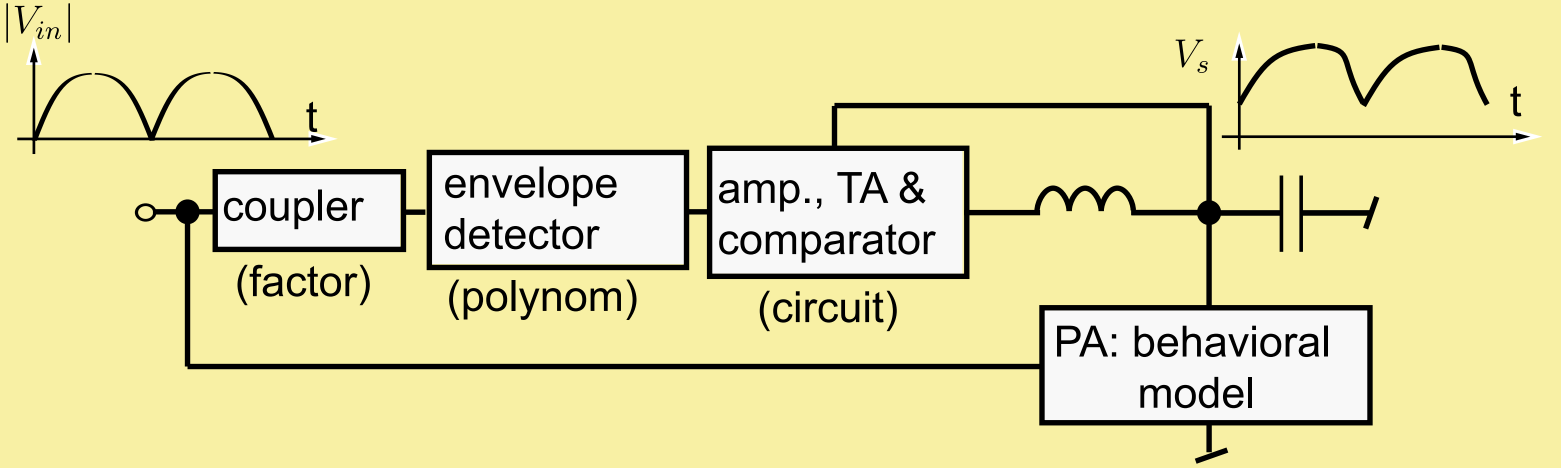
# *DSPA Simulation: difficulty*

**Objective: DSPA linearity prediction** linearity=$f(P_{in},\ f_{env.})$

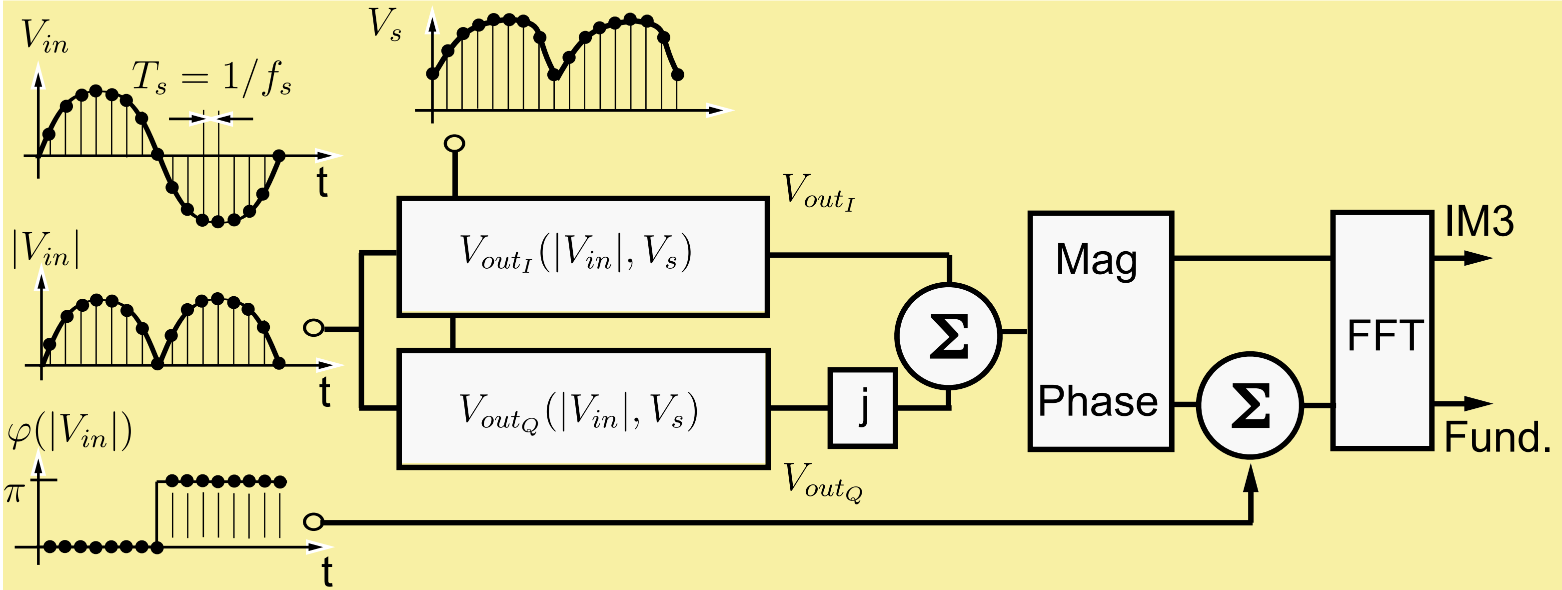
- "transient" simulation type:
  - RF cycle makes simulation time step small
  - long simulation time
  - lack of non linear RF power transistor models
- Harmonique balance & Envelope simulation
  - PWM modulation = non linear process
  - poor convergence
- **Two stages DSPA simulation**
  - Base-band simulations
  - No carrier $\Rightarrow$ save simulation time

## *DSPA Simulation: stages 1 & 2 for a double tone signal*

Stage n°1: transient simulation. Objective: getting Vs



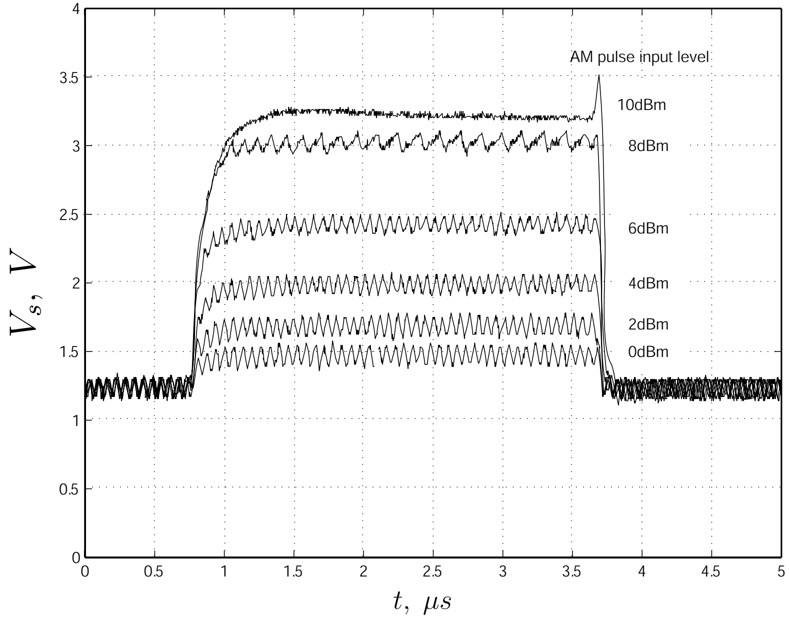
Stage n°2: envelope simulation. Objective: getting IMs products



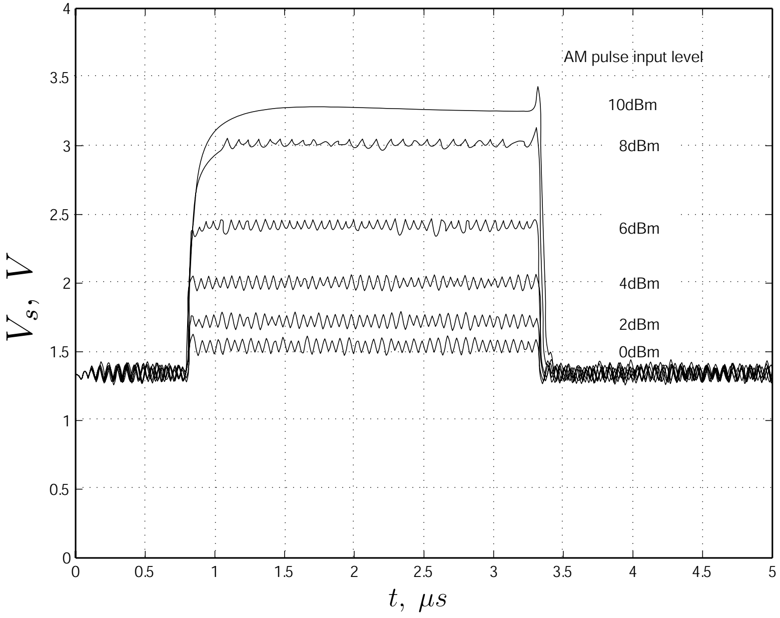
polynoms $V_{out_I}(|V_{in}|, V_s)$ & $V_{out_Q}(|V_{in}|, V_s)$ extracted from AM-AM & AM-PM measurements

# DSPA simulation: stage 1, simulation & measurement comparison (pulsed AM)

measurement

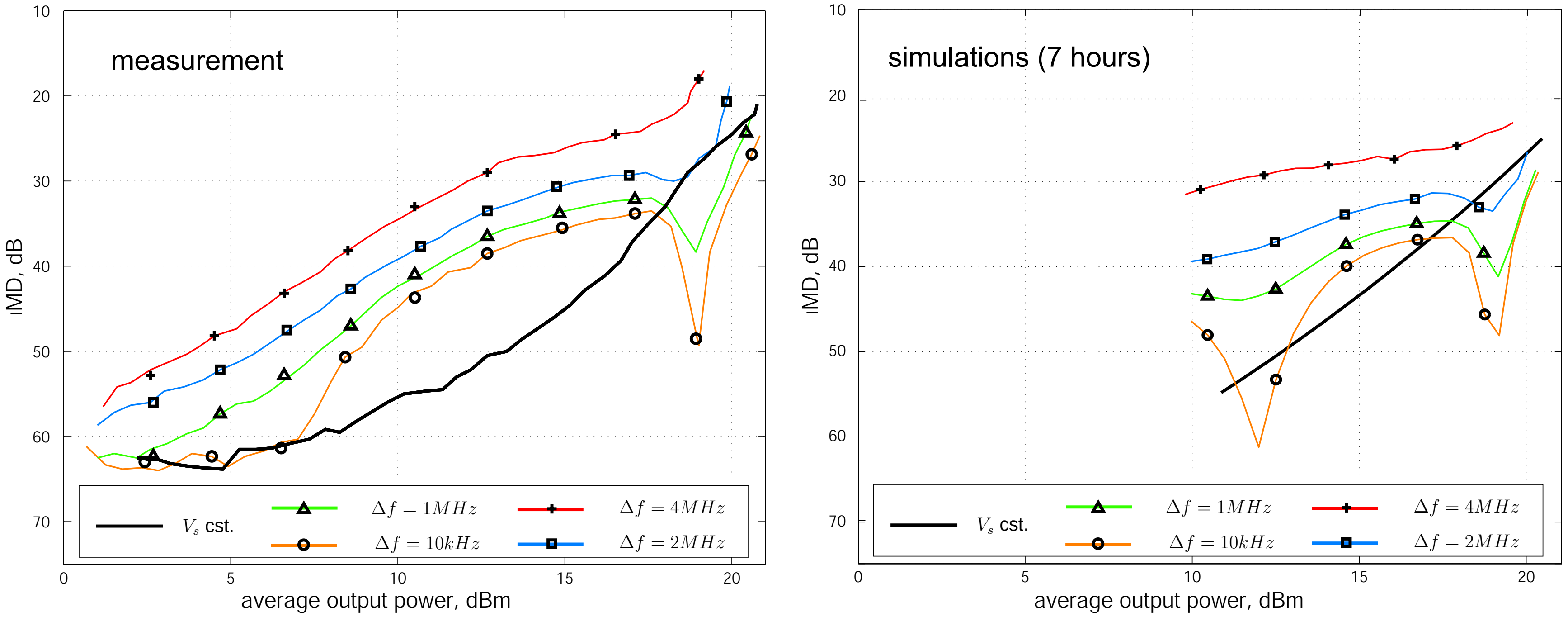


simulation (stage 1)



- similar measurement-simulation responses
- differences: rise time & ripple

# *DSPA Simulation: stages 1+2, double tone signal*



- similar measurement-simulation responses
- differences:
  - better simulated IMDs (about 2dB)
  - long simulation time makes differences difficult to understand

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# Conclusion

## *DSPA measurements*

- efficiency improvement in the PA linear range up to 210%
- linearity improvement at high output power

- efficiency and linearity maintained for RF envelope frequency up to 2MHz

**For more details, please refer to the following article:**

N. Schlumpf, M. Declercq and C. Dehollain, *A fast modulator for dynamic supply linear*

*RF power amplifier*,

IEEE Journal of Solid-State Circuits, Vol. 39, N0 7, July 2004, pp. 1015-1025