



RF Digital Transceiver for Impulse Radio Ultra Wide Band Communications

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STMicroelectronics

Presentation Outline

- ▣ UWB for Wireless Communications
- ▣ STM UWB Architecture Principles
- ▣ Rx Architecture
- ▣ Tx Architecture
- ▣ Multiphase PLL: Timing Accuracy
- ▣ Coexistence Issues

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Why is UWB Attractive?

$$C = B \log_2 \left(1 + \frac{P}{BN_0} \right)$$

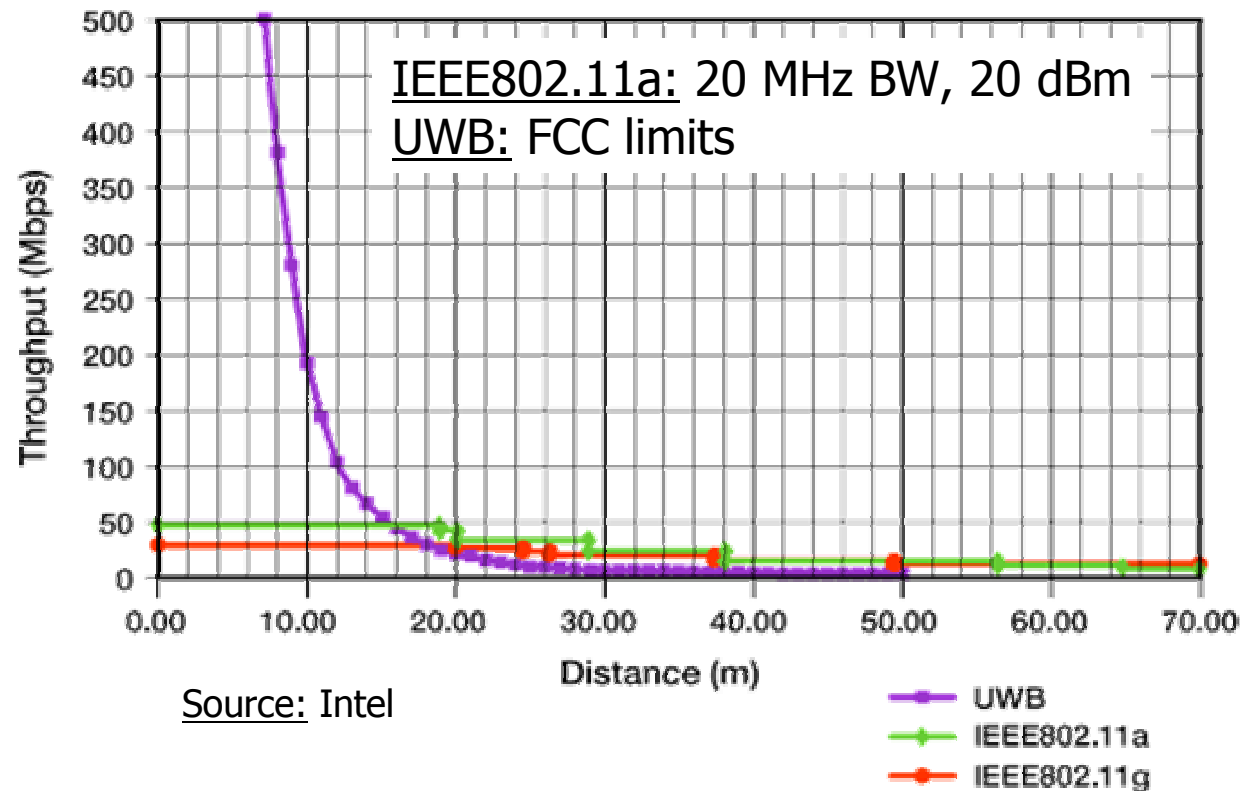
Where:

C = Channel Capacity (bits/sec)

B = Channel Bandwidth (Hz)

P = Received Signal Power (watts)

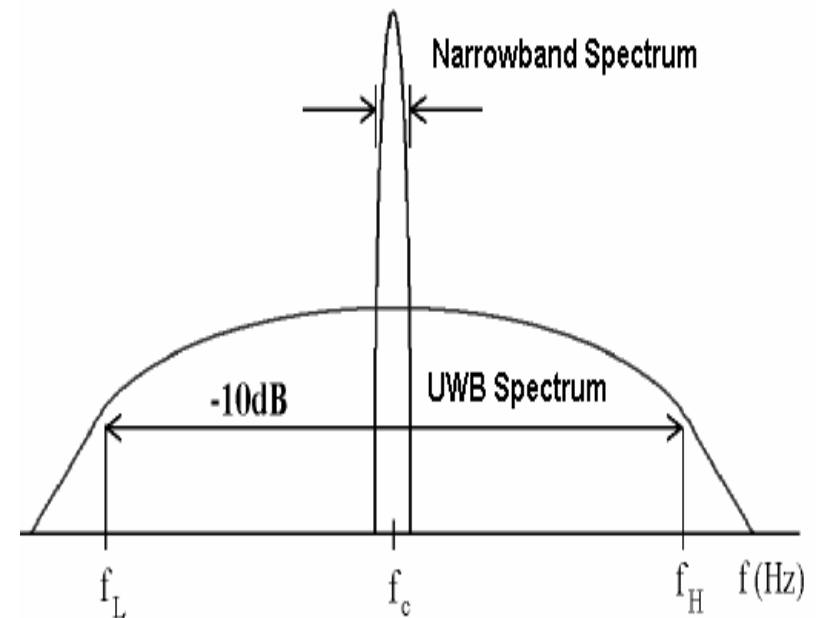
N_0 = Noise Power Spectral Density (watts/Hz)



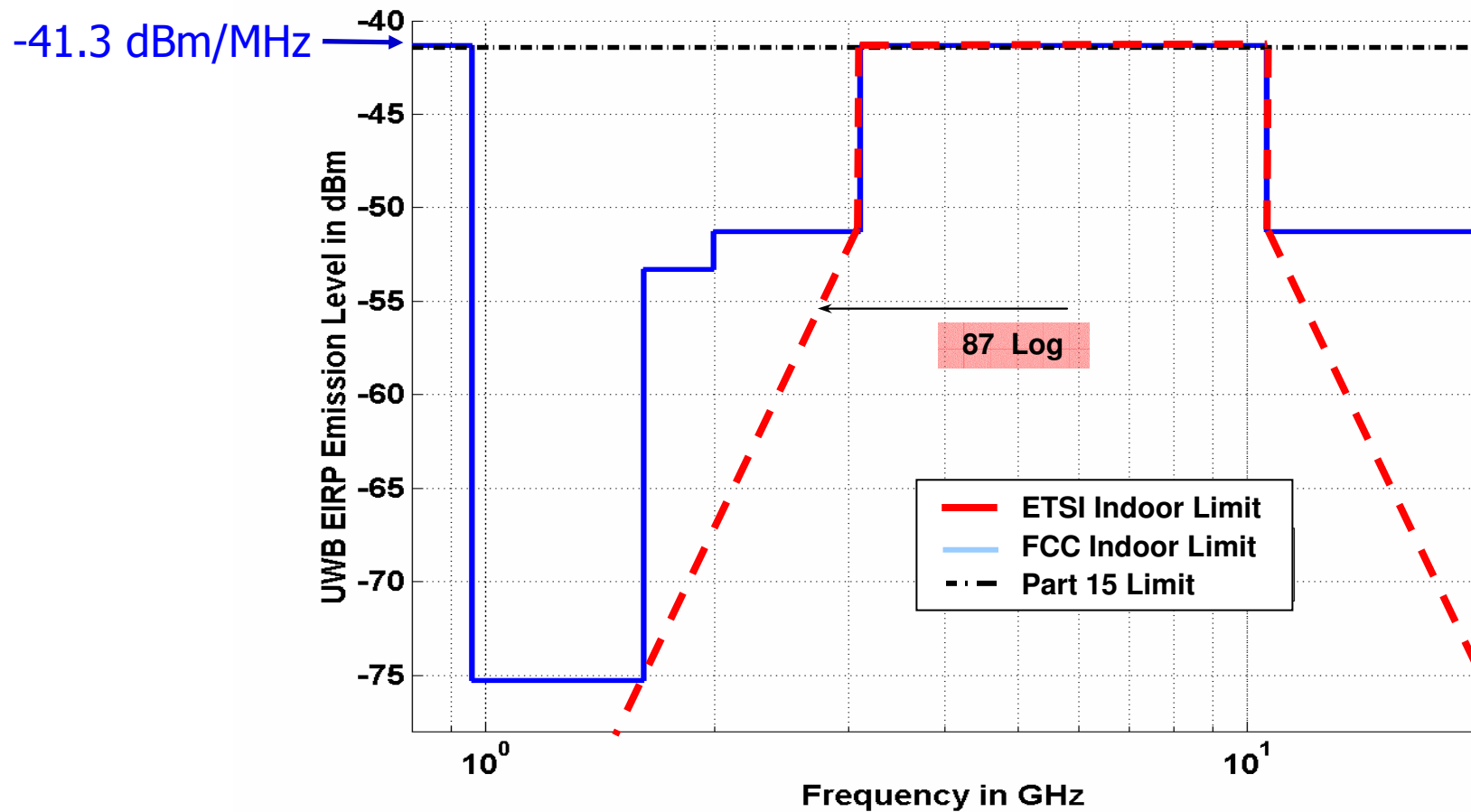
- UWB for High Data Rate at Short-Range -

UWB Emission - FCC Definition

- Bandwidth at -10 dB : $B_{-10dB} = (F_H - F_L)$
- Center Frequency : $F_c = \frac{(F_H + F_L)}{2}$
- Fractional Bandwidth : $\frac{B_{-10dB}}{F_c} \geq 0.2$
- If $F_c > 2.5$ GHz : $B_{-10dB} \geq 500MHz$

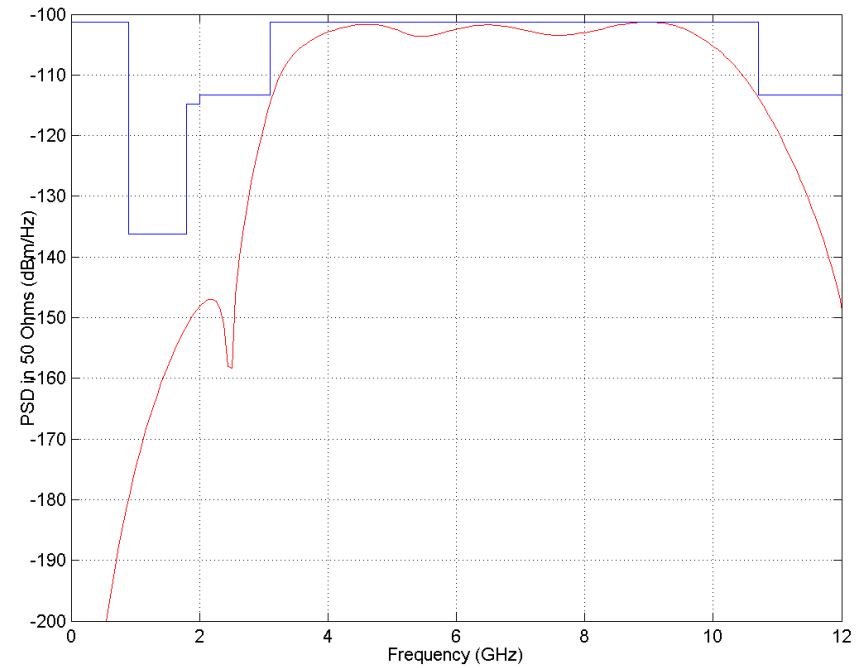
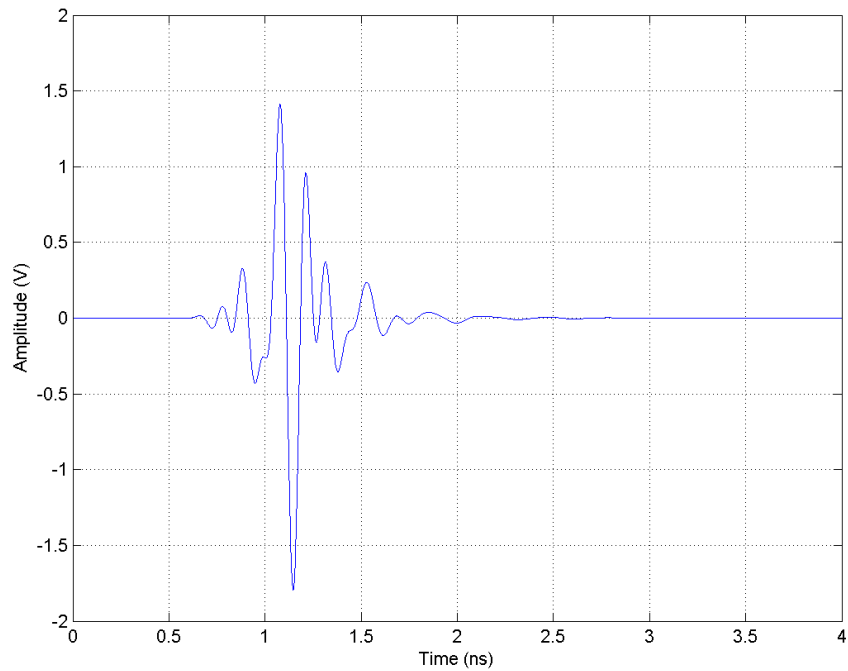


Indoor UWB Emission Mask



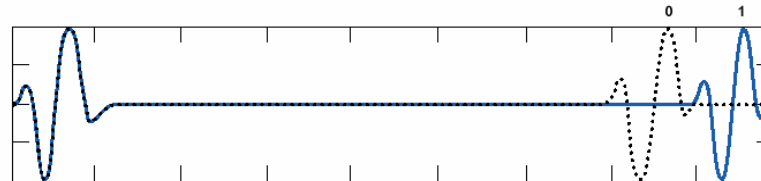
- UWB mask permits to access 7.5 GHz of unlicensed spectrum: 3.1 GHz to 10.6 GHz -

UWB Spectrum with Very Short Pulse

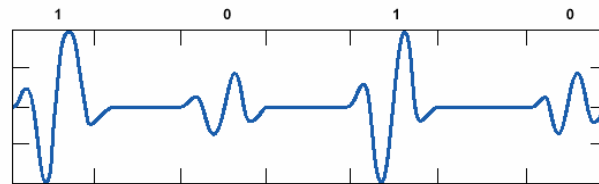


Pulse Modulation Techniques

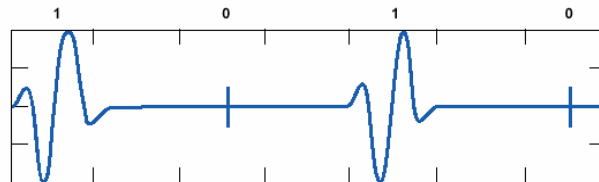
Pulse Position Modulation



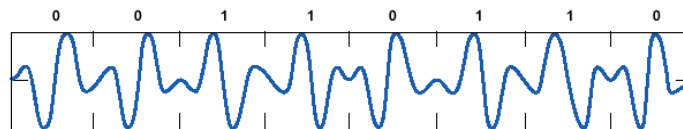
Pulse Amplitude Modulation



On-Off Keying



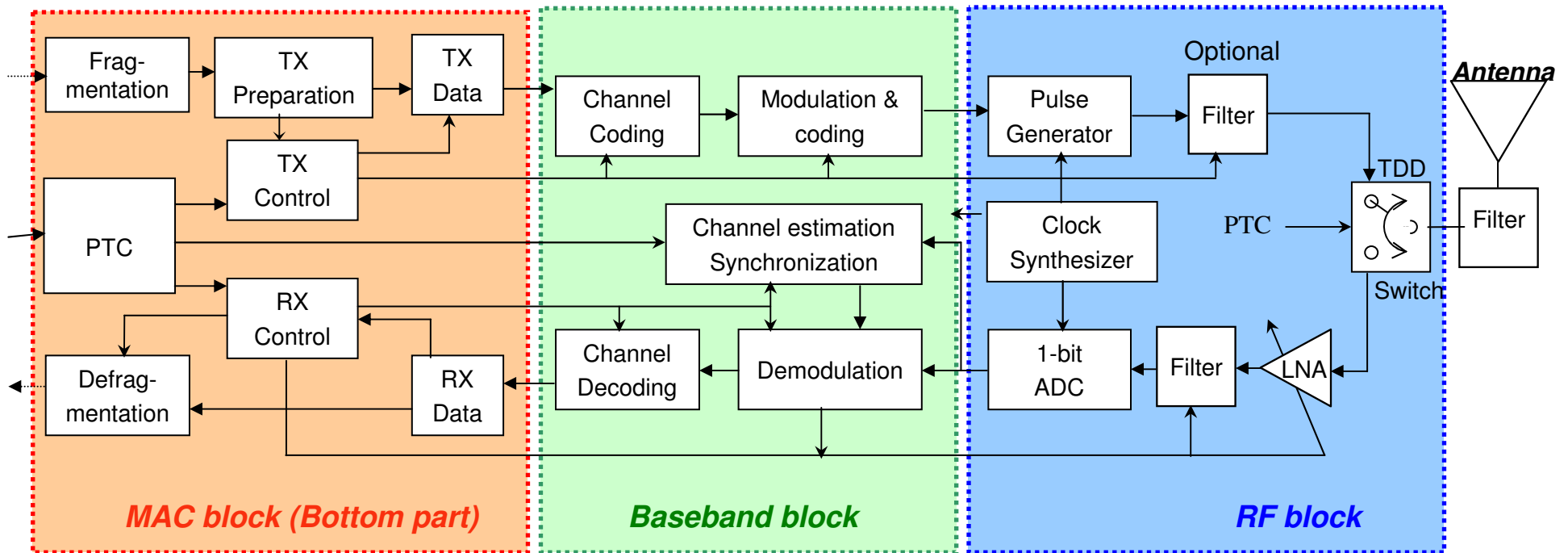
Polarity Modulation (BPSK)



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UWB System-On-Chip Block Diagram



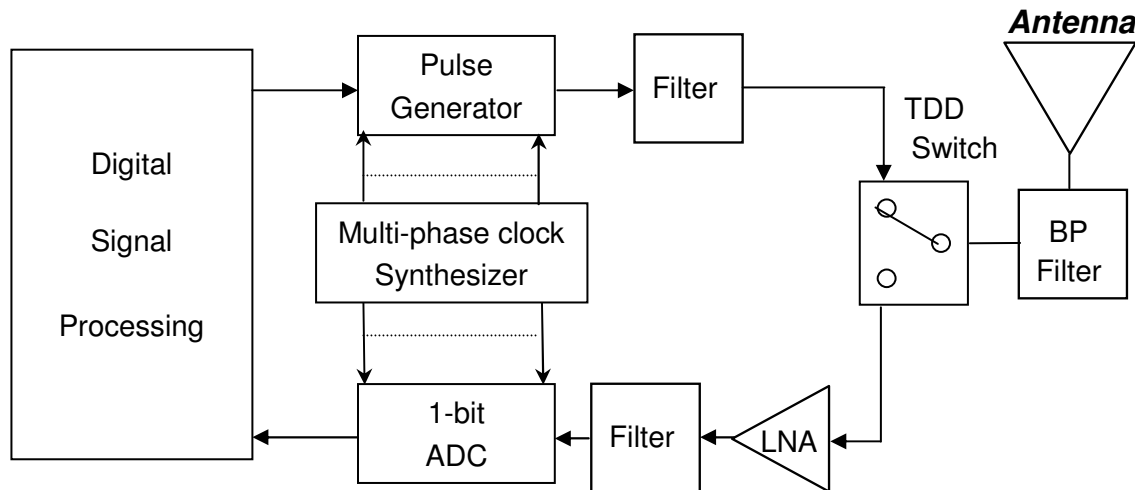
PTC = Piconet Time Control

UWB RF Architecture

Ideas:

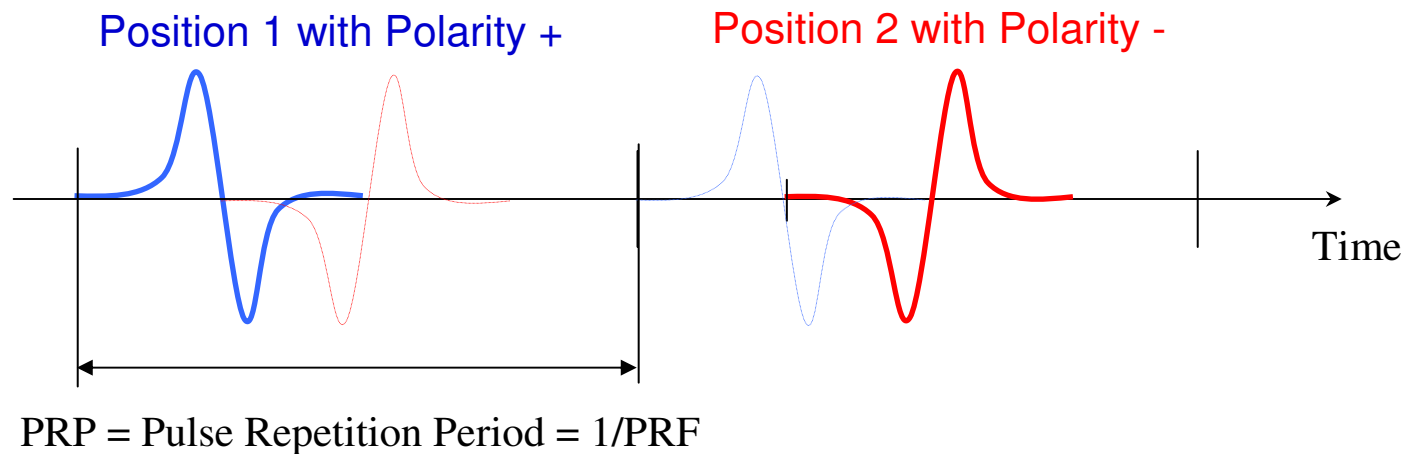
- Pulse modulation: Polarity and Position
- Direct sampling of the received signal
- Digital matched filtering – No pulse shape assumption
- Digital pulse generation

- **Digital Correlator**
- **20 GHz Sampling Rate**
- **1 bit output ADC**
- **Adaptable Template**
- **Multipath Rake Receiver**



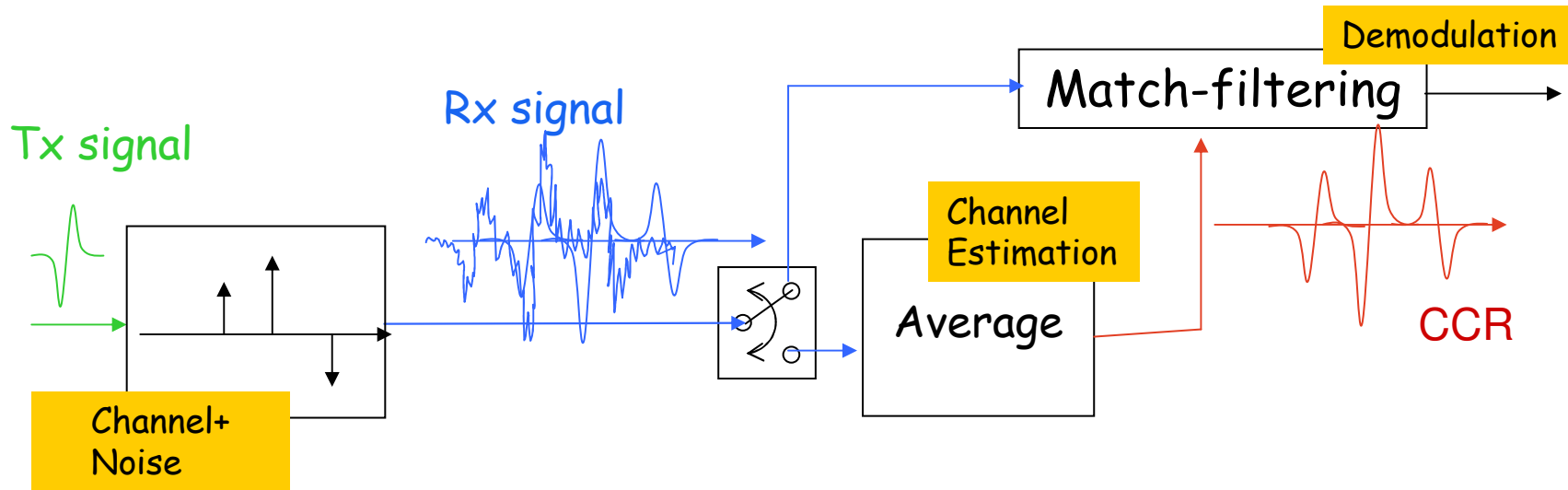
UWB Pulse Transmission

Information coding : Pulse Position Modulation (PPM) + Polarity (BPSK)



A system with a PRP of 5 ns ($PRF = 200$ MHz) using a 2-PPM + Polarity transmits 400 million bits per second

Demodulation: Digital Matched Filtering



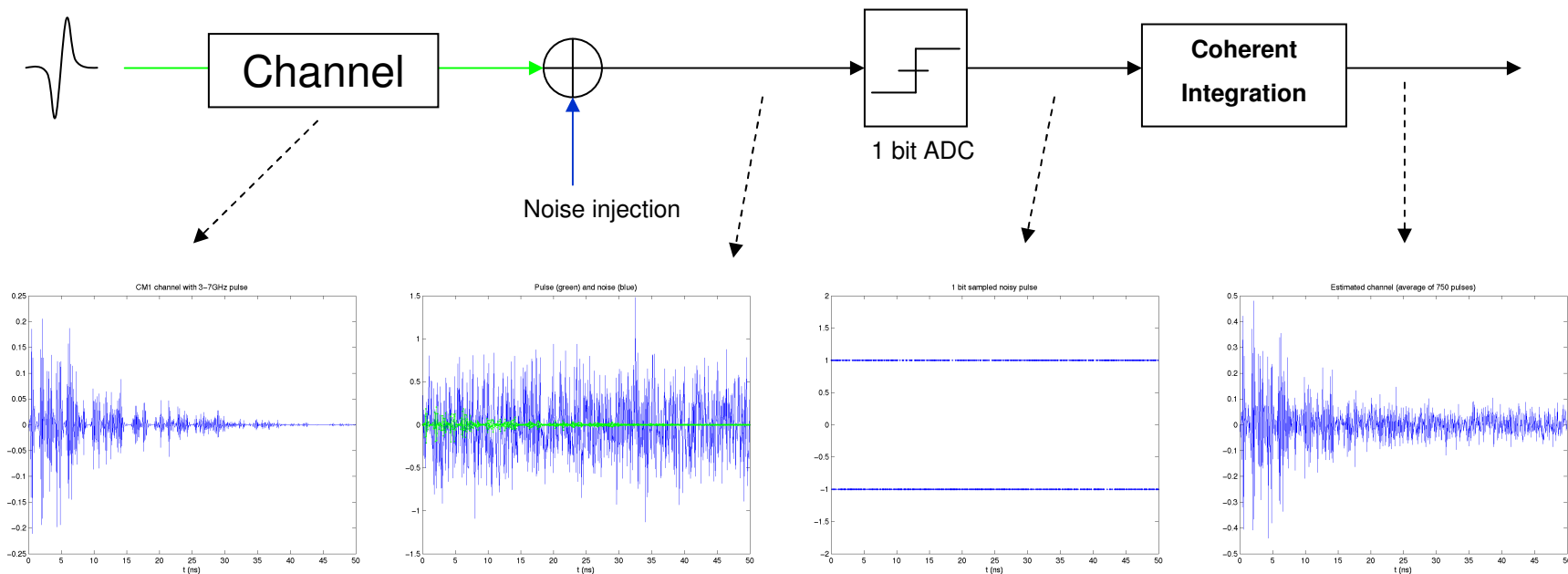
No TX pulse shape assumed (relaxes Analog Front End specs)
Takes advantage of multi-path (complete immunity)

Procedure

- 1 - TX sends known sequence of pulses (position/polarity)
- 2 - RX synchronizes to the sequence
- 3 - RX learns **Compound Channel Response (CCR)** to a TX pulse
- 4 - RX uses CCR as a matched filter to demodulate TX data

1-bit Channel Estimation

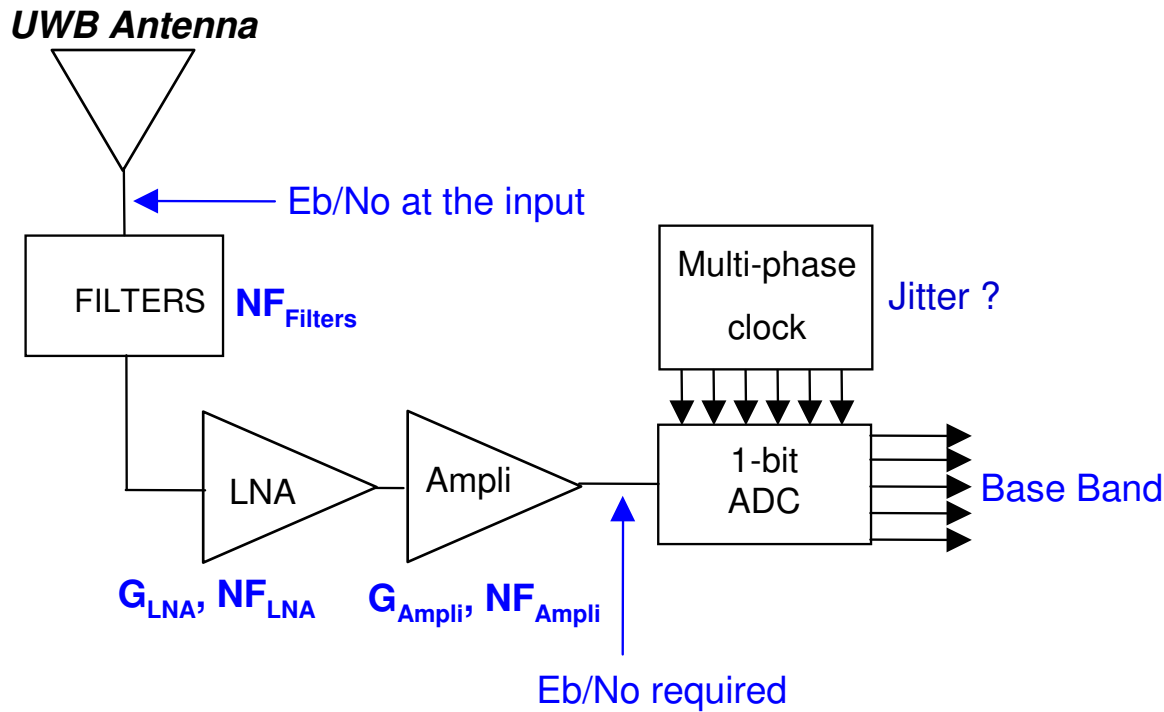
- 20 GHz 1-bit sampling
- Coherent integrations to estimate the CCR used for demodulation



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RF Rx Front-End Specifications

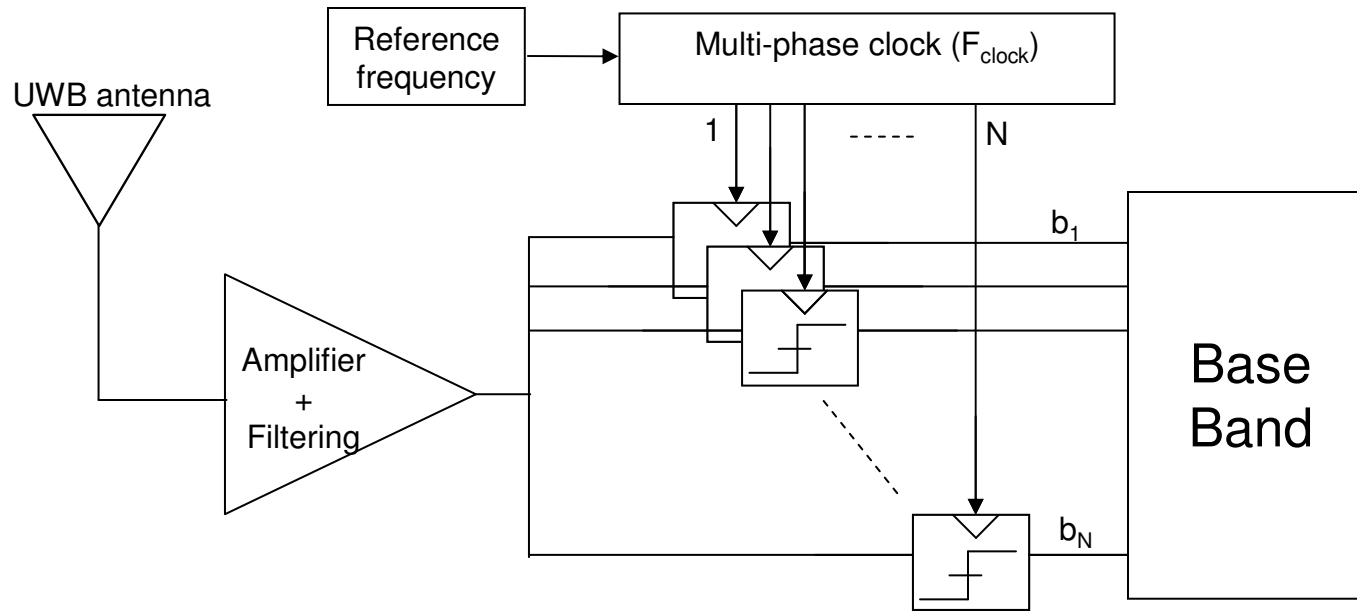


- **BW = 4 GHz, (3 to 7 GHz)**
- **NF_{Filters} < 3 dB (Insertion Loss)**
- **G_{LNA} > 12 dB, NF_{LNA} < 6 dB**
- **G_{Ampli} > 15 dB, NF_{Ampli} < 10 dB**

$$(NF_{RF})_{dB} \leq \left(\frac{E_b}{N_0} \right)_{in} - \left(\frac{E_b}{N_0} \right)_{required} \quad \text{– Implement. Loss - Link margin}$$

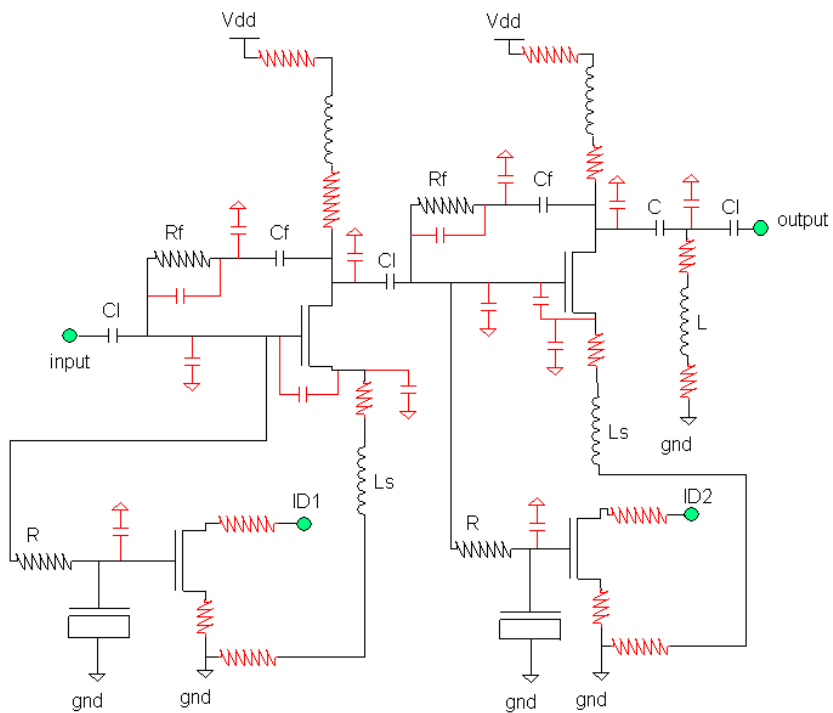
$$NF_{RF} < 10 \text{ dB}$$

1-bit Direct Sampling

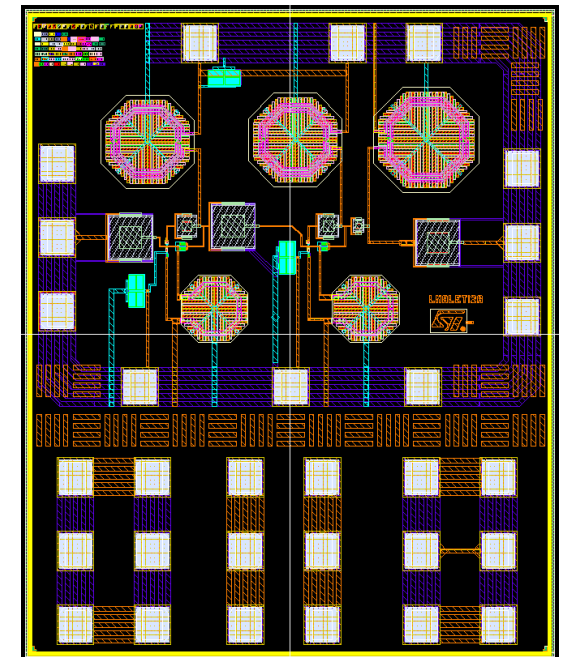


- Operating frequency = 614.4 MHz (32 x 19.2 MHz)
- N clocks of 614.4 MHz
- Sampling frequency = N x 614.4 MHz
- N = 32 => Sampling frequency = 19.7 GHz

UWB LNA Implementation HCMOS 0.13 μm



1.02 mm

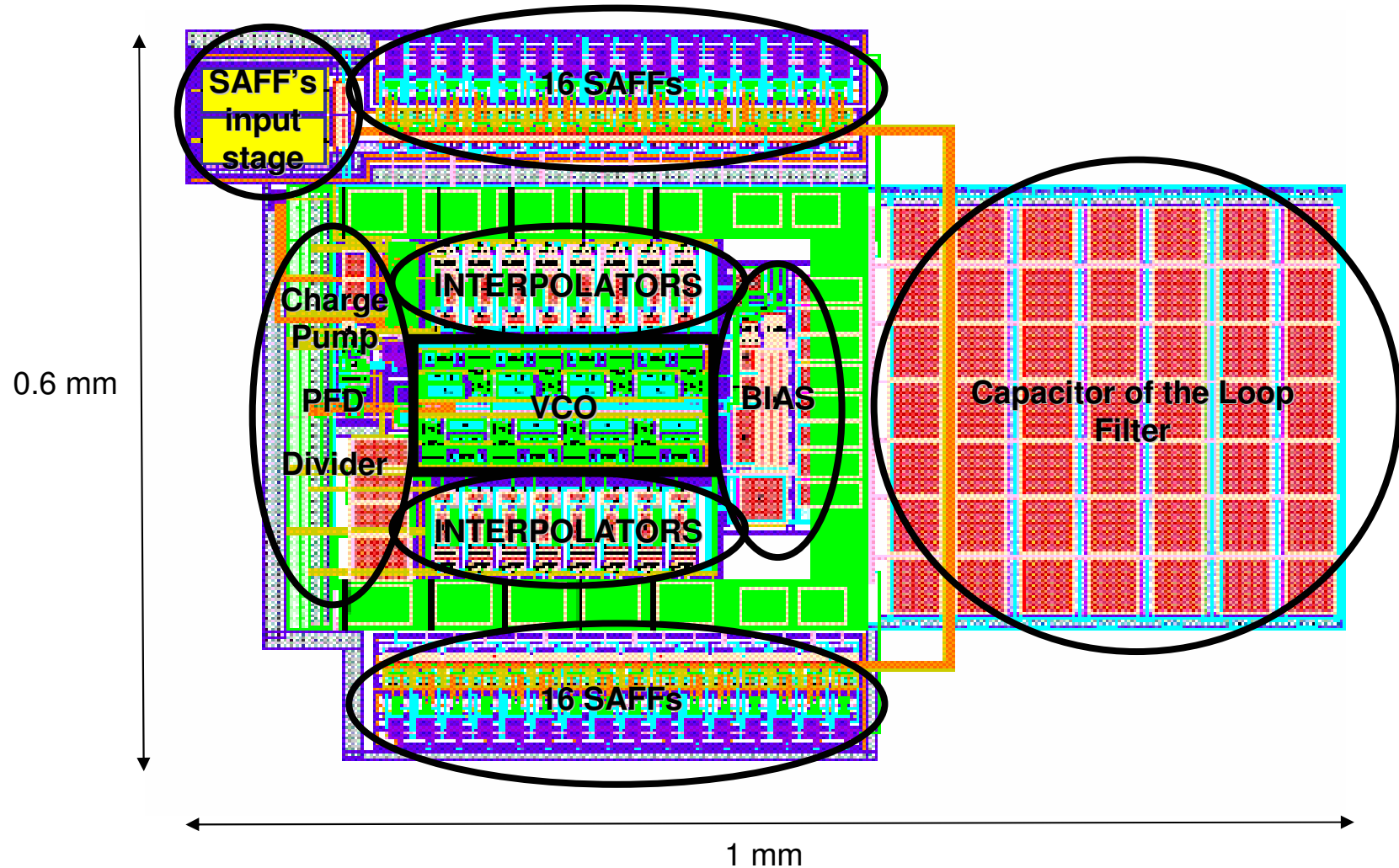


0.79 mm

UWB LNA Performances

| | Simulations | On wafer probing |
|------------------------------|------------------|------------------|
| Vdd | 1.2 V | 1.2 V |
| -3dB bandwidth | 2.8 GHz to 6 GHz | 2.8 GHz to 6 GHz |
| S(1,1) | ≤ -11.5 dB | ≤ -11.5 dB |
| S(2,2) | ≤ -15 dB | ≤ -12 dB |
| S(2,1) | ≤ 13.5 dB | ≤ 11.4 dB |
| S(1,2) | 2.1 dB | 2.1 dB |
| Gain ripple | 2.1 dB | 2.1 dB |
| Noise Figure | ≤ 3.8 dB | ≤ 5.54 dB |
| IIP3 | 4.5 dBm (4 GHz) | TBD |
| 1dB Compression Point | -7.6 dBm (4GHz) | TBD |
| Current Consumption | 32 mA | 32 mA |

Multiphase PLL + 1 bit ADC Lay-Out HCMOS 0.13 μm

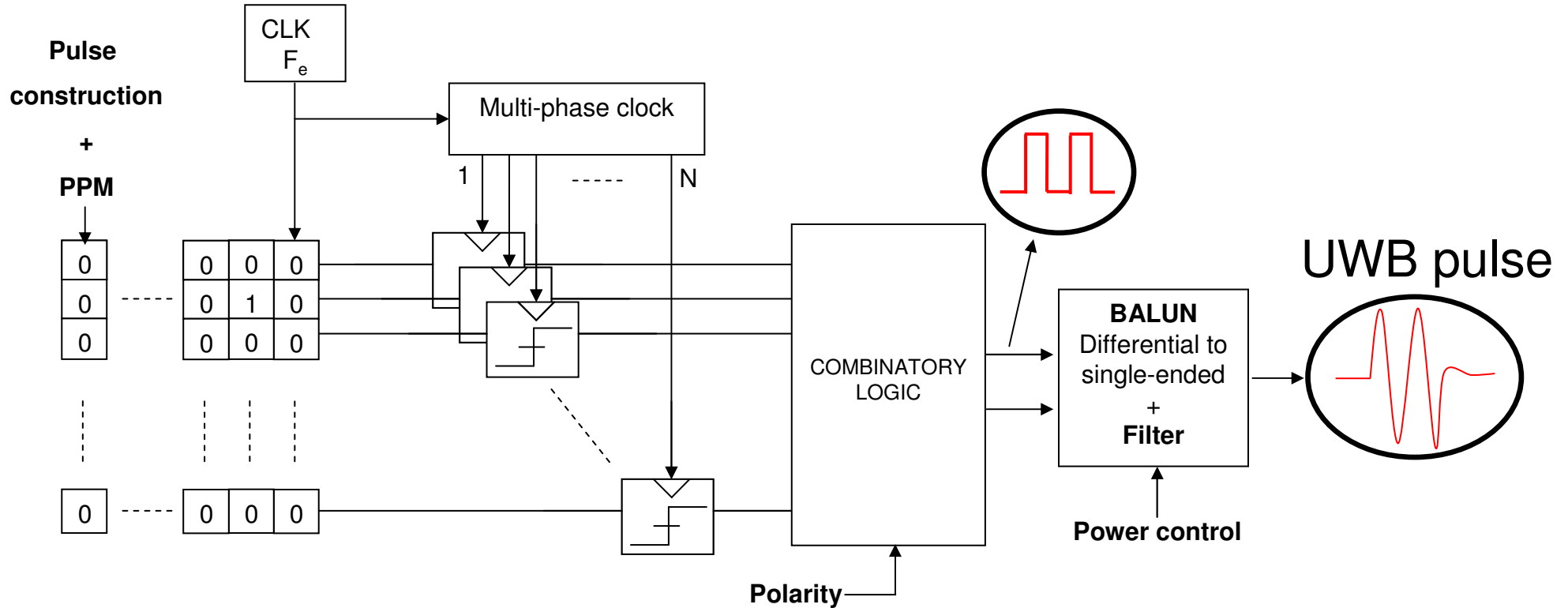


Presentation Outline

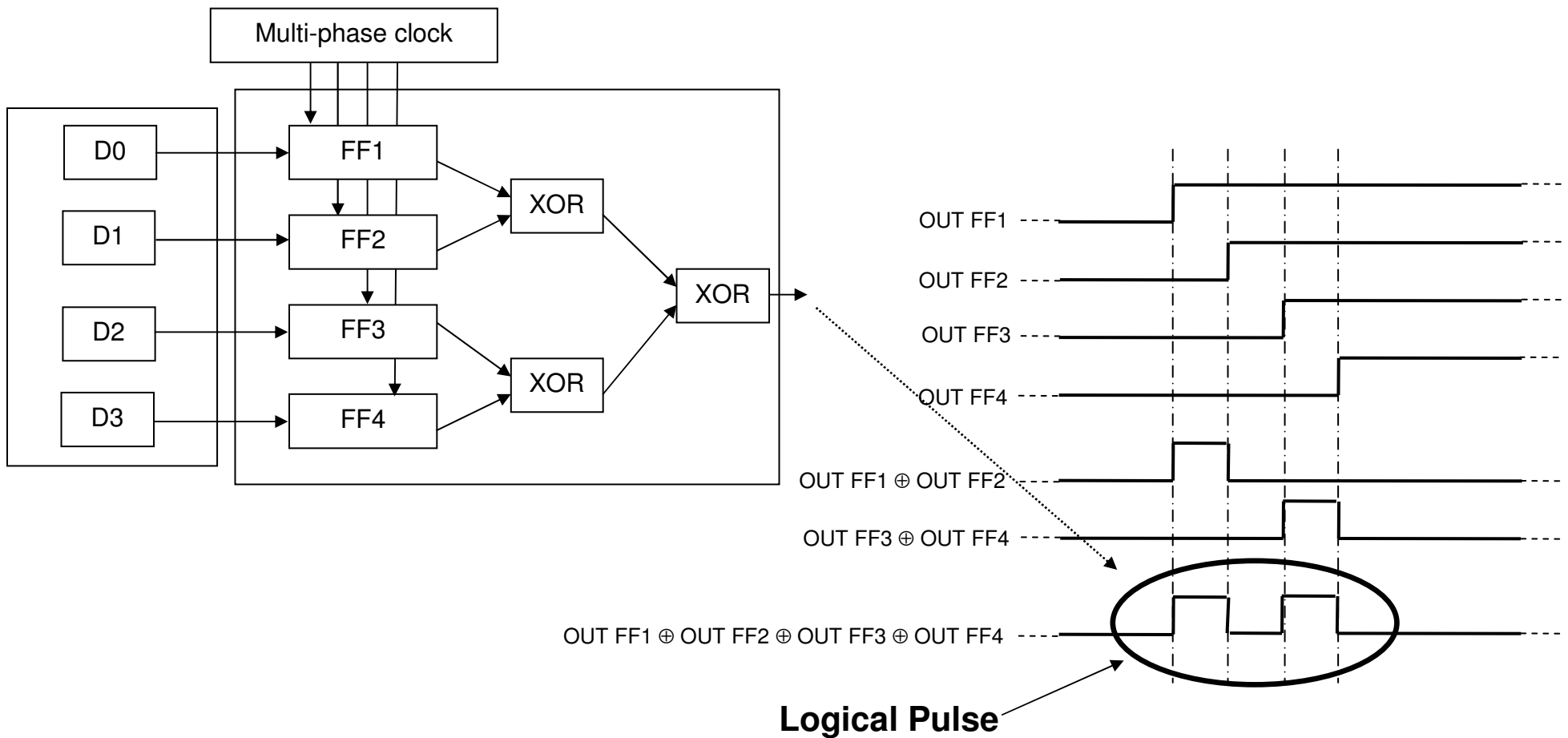
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UWB Pulse Generator Architecture

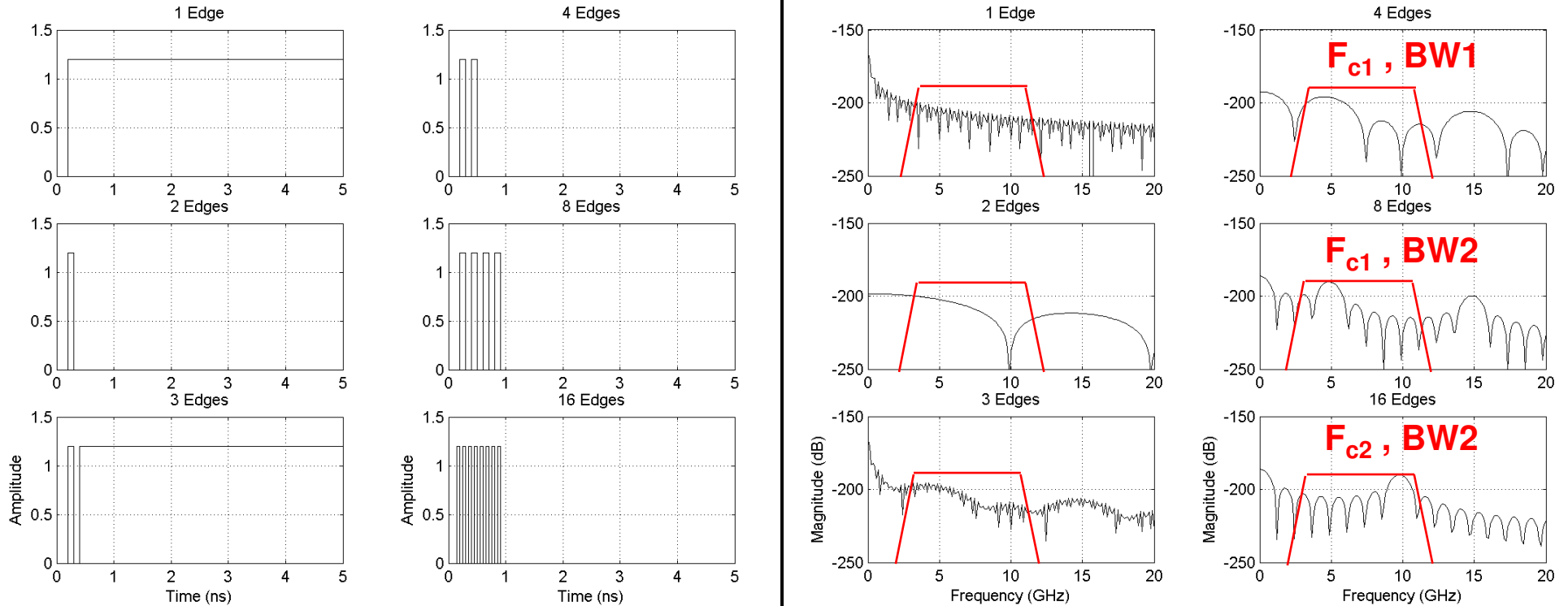
Idea: Use of the multi-phase clock with the addition of a logical circuitry and a Balun to simply generate UWB pulses with PPM and polarity modulations.



Example of Combinatory Logic Realization



Spectrum for Different Logical Combinations



- Possibility to control the center frequency and the bandwidth of the pulse -

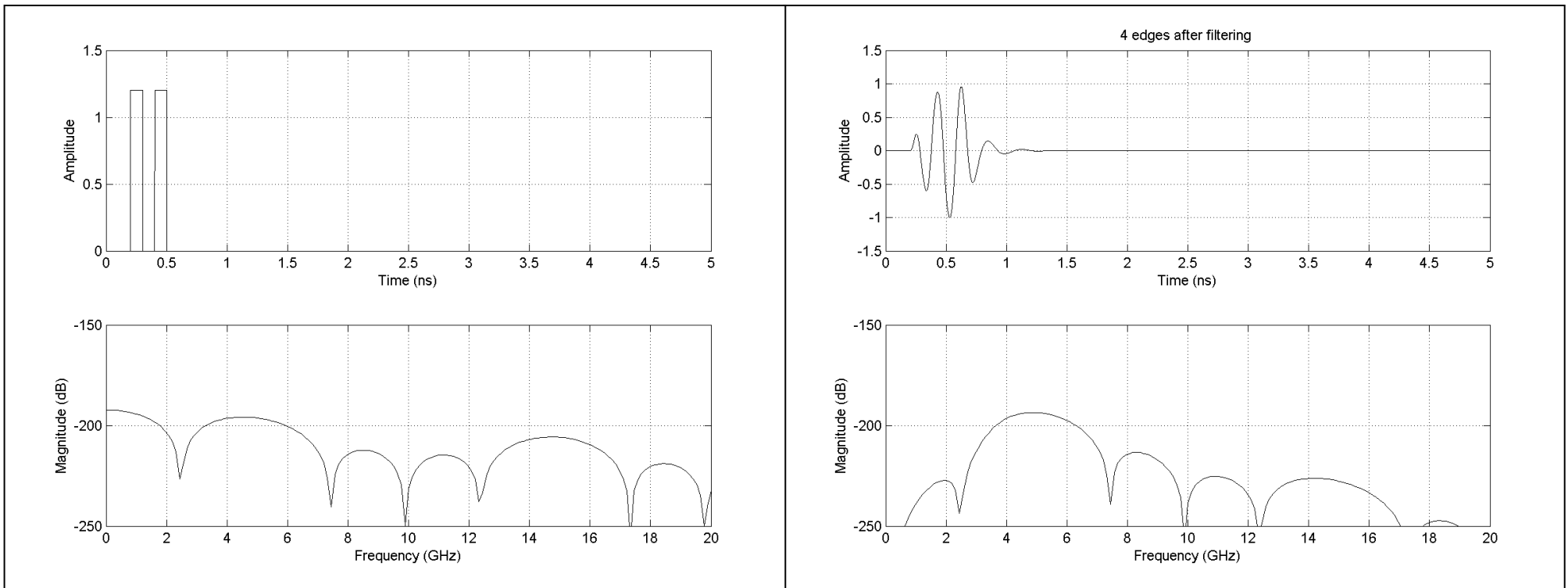
From Logical Combination to UWB Pulse

Before the balun

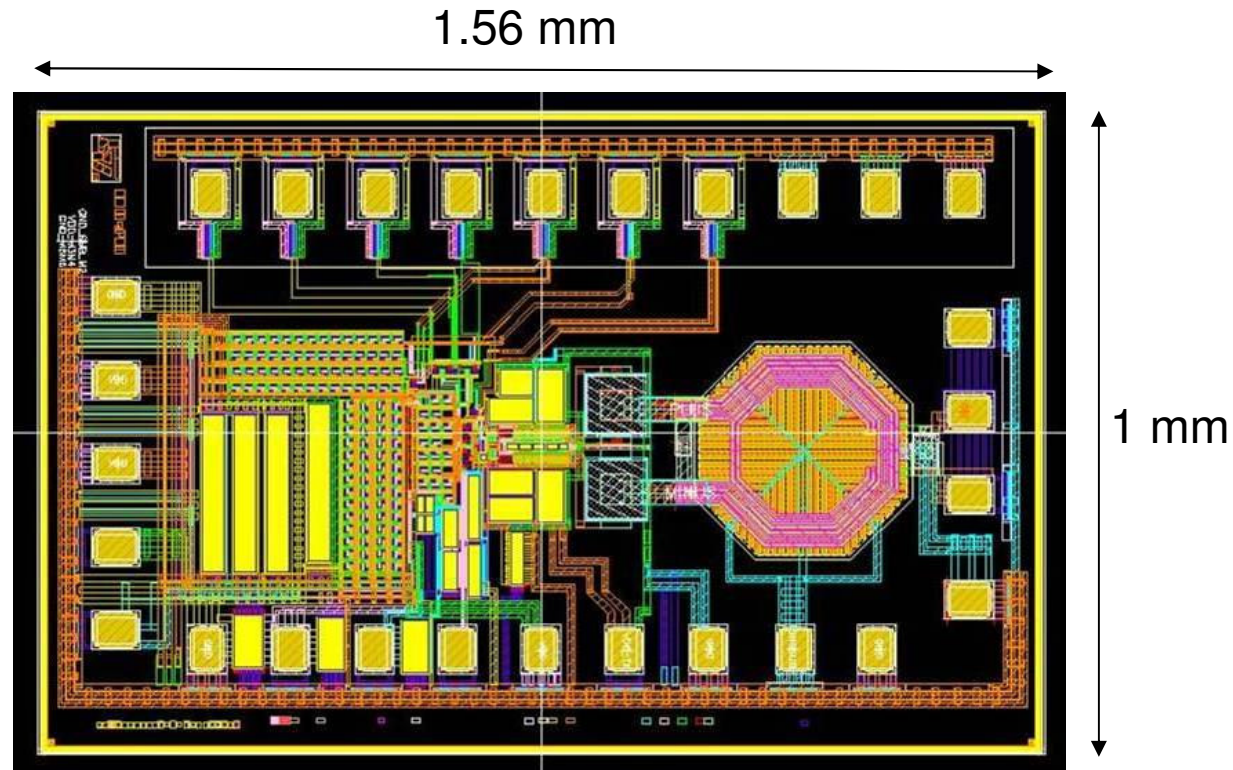
« Combinatory logic output »

After the balun and the filter

« Antenna input »



UWB Pulse Generator Lay-Out

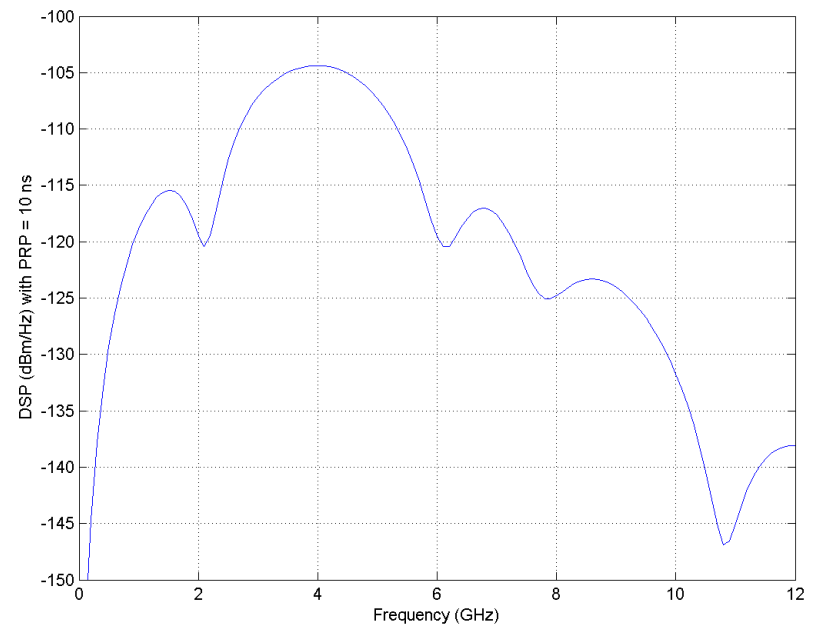
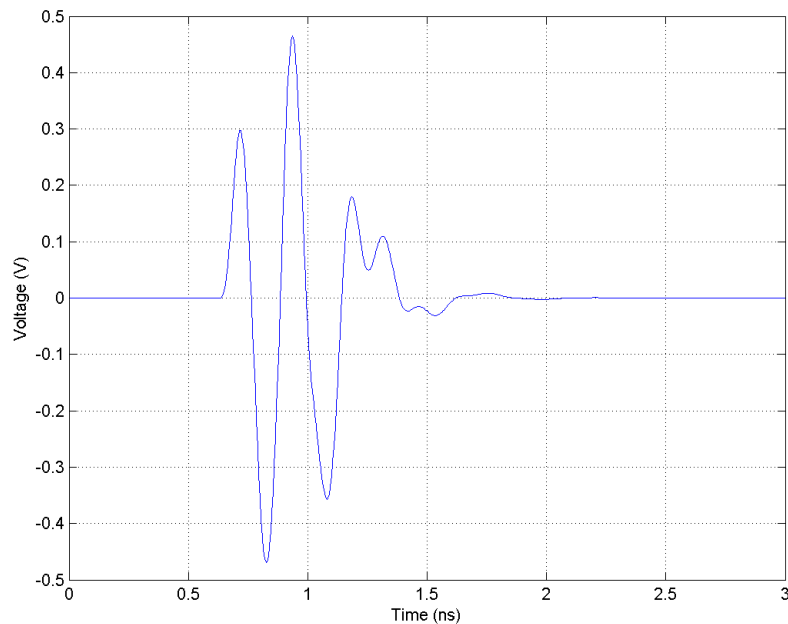


- Implementation in full HCMOS $0.13 \mu\text{m}$
- Power consumption: $< 50 \text{ mW}$ (Supply voltage = 1.2 V)

Pulse Generator

Post Lay-Out Simulation Results

- Bonding and parasitic capacitances have been taken into account

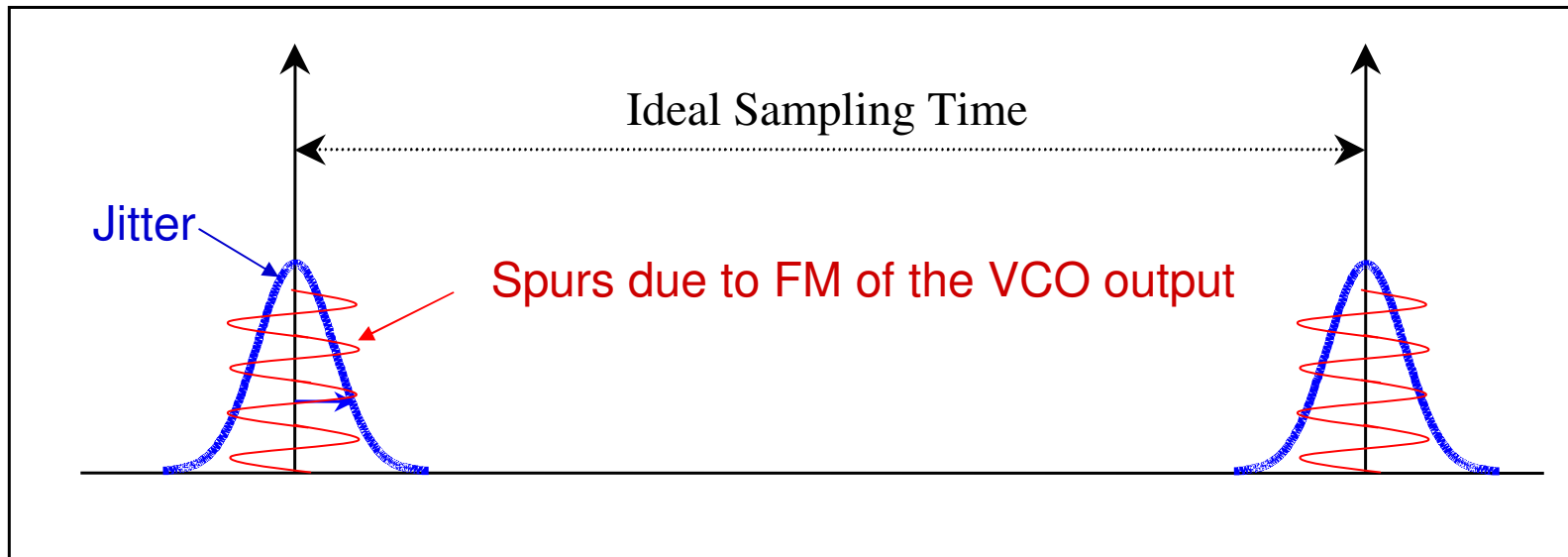


- Center frequency = 4 GHz
- -10dB bandwidth = 3.1 GHz (2.3 GHz to 5.7 GHz)

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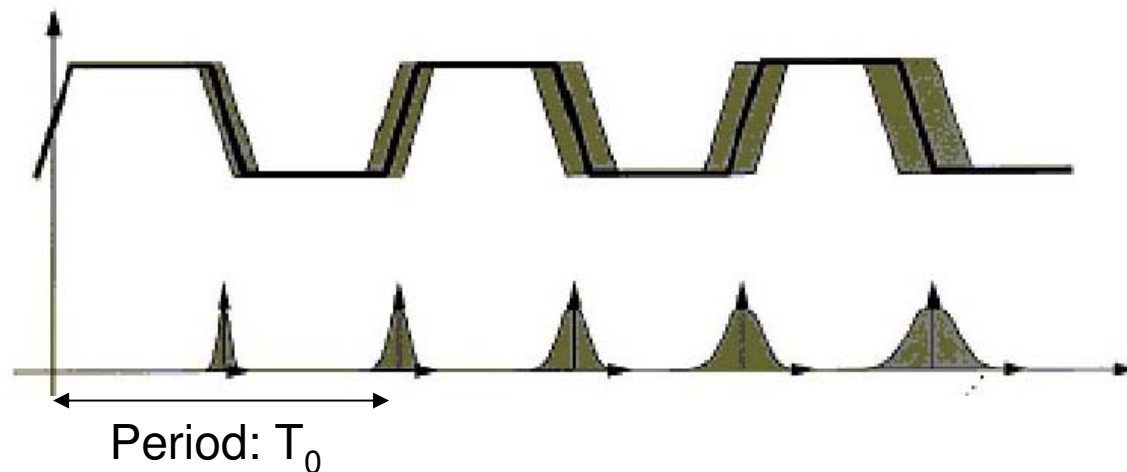
PLL Timing Accuracy



$$\text{Real sampling time} = \text{Ideal sampling time} + \underbrace{\text{jitter}(0, \sigma_{\text{abs}})}_{\text{Cumulative jitter}} + \underbrace{A \cdot \sin(\omega_{\text{spurs}} t)}_{\text{PLL spurs}}$$

Timing Jitter Definitions and Effect

- **Cycle Jitter** σ_c : Timing error in one clock period related to the phase noise
- **Absolute Jitter** σ_{abs} : Takes into account the cumulative nature of jitter



- **Effect of jitter:** The sampling time uncertainty increases with the time

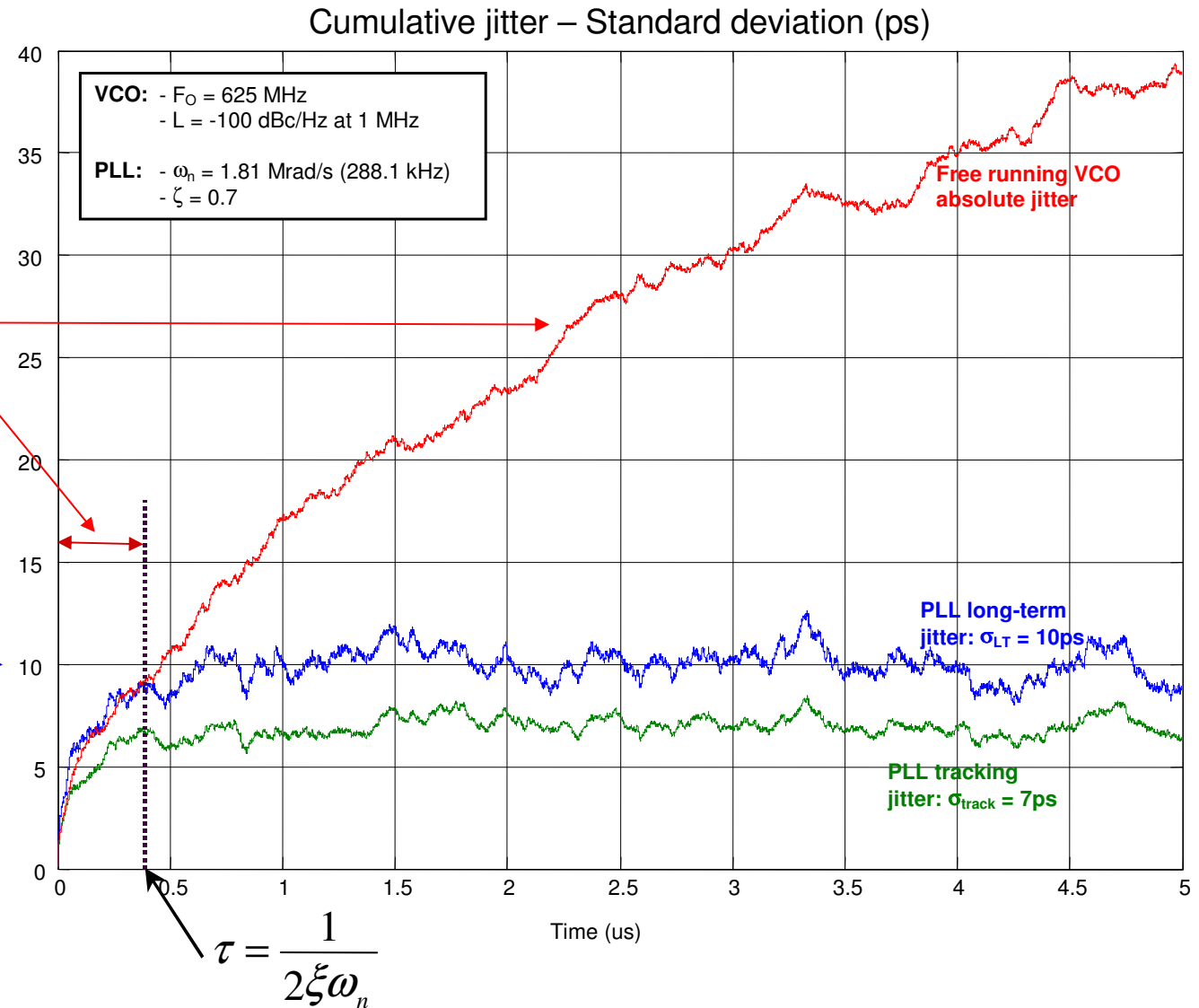
PLL Jitter Behaviour Simulations

σ_c : VCO cycle jitter

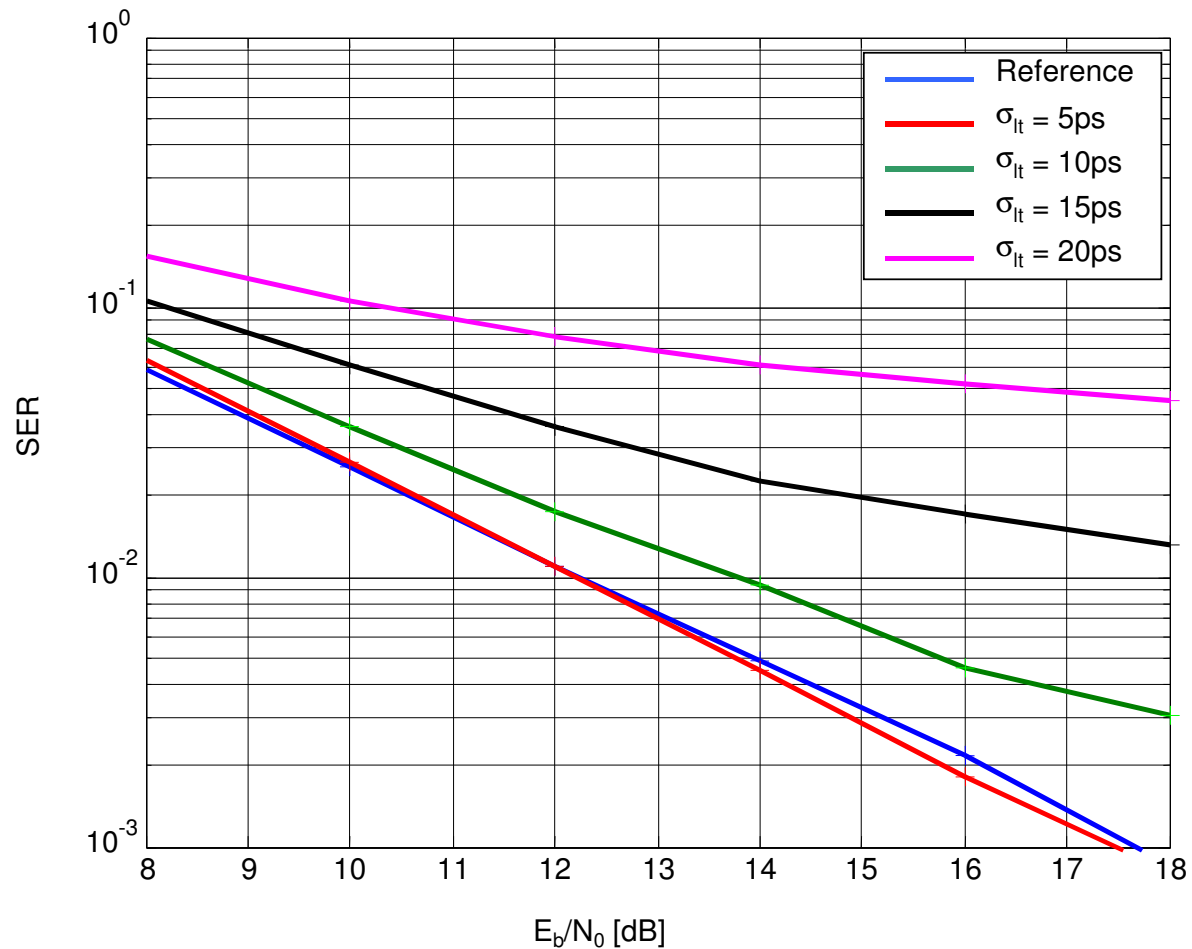
Deduced from phase noise

$$\sigma_{lt}^2 = \frac{\sigma_c^2}{T_0} t$$

$$\sigma_{lt}^2 = \frac{\sigma_c^2}{T_0} \cdot \frac{1}{2\xi\omega_n}$$

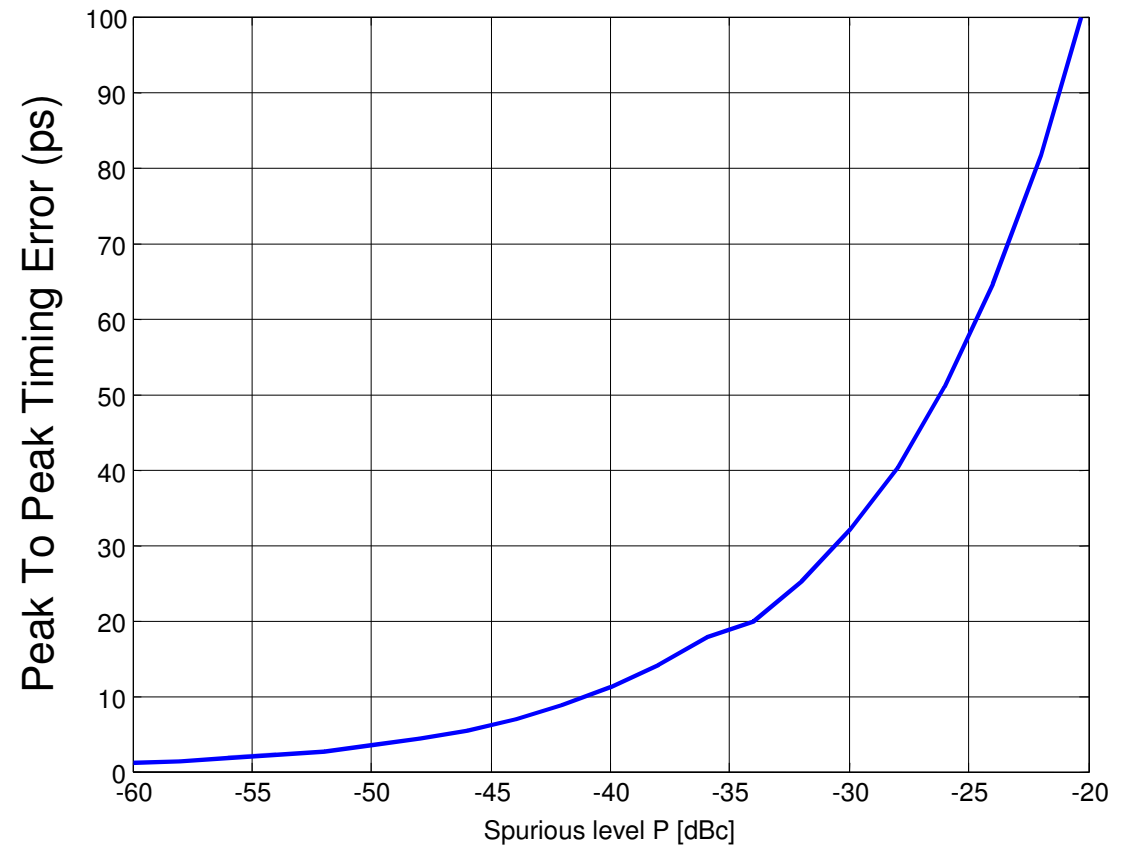
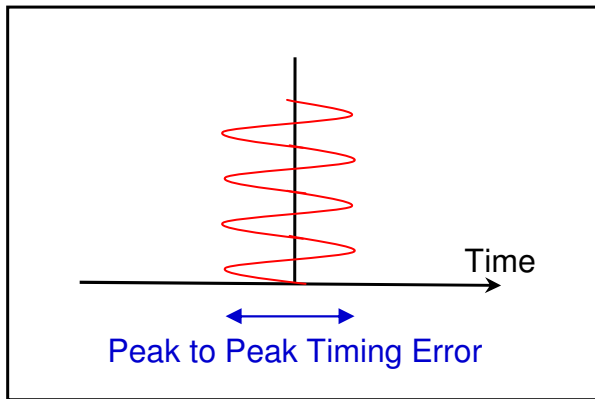


Effect of Jitter on Demodulation Performances

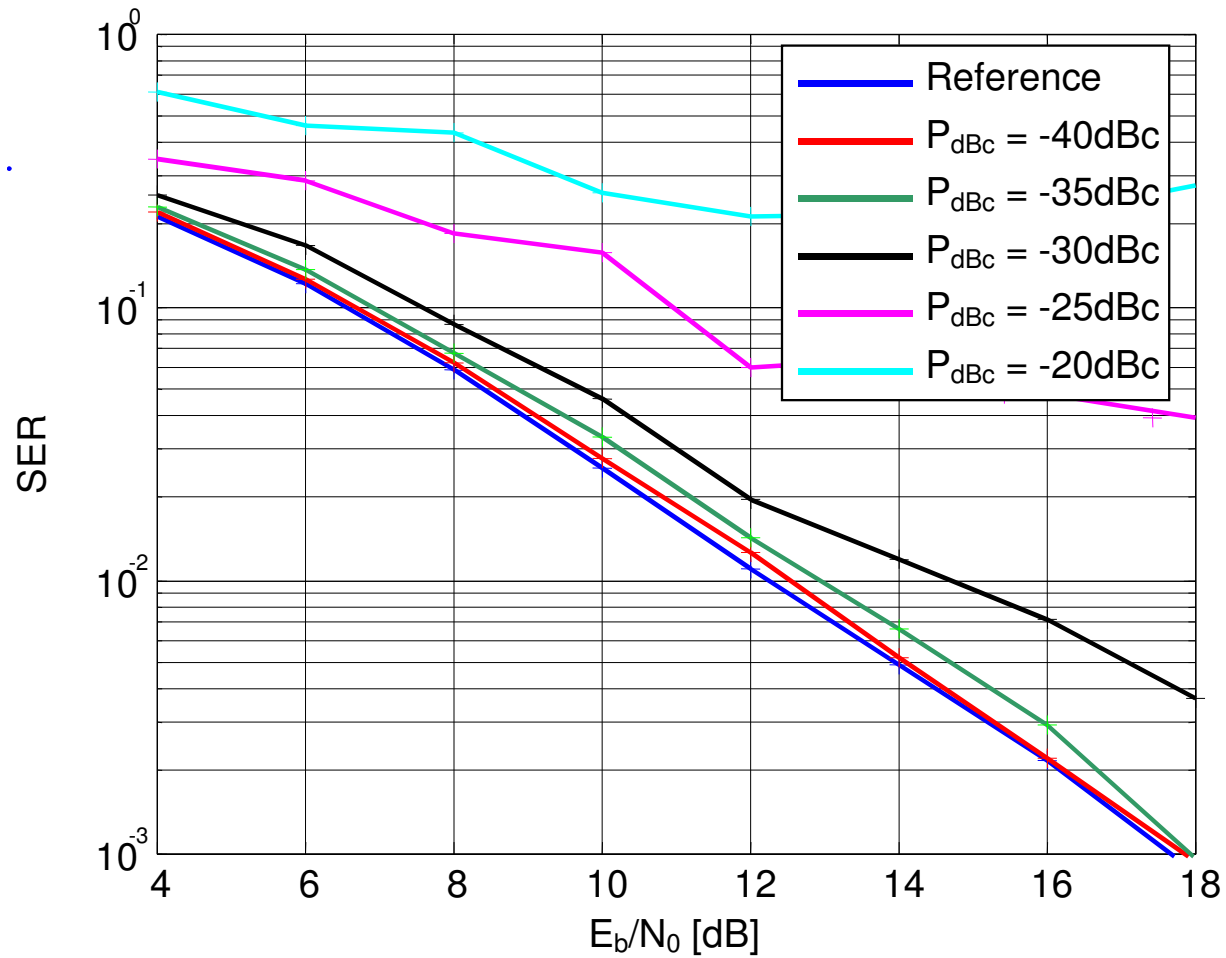


- Conclusion: $\sigma_{jt} < 10\text{ps}$ -

PLL Spurs Effect on Timing Accuracy



Effect of Spurs on Demodulation Performances



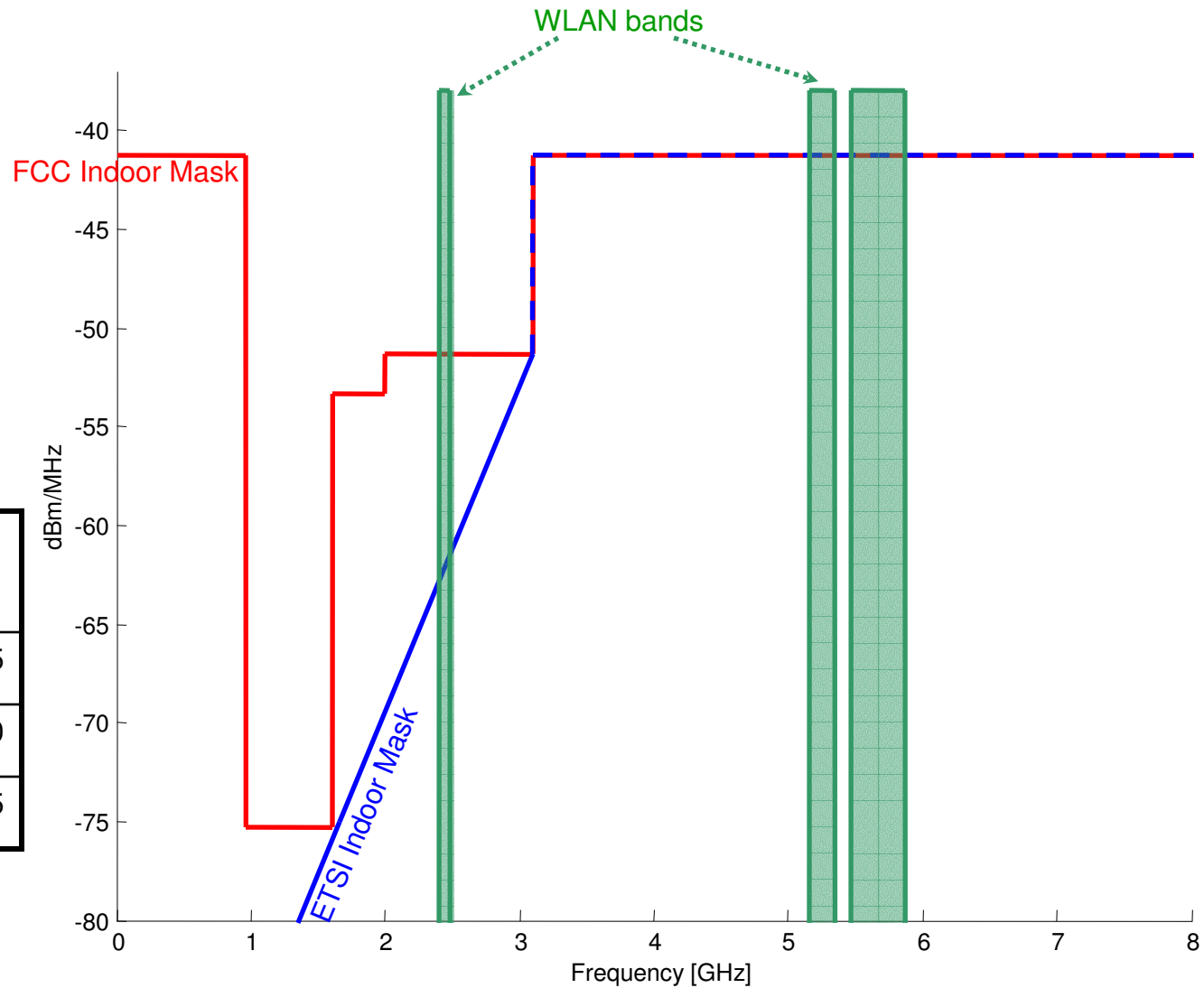
- Conclusion: $P_{dBc} < -35dBc$ -

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Coexistence with WLAN

| WLAN band # | Lower Frequency [MHz] | Upper Frequency [MHz] |
|-------------|-----------------------|-----------------------|
| 1 | 2400 | 2483.5 |
| 2 | 5150 | 5350 |
| 3 | 5725 | 5875 |

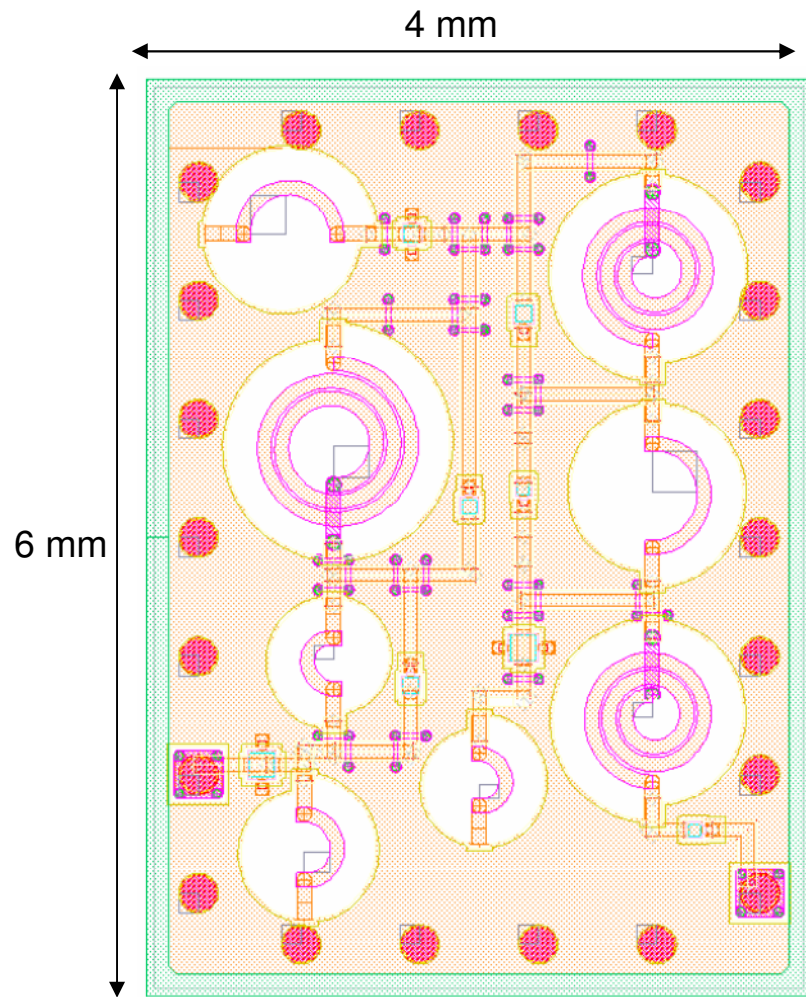


Possible Solutions to Avoid WLAN Bands

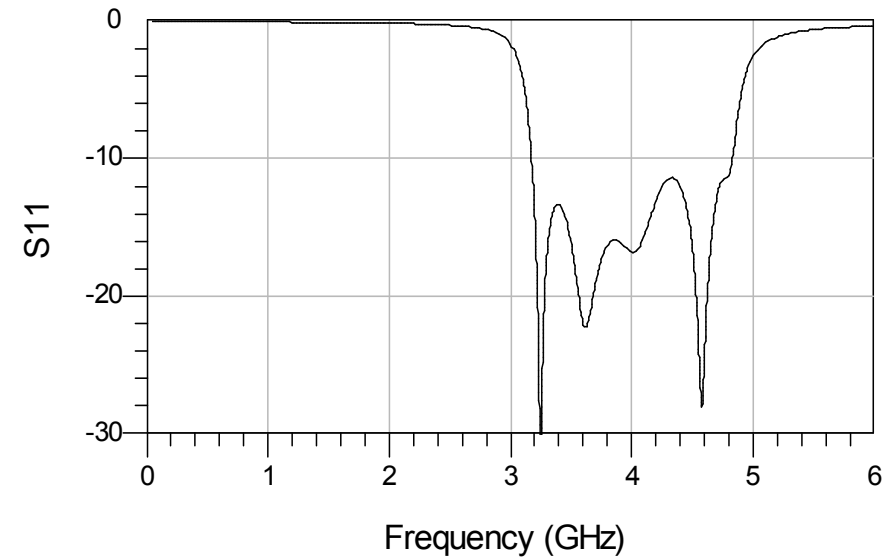
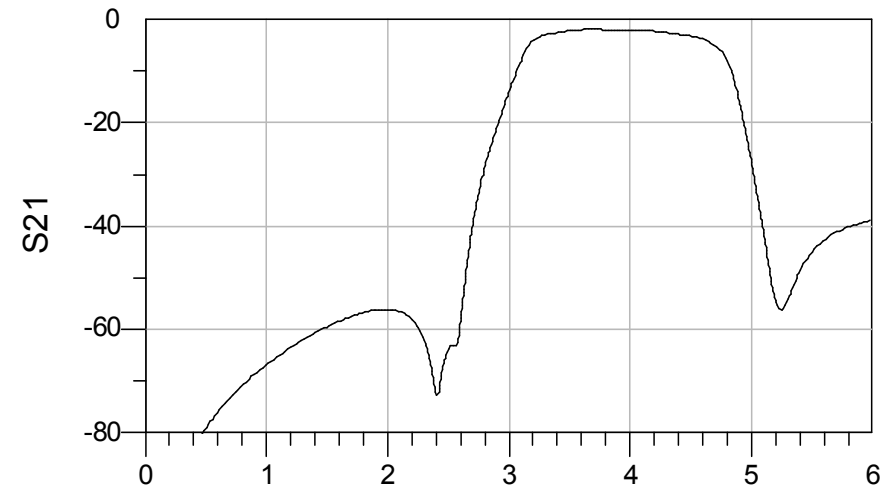
- **Avoid using concerned bandwidth**
 - UWB lower band: 3.1 to 5 GHz
 - UWB higher band: 6 to 10.6 GHz

- **Use of notch filters at Tx and RX**

UWB Band-Pass Filter Elliptic 6th Order



- STM IPAD technology -



STM UWB RF Transceiver Summary

**UWB single chip full HCMOS 0.13 μm solution
(except filters and antenna)**

with

Numerical UWB pulse generation

20 GHz 1-bit direct sampling

Digital matched filtering with no pulse shape assumption

(Learn pulse signature after channel propagation)

Acknowledgments

▣ CEA – LETI (Grenoble, France)

- UWB LNA design
- PLL/DLL + 1 bit ADC design
- PLL jitter study

▣ ISD (Athens, Greece)

- PLL + 1 bit ADC design

▣ STM - Discrete Standard Circuit & RF Group (Tours, France)

- UWB band-pass filter design

▣ STM - Central R&D (Crolles, France)

- UWB pulse generator design