



ABSTRACTS OF THE TALKS

**Workshop on Multi-Mode Multi-Band  
Reconfigurable Systems for  
3<sup>rd</sup> Enhanced Generation Mobile Phones**

Leuven, Belgium

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**Introduction:**

This workshop is organized by the Electronics Laboratories (LEG) of the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in the frame of the IST European project MuMoR on 3rd enhanced generation mobile phones (Project number: IST-2001-34561; Title: Multi-mode radio architecture platform for enhanced 3G; web page: [www.mumor.org](http://www.mumor.org))

The aim of this one day workshop is to present the main results of the project MuMoR to the international scientific community. The main objective of this project is to design multi-mode multi-band RF wireless systems dedicated to 3rd enhanced generation mobile phones. The targeted modes of operation are: GSM, HSDPA, and UMTS FDD and TDD.

**Workshop objective:**

This workshop aims to bring together researchers, developers and potential users concerned with advanced low-power design solutions applicable to the design of RF, analog, digital or mixed-signal front-ends dedicated to enhanced 3rd generation mobile phones. It tries to reflect European activities with state-of-the-art / innovative aspects in the RF field. The talks are given by international speakers from industry and the academic world.

Low-power design of microelectronic circuits is becoming increasingly important as chips become larger, more complex and faster, and as a consequence of the drive towards portable high-performance products for wireless communications. The design effort for the analog parts and front-ends of these products is high, especially when the power consumption needs to be kept minimal. Low-power design and reconfigurability of the analog and digital parts have to be addressed both at the architectural level and at the circuit level.

**Date:** September 24, 2004

**Place:** Leuven, Belgium

**E-MAILS OF THE SPEAKERS  
(by order of talk)**

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## PROGRAM

### From 8.30 a.m. to 8.45 a.m. Workshop registration

### At 8.45 a.m. Multi-Mode Radio Architecture Platform for Enhanced 3G

- Catherine Dehollain (EPFL, Electronics Laboratory, Lausanne, Switzerland)

### At 9.00 a.m. Session 1: RF front end architecture for wireless mobile terminals

- Horst Fischer (IMST, Kamp-Lintfort, Germany)  
*IST European project MuMoR - Component specifications for a re-configurable multi-mode receiver*
- Michael Engels (IMST, Kamp-Lintfort, Germany)  
*IST European project MuMoR - A novel architecture for GSM/UMTS multi-mode transmitters*
- Lydi Smaini (STMicroelectronics, Geneva, Switzerland)  
*RF digital transceiver for Impulse Ultra Wide Band communications*

### From 10.45 a.m. to 11.10 a.m: Coffee break

### At 11.10 a.m. Session 2: Analog to Digital Converters for Telecom Applications

- Franco Maloberti (University of Texas, Dallas, Texas, USA)  
*ADC for telecom applications*
- Vasileios Sinnis, Theodoros Nikolaidis (ISD SA, Athens, Greece)  
*IST European project MuMoR - Reconfigurable pipeline Analog/Digital Converter for WCDMA/GSM operation*

### From 12.25 to 1.50 p.m. : Lunch

### At 1.50 p.m Session 3: Frequency synthesizers for enhanced 3G mobile phones

- Roberta Cambio (University of Aberdeen, United Kingdom)  
*IST European project MuMoR – An Agile Multi-Mode frequency synthesizer*
- Emmanuel Chataigner (STMicroelectronics, Crolles, France)  
*IST European project MuMoR - A reconfigurable 4-GHz VCO for 3G multimode transceivers*
- Franck Badets (STMicroelectronics, Crolles, France)  
*IST European project MuMoR - Design of a 800 MHz frequency synthesizer for a 4GHz Synchronous Oscillator based frequency synthesizer*
- Markus Mueller, Stephan Boecker, Ralf Kakerow (Nokia, Bochum, Germany)  
*IST European project MuMoR – New approach for frequency synthesizers in multi-mode radio applications*

### From 3.35 p.m. to 4.00 p.m: Coffee break

### At 4.00 p.m Session 4: General aspects for mobile communications

- Nicolas Schlumpf (EPFL, Electronics Laboratories, Lausanne, Switzerland)  
*IST European project MuMoR – A fast modulator for dynamic supply linear RF power amplifier*
- Marc Laugeois (CEA, LETI, Grenoble, France)  
*IST European project MuMoR - Reconfigurability approach on hardware Design for UMTS terminal*

### At 5.00 pm: Closing of the workshop

## Opening of the workshop (8.45 a.m.)

### **Catherine Dehollain (EPFL, Electronics Laboratory, Lausanne, Switzerland)**

#### *Multi-Mode Radio Architecture Platform for Enhanced 3G*

The aims of the IST European MUMOR project (Multi-Mode Architecture Platform for Enhanced 3G) are :

- To investigate the impact of the mobile terminal performance on the communication network infrastructure.
- Today's standards as well as future extension of UMTS towards higher data rates (up to 10MBit/s) and their influence on the mobile terminal architecture and components are considered.
- RF front-end as well as base-band is investigated in order to find a common re-configurable architecture which is flexible to adapt to different standards.

Within MUMOR, a promising system architecture for the RF front-end and the base-band is defined. Based on the specifications from different communication standards, the required performance for the main function blocks has been derived. Critical function blocks have been evaluated taking into account advanced semiconductor technologies. Promising technologies like SiGe-BiCMOS have been considered for development of IPRs.

Talk duration: 15 minutes (including questions and answers).

## Session 1: RF front-end architecture for wireless mobile terminals

### **Horst Fischer (IMST, Kamp-Lintfort, Germany)**

#### *IST European project MuMoR - Component specifications for a re-configurable multi-mode receiver*

From the technical specifications for the different mobile phone standards RF relevant parameters like SNR, NF, IIP3, etc are derived. These parameters define the whole receiver from antenna to digital baseband. The specification and choice of external components sets the boundary conditions for the transceiver chip. The influence of particular components on the overall RF-performance will be shown. These components are specified to meet the required RF performance. After the boundary conditions for the transceiver chip are defined by external components, the RF-parameters of the chip are broken down to building block level.

Talk duration: 25 minutes (plus 5 additional minutes for questions and answers).

### **Michael Engels (IMST, Kamp-Lintfort, Germany)**

#### *IST European project MuMoR - A novel architecture for GSM/UMTS multi-mode transmitters*

A novel architecture for multi-mode RF transmitter front-ends is presented. In the first mode the proposed architecture is capable of transmitting constant envelope signals like GSM with the required very low phase noise; in the second mode, the transmitter can generate non-constant envelope signals like UMTS. Compared to commonly used architectures for multi-mode transmitters, the required performance specifications of the components are significantly reduces, leading to advantages in current consumption and cost.

Talk duration: 20 minutes (plus 5 additional minutes for questions and answers).

### **Lydi Smaini (STMicroelectronics, Geneva, Switzerland)**

#### *RF digital transceiver for Impulse Ultra Wide Band communications*

This talk will present a promising UWB transceiver architecture functioning in the allowed FCC spectrum mask (between 3.1 and 5 GHz). Circuits as well as simulated results will also be described. The transceiver features a novel numerical pulse-shaping generator for the transmitter part (TX), and an efficient receiver based on a one-bit high-speed sampler on the receiver side (RX). This all-CMOS PHY implementation follows the single pulse philosophy (as opposed to the OFDM/multiband approach), applying pulse position modulation (PPM) combined with polarity modulation. The pulse generator is capable of shaping the pulse so that it occupies the desired spectrum, by piloting its center frequency and bandwidth (e.g. in order to follow the regional regulation constraints). The RX part is characterized by a 20 GHz one-bit ADC, based on a 625 MHz Phase-Locked Loop (PLL), which is also used for the pulse generation. 3dB are lost in the process, compared to infinite sampling, but it makes the baseband post-processing more manageable. The demodulation is independent from the transmitted pulse shape, making the transceiver very flexible.

Talk duration: 45 minutes (plus 5 additional minutes for questions and answers).

**10.45 a.m. to 11.10 a.m: Coffee Break**

## Session 2: Analog to Digital Converters for Telecom Applications

**Franco Maloberti (University of Texas, Dallas, Texas, USA)**

*ADC for telecom applications*

The talk addresses the use of sigma-delta and Nyquist-rate ADC for telecom applications. Sigma-delta converters have been conventionally used for low-bandwidth and high resolution. Recent results show that complex structures can achieve relatively high resolution while using low oversampling ratios. Therefore, extending the signal bandwidth to the MHz bandwidth range enable using sigma-delta techniques for an increasing number of communication applications. A sigma-delta 2MHz band capable to satisfy the W-CDMA specs consuming around 2 mW and a sigma-delta 5 MHz band-pass ADC with 80 MHz IF and 80 dB SNR are described. Pipeline architectures have been widely used for high-speed and high resolution. Now the focus is on low power for portable devices. Specific examples are given and the trend on the design of low power pipelines is addressed.

Talk duration: 45 minutes (plus 5 additional minutes for questions and answers).

**Vasileios Sinnis, Theodoros Nikolaidis (ISD SA, Athens, Greece)**

*IST European project MuMoR - Reconfigurable pipeline Analog/Digital Converter for WCDMA/GSM operation*

This work concerns the design of a 10bit/8bit 15.36/2.16MHz reconfigurable pipeline ADC for WCDMA/GSM operation. The pipeline ADC consists of 9 stages with 1.5bit per stage resolution. Redundancy in the number of bits resolved by each stage has been added, in order to cancel comparator offsets through efficient digital error correction blocks. Power minimization has been achieved by scaling the value of the sampling capacitances along the pipeline chain. The complete design has been performed with the CMOS option (0.25 $\mu$ m) of the BiCMOS7 library of ST Microelectronics. Extensive schematic and layout extracted level simulations revealed that the 10bit 15.36MHz pipeline ADC for WCDMA operation achieves +/-0.4LSB DNL, +/-1LSB INL, 8.9ENOB at the Nyquist frequency and total current consumption less than 5.5mA with 2.5V power supply.

Talk duration: 20 minutes (plus 5 additional minutes for questions and answers).

**From 12.25 to 1.50 p.m: Lunch**

## Session 3: Frequency synthesizers for enhanced 3G mobile phones

**Roberta Cambio (University of Aberdeen, United Kingdom)**

*IST European project MuMoR - An Agile Multi-Mode frequency synthesizer*

At this workshop we introduce the design of a hybrid wide-band re-configurable frequency synthesizer which has been developed at the University of Aberdeen. The novelty of this design is that the ratio between the frequency of the input signal and the frequency of the feedback signal is kept constant at lock. Simulation results are presented for VHDL and Verilog-AMS models, the latter for a VCO output frequency of around 4.5 GHz. Results for an interim 5 MHz hardware implementation are presented. This interim hardware implementation allows a more detailed analysis of the spurious signals generated at the DAC output, and the introduction of special filters to suppress the same. Currently we are testing in collaboration with IMST at their laboratories in Germany an RF board implementing the complete UMTS TDD synthesizer, which includes a VCO developed by ST Microelectronics and a divide-by-64 frequency divider.

Talk duration: 25 minutes (plus 5 additional minutes for questions and answers).

**Emmanuel Chataigner (STMicroelectronics, Crolles, France)**

*IST European project MuMoR - A reconfigurable 4-GHz VCO for 3G multimode transceivers*

A fully integrated 4-GHz voltage-controlled-oscillator (VCO) has been realized in a state-of-the-art BiCMOS process. Its differential Colpitts architecture offers very good phase noise for moderate power consumption. Aimed at 3G multimode transceivers it can be digitally configured for low phase noise or for low consumption thanks to an automatic amplitude control (AAC) loop. With a 2.7-V supply, it achieves a phase noise of -124 dBc/Hz @ 1-MHz offset at a tail current of 7 mA.

Talk duration: 20 minutes (plus 5 additional minutes for questions and answers).

**Franck Badets (STMicroelectronics, Crolles, France)**

*IST European project MuMoR - Design of a 800 MHz frequency synthesizer for a 4GHz*

*Synchronous Oscillator based frequency synthesizer*

A new architecture of RF frequency synthesizer has been proposed using an injection locked oscillator as a multiply by 5 frequency multiplier (Synchronous Oscillator, SO). After a brief description of the overall SO based frequency synthesizer architecture and of the SO, the presentation focuses on the design of the 800 MHz frequency synthesizer that drives the SO.

Talk duration: 20 minutes (plus 5 additional minutes for questions and answers).

## Session 3 (continued)

**Markus Mueller , Ralf Kakerow, Stephan Boecker (Nokia, Bochum, Germany)**

*IST European project MuMoR – New approach for frequency synthesizers in multi-mode radio applications*

Frequency synthesizers in multi-radio wireless transceivers have to cope with various differences in standard related parameters like tuning range, phase noise, and switching time. That typically leads to dedicated architectures to fulfill technical requirements in an optimized way. On the other hand, cost requirements force high integration and component sharing for various standards. An interesting approach to solve this conflict is multi-architecture frequency synthesis, supporting both Integer-N and Fractional-N PLL architectures by sharing main hardware. Key component of that approach is a configurable frequency divider that provides a wide division range with low power consumption. Introducing software control allows the adaptation to each operating mode. The presented multi-mode frequency synthesizer is designed for multi-mode GSM900/1800/1900/WCDMA/HSDPA wireless transceiver systems.

Talk duration: 20 minutes (plus 5 additional minutes for questions and answers).

**3.35 p.m. to 4.00 p.m: Coffee Break**

## Session 4: General aspects for mobile communications

**Nicolas Schlumpf (EPFL, Electronics Laboratories, Lausanne, Switzerland)**

*IST European project MuMoR – A fast modulator for dynamic supply linear RF power amplifier*

Conventional RF power amplifiers (PAs) usually give their maximum efficiency near the maximum output power level. When the output power decreases, the efficiency drops sharply. Deep class AB or B PAs improve their efficiency by a self-adaptation of the current drawn from the power supply. However, in many cases, both deep class AB and B do not provide enough linearity like, for instance, in CDMA applications where spectral re-growth is of first concern. From class A to class B, RF PAs face the linearity-efficiency trade-off. The class A is linear but power inefficient, whereas class B is efficient but has a poor linearity.

An alternative to the linearity-efficiency trade-off is to dynamically adapt the power supply voltage of a linear PA. The linear PA is of class A or of moderate class AB and its collector or drain voltage is adapted to avoid RF output voltage to saturate. This same principle has been called dynamic power supply, bias adaptation, and envelope tracking.

A fast modulator for dynamic supply linear RF amplifier has been integrated in a 0.35 $\mu$ m CMOS technology. The use of this modulator with an external linear Power Amplifier (PA) allows to maintain its efficiency at a higher level than it would with the same PA supplied at constant voltage. The modulator is designed to track rapid envelope variations at high efficiency without compromising the RF PA linearity.

The design and the measurements of a fast modulator for dynamic supply linear RF PA are presented during this talk. The modulator integrates all the required functions to efficiently convert a low-level varying RF envelope to a high-level supply for an external RF power transistor.

The linearity of the dynamic supply PA supplied by the modulator is a function of the input power and of the envelope bandwidth. Thanks to the fast modulator design, the linearity dependence on the envelope bandwidth remains controlled up to 2MHz. Within the linear range of the dynamic supply PA, the efficiency is greater than its constant supply counter part.

Talk duration: 35 minutes (plus 5 additional minutes for questions and answers).

**Marc Laugeois (CEA, LETI, Grenoble, France)**

*IST European project MuMoR - Reconfigurability approach on hardware Design for UMTS terminal*

The purpose of the baseband part of the MUMOR project is to prove the reconfigurability of a UMTS terminal.

The terminal has to deal with three transmission standards: TDD, FDD, FDD/HSDPA. Reconfigurability means the ability of merging of these three modes, getting a good silicon area / performance / power consumption trade-off.

Another aspect is the hardware resources reuse.

The synchronisation is one of the main module. The goal is to recover the frame and slot synchronisation, and the scrambling code used which identifies the transmission cell.

Although the mechanisms of synchronisation decoding for TDD and FDD modes are based on the same sequences, the way it is carried out presents some differences.

Thus, the in depth study of the algorithm reconfigurability is a key point in the conception of a reconfigurable chain. Currently, the synchronisation module is very hardware and power consuming due to the operations processed out (match filtering, correlation, look-up table addressing, maximum seeker).

Mode-merged architecture and scheduling will be presented, a synthesis result targeting FPGA platform will be given.

Talk duration: 15 minutes (plus 5 additional minutes for questions and answers).