



# Re-configurable Multi-mode Radio Architectures for enhanced 3G Terminals

## – ABSTRACT –

- **Working Group:** WG 6 “Reconfigurability”
- **Addressed objectives:** (c) Contributing towards the already identified research areas  
(e) Sharing information about, or results from, complementary research projects or activities outside the Forum
- **Title of the research item:** Re-configurable Multi-mode Radio Architectures for enhanced 3G Terminals
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- **Subject Area:** Base band and RF architectures,  
Re-configurable Equipment Management and Control,  
Re-configurable Modem RF/BB
- **Relevance of the Topic to the Objective(s):** The IST funded project MuMoR project undertakes research in the area of power and area optimized implementations of 3G and enhanced 3G (HSDPA, insertion of WLAN) UE terminals in both FE and BB domain. This paper gives an overview of the most critical research issues to be tackled as well as first project results, i.e. approaches to overcome the major obstacles.

## I. INTRODUCTION

The IST funded project MuMoR (Multi-Mode Radio) has its main objectives in investigating mobile terminal architectures for multi-mode operation. The investigated radio systems are mainly UMTS/FDD, UMTS/TDD, and HSDPA/FDD. Additional investigations towards the operability with other cellular and non-cellular standards like GSM and WLAN (IEEE 802.11 a/b) are also considered.

MuMoR covers physical layer aspects for the analogue RF part as well as for the digital baseband part of a terminal. Because of investigating the analogue and digital parts of the system in only one project, particular attention will be on the simulation of the overall transceiver system and the definition and design of the interface circuits, like the ADC.

In Figure 1 the overall system design and simulation flow established in the project MuMoR is depicted. According to traditional design methodologies for the analogue front-end and digital baseband an overall system approach has been introduced based on a high-level C/C++ description. Speciality of this approach is the inclusion of separate front-end blocks models that allows detailed front-end partitioning and block specification already on abstract system level. This way a global optimization considering the whole transceiver system becomes possible. Further advantage is the simulation of RF behavior and baseband functionality in one simulation environment and so in a common test bench [1][2].

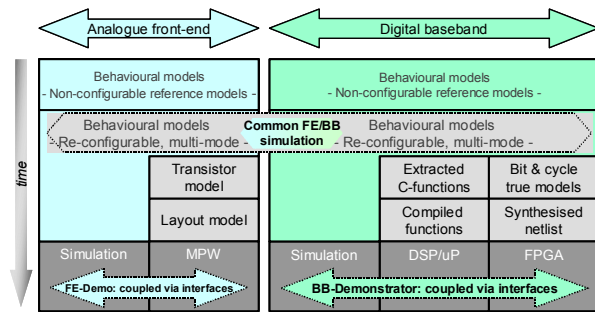


Figure 1 - Overall System Design and Simulation Flow

Section II of this abstract presents the research areas and results in the radio frequency front-end domain, whereas section III focuses on investigations concerning digital baseband.

## II. RADIO FREQUENCY FRONT-END

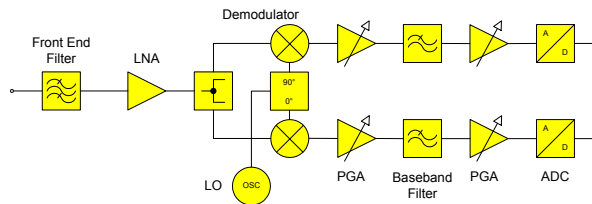
The radio frequency front-end is the interface between the antenna and the digital baseband-processing unit. In the project MuMoR front-end architectures and circuit components are investigated for their eligibility in multi-mode cellular transceiver systems. A main parameter in this analysis is power consumption that has to be minimized for use in mobile applications. In a first phase multi-mode operation for UMTS FDD/TDD, HSDPA is

investigated taking into account the frequency re-configurability for GSM. Further extension of the architectures and re-configurable techniques towards other standards is a general target that the base approach should support.

### A. Architecture Studies

Aim of multi-mode architectures with respect to the use in mobile devices is the suitability for high integration. That means that the number of external components has to be reduced to a minimum. On top most of the individual front-end blocks should be re-configurable and re-useable in order to save die size and cost.

Various RF front-end architectures are established that could be used for the reception (RX) of the RF frequencies, including Superheterodyne, Low-IF and Direct Conversion Receiver (DCR). The Superheterodyne receiver is well established and used for many years, but it requires a variety of functional RF building blocks including filters which could not be integrated on the silicon chip, whereas the Low-IF architecture has the disadvantage that the required I/Q imbalance accuracy must be better as  $1^\circ$  deg in order to achieve the specified image suppression [3]. Another disadvantage of the Low-IF is related to the multi-mode operation where the filters for channel selection need to be re-configurable for support of the different standard. This is particular more complicated to achieve with the Low-IF receiver since polyphase and analogue baseband filters require a bandpass characteristic. The Direct Conversion Receiver (DCR) just uses lowpass filtering in the analogue baseband part, allowing a straight-forward adaption of the corner frequency and so being preferable concerning re-configurability issues. Research on the DCR architecture has shown that this topology is well suited for RF system integration [4][5]. In Figure 2 the architecture of a DCR used in the project MuMoR is shown. The analogue baseband filters have a 5<sup>th</sup> order butterworth characteristic that is distributed over several filter stages. The specification of the filters shows a flexible bandwidth, in order to be re-configurable between 2.3 MHz and 200 kHz to support the targeted standards [6]. Configuration of the corner frequency can be simply done by using capacitor arrays that are switched in dependence of the selected mode. With this approach the area requirements are defined by the lower corner frequency, when all capacitors are connected to the filter. Increasing the filter corner frequency by reducing the capacitance by disconnecting capacitors of the switching array does not increase capacitor area requirements. Of course additional area required for switches to vary the capacitance value, but this is very small in relation to the passive components area. Further re-configurability is introduced on the analog baseband programmable gain amplifier stages (PGA), and the data converters. Here the resolution is selectable between 8 bit and 10 bit, depending on the selected operating mode of the transceiver. In case of supporting GSM and 3G standards, also the converter sampling rate has to be adapted in a wide range.



**Figure 2 – Direct Conversion Receiver Architecture**

A similar re-configuration strategy can be applied to transmit (TX) path and frequency synthesis. The latter one is challenging in particular, as it usually contributes significantly to the total transceiver power consumption due to the high synthesizer frequency in DCR architectures. This is especially true for multi-mode operation. Here, critical parameters like phase noise requirements in GSM and high operating frequency in UMTS require careful architecture partitioning and re-configurable approaches for each component to avoid over-designing the circuit against the specification for the selected standard.

A preferred architecture for frequency synthesizers is the Integer-N PLL architecture that offers good performance and power consumption behavior. Like in RX and TX paths, an integrated solution is preferable to minimize cost. On the other hand the fully integration of a VCO is still challenging for wireless transceivers. An alternative can be the Fractional-N approach that provides better phase noise by sigma-delta modulation and a faster settling time by introducing a larger loop bandwidth [7]. The additional flexibility of the Fractional-N architecture must be paid with a higher complexity, resulting in higher power consumption. So a trade-off between frequency synthesizer architecture and integration level has to be found under given specifications like settling time, phase noise, and power consumption.

Below a concept of a re-configurable voltage controlled oscillator (VCO) providing a good phase noise performance is described more in detail.

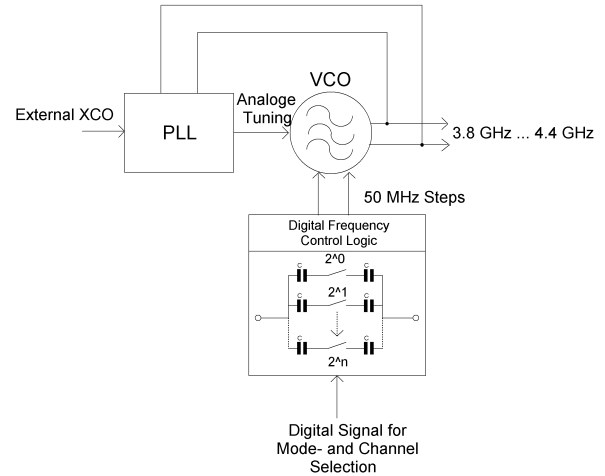
### B. Re-configurable Voltage Controlled Oscillator

The voltage-controlled oscillator (VCO) is a key component in synthesizers for wireless transceivers and therefore important for accurate frequency generation. As UMTS/FDD and HSDPA/FDD are frequency duplex modes at least two oscillators are required for transceiver operation. UMTS/TDD can even be handled by a single oscillator. Considering also GSM900/1800 compatibility, a total tuning range between 3420 MHz and 4340 MHz has to be covered. This is twice (for GSM900 four times) the required frequencies, as the direct conversion architecture is quite sensitive to injection pulling and other coupling between VCO local frequency (LO) and the RF signal.

An approach that is useful for multi-mode operation considers two oscillators. One of them covers all GSM modes and UMTS/FDD transmit channel, while the other handles UMTS/FDD receive channel and UMTS/TDD

mode. This results in two VCO's, each covering a frequency range of 540 MHz.

A block diagram of a multi-mode VCO is depicted in Figure 3. Additional to the analog tuning voltage from the PLL feedback loop, this VCO comprises a configurable resonator tank. Configuration is realized by inserting a CMOS switched resonator capacitor matrix. The switches are controlled by a decoded digital control word, allowing a variable oscillator gain ( $K_{VCO}$ ). This way an optimum trade-off between phase noise, power consumption, tuning range, and sensitivity to control signal noise is obtained.



**Figure 3 – Multi-mode Voltage Controlled Oscillator**

The most severe requirement on the spectral purity of the VCO is the phase noise in GSM standard that has to be smaller than  $-145$  dBc/Hz at 20 MHz offset when the radio is in transmit mode. Even today this requirement is still a challenge for a VCO that is fully integrated on a transceiver chip. Simulations have shown that this parameter is achievable by careful VCO design even in standard BiCMOS technology (70 GHz/0.25um).

## III. RE-CONFIGURABLE DIGITAL BASEBAND

### A. Motivate Re-configurability in the digital baseband

Terminals for 3G and enhanced telecommunication systems require a tremendous amount of high-speed signal processing in the digital baseband. This demand is caused by the selection of algorithms, which have to be implemented to achieve a sufficient performance. Furthermore the traditional design alternatives, namely hardwired ASICs and SW on digital signal processor, which are used in the implementation of single-mode systems, are no longer feasible for multi-mode systems operating in a high data rate regime. The SW solution on processors would well support the multi-mode design, but often is too slow or inefficient in terms of power consumption. The HW solution on the other hand is not flexible enough to take advantage of the similarities of the systems and requires the parallel implementation of each of the systems, which is not at all area efficient.

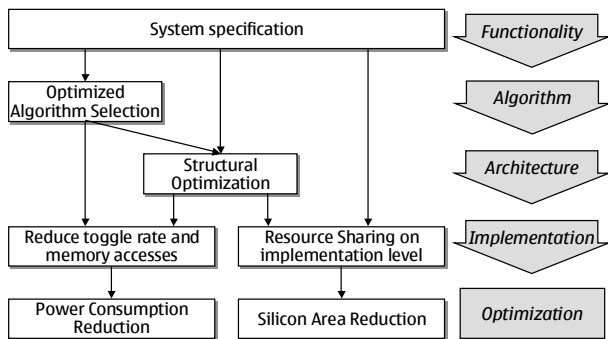
The scenario, which has been examined here, is a system that either operates in FDD mode using UMTS and HSDPA channels or in TDD mode using UMTS channels only. The fact that in this scenario two similar systems operate mutual exclusive in time offers some potential for re-configuration, that enables resource sharing on the implementation level, thus leading to a more area-efficient design. However optimization in terms of area is only one issue, having an eye on the power consumption is often even more important.

The optimization of design time and design cost have been neglected here for two reasons: First, it is extremely difficult to measure the cost and time required for implementing the final solution without the detours and cul-de-sacs, which have been taken during the establishing of the final solution. Second, some of the new design steps take much time because there is a lack of tools to support them. This may quickly change as soon as a change in the design flow is widely accepted and tool vendors react accordingly. The design time and cost estimations would be fundamentally dependent on tool availability.

*B. Favoring Re-configuration by Algorithm Selection*

Though the final re-configurability of the design has to be apparent in the implementation there are some measures to be carried out during the definition of the applied algorithms to favor the implementation. This is similar to a power optimization process, which also has to be applied at all levels of abstraction in the planning and design to have most success.

One key issue during the selection of algorithms to favor the re-configurability is to find algorithms using the same kind of fundamental operations or common set of operations. During the conception of a *single-mode* system there is only a trade-off between performance and implementation effort whereas in a *multi-mode* system this optimization becomes a multi-dimensional problem due to its effect on the performance on all modes to be supported.



**Figure 4 – (Multi-mode) Design Optimizations**

Figure 4 shows in a graphic representation how the system specification can either directly offer potential for e.g. resource sharing inherently. Alternatively the combination of a clever algorithm selection with a structural optimization, i.e. the addition of means on architectural level, may also offer potential for resource sharing thus

reducing the silicon area either for removing registers and combinational logic or by reducing the amount of memory required.

In our scenario we started with optimal algorithm solutions for the distinct modes FDD and TDD. For the channel estimator (CE) this meant using a correlator based CE operating on the Common Pilot Channel and Rake receiver for FDD on the one hand and a DFT based CE (Steiner Algorithm [8]) operating on the midamble with Joint Detection for TDD on the other hand. For a single-mode system these different solution are doing well but for a FDD/TDD multi-mode system it has to be checked if there is a more optimal solution. This means that after modifying the algorithm selection towards a *common* optimum a certain loss in performance and/or increase in computational complexity may occur but the benefit for the final implementation can still prevail.

Here the Steiner algorithm has been replaced by a correlator based one as preferred in FDD. The advantage of this compromise is that the FDD solution is not affected at all, which makes it easier to determine the “cost” of the optimization. In our case simulation showed that the computational complexity did increase for TDD to achieve similar performance for the test cases defined by 3GPP, e.g. “DL reference measurement channel (2 Mbps), 3.84 Mcps TDD Option” according to chapter A.2.8.1 of [9]. Still the obvious benefit is the re-use of HW components in this case the correlator structure for both modes. There is no need to additionally implement an FFT structure in parallel any more.

The argumentation above assumes that the implementation of the components will be in HW. In the case of the CE this assumption can safely be made. For components that will be implemented in SW on a DSP it is much more difficult to express the gain in such case. However there are cases, where it is still apparent, e.g. when the DSP has special support for certain algorithms, these ones should be used preferably. Other examples are shown in the subsequent sections.

*C. Implementation Level Optimizations*

The final results of any optimization process will be visible on implementation level. This means that in the end the architecture and the implementation have to support the optimizations, which have been made on algorithm level. For a multi-mode design this often means that a certain degree of flexibility has to be achieved, namely more flexible than dedicated HW but with competing performance, i.e. re-configurable or soft-configurable.

There have been several approaches developed by academic institutes and industry to achieve a soft-configurable design. The approaches can be grouped into three main categories:

*1. Monolithic microprocessor with extensions*

Proposals of this category are centered around one general-purpose microprocessor, which is very similar to other

well-known microprocessors or DSPs and therefore the design-flow for control-oriented programming is very similar to application development on DSP platforms. The main difference are the extensions of ASIC-like parts within the microprocessor in order to speed up certain operations so that the high processing power demands of telecommunication applications can be met. The biggest problem in this approach is the bottleneck of data throughput because all data mostly has to be transferred via the processor bus. (Example: [10]).

### 2. FPGA-like structure with big number of low complexity processing elements

Other approaches can be characterized and compared to FPGA-like structure having a symmetrical matrix interconnection network and consist of many low-complexity processing elements, which are mostly identical but in some cases can be a set of a few different cells to solve distinguished computation problems. The speed up is mainly achieved by massive parallel processing. Algorithms are divided into very basic operations mostly not more complex than additions or multiplications. In this approach the significant problem lies in the great challenges of the compiler to keep all processing elements busy in operation to maximize the efficiency. (Example: [11])

### 3. Multiprocessor concepts

Concepts of the last category are based on a multiprocessor approach. This is defined by a network of complex general purpose processors, which are similar to already available cores connected by a processor bus or communicate via shared memory. The design flow is still very similar to developing applications on single-processor systems for parallelizable algorithms, but as more communication between parallel computed algorithms is needed the effort of synchronization and scheduling becomes more and more obvious to the designer. A problem that can occur in this approach is the bottleneck of data throughput on the shared processor bus. (Example: [12])

For our implementation we selected an implementation, which would best fit to the first category we defined. To keep the most flexibility it is microprocessor-centric with extensions for acceleration for selected operations. In section D an example for a useful extension to a DSP for the investigated enhanced 3G scenario will be given.

Up to this point we focused on the optimization of computational parts of the design, the combinational logic and registers. But beside the computation there is a second domain that has to be covered by the implementation independent of the HW/SW partitioning: The storage of (intermediate) data. When a system is operating in different modes one can imagine that the amount of data to be stored varies for the different components. If the HW architecture allows the usage of centralized shared memories which several modules of the digital baseband can access, the required *total* memory for the system is

ideally as big as the memory requirements of the operating mode with the *biggest* memory consumption, i.e.

$$\text{mem}_{\text{total}} = \text{MAX}(\text{mem}_{\text{mode } 1}, \text{mem}_{\text{mode } 2}, \dots, \text{mem}_{\text{mode } n}).$$

The scenario we investigated offers some potential to share memory. The Cell Searcher (CS) requires different amount of memory depending on the operating modes FDD and TDD. The front-end of the CS as depicted in Figure 5 mainly consists of two parts, the P-SCH matched filter and the S-SCH correlator. The arithmetic of the P-SCH computation in FDD and TDD is similar (correlation), but TDD requires more memory compared to FDD. But when we recall that in our scenario during FDD operation also the High-Speed channel may be active it is easy to find a usage for the additional memory: The H-ARQ buffer between the two stages of the rate matcher, which is only required for the high-speed channels and not in our TDD. Depending on the UE category the number of soft bits available in the virtual IR buffer ( $N_{\text{IR}}$ ) may have a size of up to 28.800 soft bits. [13]

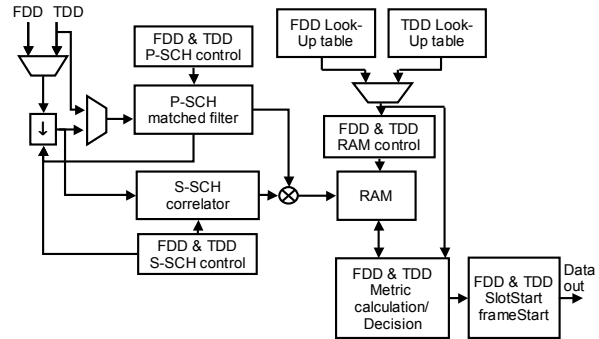
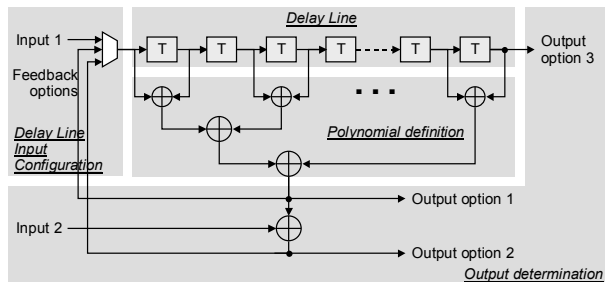


Figure 5 – FDD/TDD Cell Searcher

### D. Re-configurability through DSP co-processing

The most flexible approach is the ideal software radio, performing all computations in one or more DSPs. However in the physical layer of radio communication systems there are typically several algorithms operating on bit-level, which could be done on a DSP but are very inefficient because normal DSPs do only allow operation on byte, word, or bigger data structures. Also register and memory accesses to not allow bit-level operations. In the UMTS/HSDPA physical layer the following operation can be counted to this class:

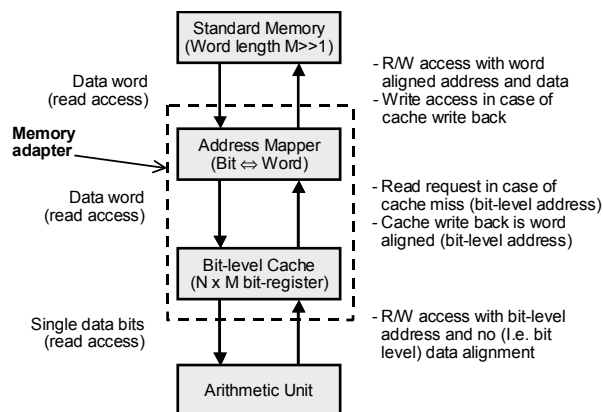
- CRC Encoder (used in all modes) (\*)
  - CRC Decoder (used in all modes)
  - Turbo Encoder (used in all modes)
  - Convolutional Encoder (used in FDD and TDD modes)
  - Bit Scrambler (used in TDD mode)
  - Bit DeScrambler (used in TDD mode) (\*\*)
- (\*) includes UMTS/FDD, HSDPA/FDD and UMTS/TDD  
(\*\*) operating on the sign bit of the softbit representation



**Figure 6 – Abstract universal bit level arithmetic unit**

Figure 6 shows an abstract view of an universal bit level arithmetic unit which can –when configured correctly– fulfill all the operations listed above, which are all based on bit pipeline, bit shift registers or filter structures with XOR operations on different stages of the pipeline. There are several kinds of configurations possible, i.e. for input signal, output signal, polynomial definition and length of the delay line. For example the filter output can be used directly as output data stream (Output option 1 in the figure) or further operations to be done with this data stream, e.g. add an input sequence on it (output option 2).

To further optimize the operation of this bit level arithmetic unit it is useful to have a dedicated memory adapter to map the words from the memory into single bits and vice versa. What is needed is a compressing unit that uses all bits of a memory word by storing neighboring bits into one standard memory word. With this approach the required amount of standard memory words will be reduced. To also reduce the number of memory accesses a cache is required, that maps the memory words to a bit level memory and includes the typical cache functionality like writing back after modifications and also requires some kind of address decoding as depicted in Figure 7. The bit-level cache is being addressed with a bit level address, i.e. the number of a bit. As the bit level operations typically operate on successive bits a burst read and write access should be available. The standard memory access, which the cache has to perform in case of write back (write access) and cache miss (read access) has to be handled by an address mapper, which contains e.g. a look-up table (LUT) to generate the standard memory address out of the bit-level address, which the cache uses.



**Figure 7 – Bit-to-Word Memory Adapter**

The advantage of combining the flexible bit level arithmetic unit with the presented memory adapter is that the number of memory adapters can be reduced because the attached arithmetic unit does process several different algorithms, thus only few of them are required, depending on HW performance and system demands. [14]

Beside computation and data storage there is a third domain, which gains importance when the architectures become more and more complex and the number of components increases. This domain is the communication, i.e. the bus systems. The application of a small bus system, which is still sufficient in terms of flexibility and performance, is as well relevant for the system features. However, for our scenario and architecture this area still has to be investigated.

#### IV. SUMMARY

Different architectures and techniques for re-configurable multi mode radios have been presented and discussed. On the radio front-end side a suitable receiver architecture has been shown and techniques to reconfigure circuits and sub-systems have been explained. Subsequently the properties of a multi-mode capable VCO have been presented. For the digital baseband several techniques to implement a re-configurable multi-mode radio have been discussed. Approaches on algorithms and implementation level have been presented covering computation and memory optimizations for reduction of area and power consumption. Techniques and components to build a flexible but still usable modem capable of supporting multiple operation modes have been shown.

#### V. ACKNOWLEDGMENT

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