

A Fast Modulator for Dynamic Supply Linear RF Power Amplifier

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Abstract—A fast modulator for a dynamic supply linear RF amplifier has been integrated in a 0.35- μm CMOS technology. The use of this modulator with an external linear power amplifier (PA) allows to maintain its efficiency at a higher level than it would with the same PA supplied at constant voltage. The modulator is designed to follow rapid envelope variations at high efficiency without compromising the RF PA linearity.

Index Terms—Dynamic supply power amplifier, efficiency improvement, power amplifier, radio frequency.

I. INTRODUCTION

CONVENTIONAL RF power amplifiers (PAs) usually give their maximum efficiency near the maximum output power level. When the output power decreases, the efficiency drops sharply. Deep class-AB or class-B PAs improve their efficiency by a self-adaptation of the current drawn from the power supply. However, in many cases, neither deep class AB or B provides enough linearity as, for instance, in CDMA applications where spectral regrowth is of primary concern. From class A to class B, RF PAs face the linearity–efficiency tradeoff. The class A is linear but power inefficient, whereas class B is efficient but has a poor linearity.

An alternative to the linearity–efficiency tradeoff is to dynamically adapt the power supply voltage of a linear PA with respect to the instantaneous envelope value of the modulating signal. The linear PA is of class A or class AB and its collector or drain voltage is adapted to avoid RF output voltage to saturate. This same principle has been called dynamic power supply in [1], bias adaptation in [2], and envelope tracking in [3]. Nevertheless, this last name is not appropriate because the “envelope tracking” method refers to the power supply adaptation with respect to the long-term rms or burst-by-burst envelope value [4]. The correct description would be “envelope following” technique.

The principle of the dynamic supply PA is presented in Section II. Section III is a study of the impedance seen from the supply pin of the PA at RF envelope frequencies. A good understanding of the PA supply impedance is required for the design of the modulator (Section IV). Section V describes the circuit

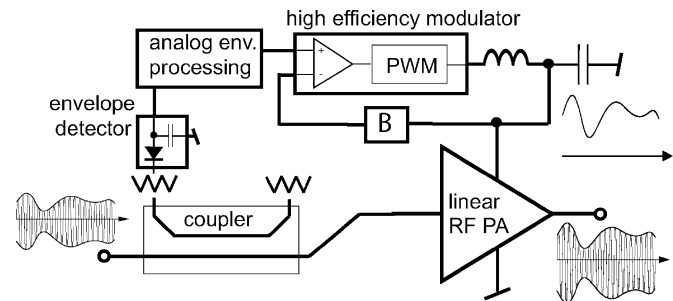


Fig. 1. Dynamic supply PA block diagram.

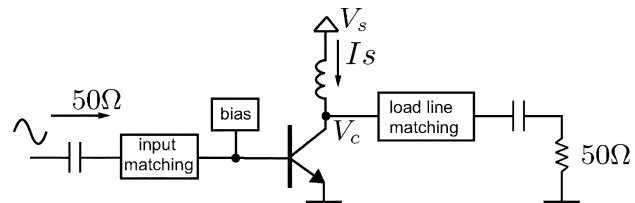


Fig. 2. Linear PA schematic.

design in a 0.35- μm CMOS process, Section VI presents and discusses experimental measurement results, and Section VII is dedicated to RF simulation of the dynamic supply PA. Finally, some conclusions are given in Section VIII.

II. PRINCIPLE OF THE DYNAMIC SUPPLY PA

A. Basic Block Diagram

The detailed block diagram (Fig. 1) shows a linear RF PA, a directional coupler, an envelope detector to measure the coupled incident power, an analog envelope processing block, and a high-efficiency modulator. The modulator is a fast high-efficiency step downconverter transforming the main power supply into a varying supply voltage for the PA. The PA varying supply voltage is dynamically adapted, proportionally to the peak input envelope voltage, such that no RF output voltage compression occurs at the PA's output.

B. Linear PA

To implement the dynamic supply principle, a moderate class-AB PA based on a single-stage commercial Si bipolar junction transistor (BJT) with an f_T of 25 GHz has been used. Fig. 2 represents the basic schematic of the PA with input matching and optimum load line matching for maximum output power operation. The single-stage PA has a 12.5-dB power gain and provides 22 dBm at the 1-dB compression point.

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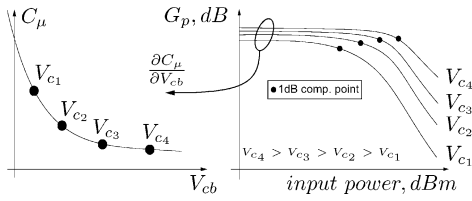


Fig. 3. Miller capacitance C_μ versus collector-base voltage V_{cb} and power gain G_p sensitivity to the supply voltage V_c, V_s .

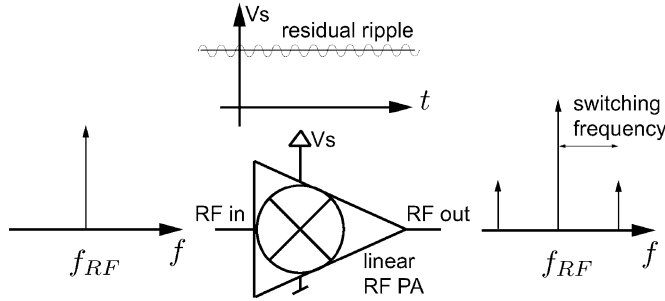


Fig. 4. RF leakage of residual supply voltage ripple.

C. Power Gain Sensitivity to Supply Voltage

As shown in Fig. 3, increasing the collector voltage V_c of the PA improves the 1-dB compression point. Normally, the collector voltage can be decreased down to the knee voltage but power gain (G_p) reduction due to Miller capacitance practically limits the minimum voltage to 1 V. At low collector voltage, the power gain sensitivity to the supply voltage is higher. The power gain sensitivity to the supply voltage and the residual supply voltage ripple due to switching operation convert the linear PA into a mixer as shown in Fig. 4. The RF output spectrum contains mixing products of the residual supply voltage ripple with the RF input signal. To keep these unwanted products as low as possible, residual output ripple and PA power gain sensitivity to supply voltage should be small.

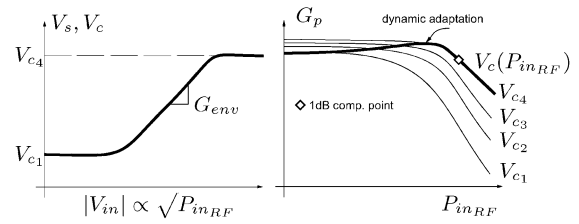
D. Supply Voltage Control

The control of the PA supply voltage is done in such a way that the resulting power gain G_p and its phase remain as constant as possible over the widest input range. The input range is the forward coupled input envelope amplitude $|V_{in}|$. Fig. 5 describes the relation between the supply voltage and the input envelope amplitude. The analog envelope processing block of Fig. 1 consists of a gain G_{env} and a sum taking into account the RF transistor output characteristic knee voltage (V_{knee}).

The 1-dB compression point of the dynamic adaptation power gain is often higher than the one obtained at the maximum constant supply voltage V_{c4} . Hence, the dynamic supply PA has a higher linear range.

E. Efficiency Improvement

With the dynamic supply PA principle, the overall PA efficiency is improved for output power levels below the maximum linear output power. This property is useful for complex modulations with large peak-to-average ratio and low peak envelope occurrence. Equation (1) gives the maximum



$$\begin{aligned} G_{env}|V_{in}| + V_{knee} < V_{c1} &\Rightarrow V_c = V_{c1} \\ G_{env}|V_{in}| + V_{knee} \geq V_{c1} &\Rightarrow V_c = G_{env}|V_{in}| + V_{knee} \end{aligned}$$

Fig. 5. Function $V_s(|V_{in}|)$ and dynamic adaptation.

efficiency improvement of a class-A PA, which current does not vary much with RF input power:

$$\Delta\eta \propto \frac{V_{c4}}{V_{c1}}. \quad (1)$$

For a reduced conduction angle PA, the efficiency improvement can be higher, to the detriment of the linearity.

F. RF Distorsion Added by the Dynamic Supply Principle

Fig. 5 illustrates a continuous wave (CW) measurement of the power gain G_p where the input power is swept with a long sweep time. In the case of rapid modulation, the envelope can vary quickly over a wide range. For the CW test of Fig. 5, this corresponds to a short sweep time. In such a case, and with a variable supply, the gain response should remain unchanged. If the sweep time is reduced, several imperfections cause the gain response to deviate from the ideal response of Fig. 5. Two factors bring about these imperfections.

- 1) The transistor has large power variation and is self-heating sensitive. Temperature variations turn into variations of bias point because of the base-emitter temperature-to-voltage dependency. This is known as bias modulation [2] and can have a strong impact on RF linearity.
- 2) The imperfect amplitude and phase response of the modulator introduces a gain error and a compression of the RF output signal.

1) *First Imperfection:* A mirrored PA configuration (Fig. 6) having a low thermal resistance partly corrects the first imperfection. It provides a low impedance bias source for linear PA operation with negative temperature feedback to prevent thermal runaway. The transistor Q2 is the RF device and Q1 is the mirror device. The electrothermal model [6] approximates the temperature dependency of the base emitter junction voltage with a voltage-controlled source in the emitter ($S_T = -1.6, \dots, -2.2 \text{ mV}/^\circ\text{C}$) [8], [9]. The heat flow propagation model is a one-dimensional RC type of transmission line. The dissipated transistor power is roughly equal to the product of the collector-emitter voltage with the collector current. For small power variations, the bias current of the RF device Q2 is modulated according to (2):

$$\Delta I_{c2} = (\Delta T_{j2} - \Delta T_{j1}) \cdot gm_2 \cdot S_T = \Delta T_j \cdot gm_2 \cdot S_T. \quad (2)$$

Even though the current in the mirror device Q1 is constant, the junction temperature difference ΔT_j modulates the power device bias current, which may not be appropriate for good RF

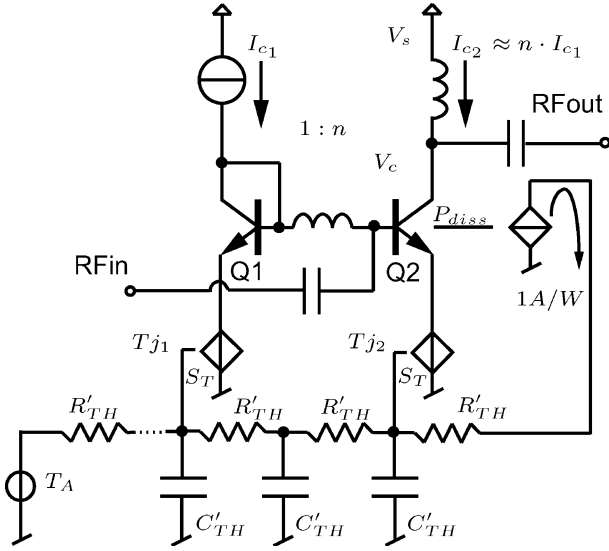


Fig. 6. Mirrored PA configuration and electrothermal model.

linearity. Moreover, ΔTj is not necessarily in phase with the power variation, resulting mainly, in the case of the dynamic supply PA, from Q2 collector voltage variation. Thermal current modulation can thus also affect the PA load, which is studied in Section III.

Bias current modulation is not advisable for high RF linearity because the PA power gain Gp can be modulated. Referring to Fig. 3, Gp is divided in two parts, a constant power gain for small input power (Gps) and a compression characteristic at high input power (Gpl). For linear PAs working with large biasing collector current, moderate modulation of the current does not have a strong impact on Gps . The unilateral maximum power gain GTU , from which the maximum oscillation pulsation w_{max} [7] is found, is considered here and given by (3):

$$G_{TU} = \frac{r_o \cdot |ib \cdot \frac{\beta(j\omega)}{2}|^2}{rb \cdot |ib|^2} \approx \frac{1}{4} \cdot \frac{\omega_T}{\omega^2 \cdot rb \cdot C_\mu},$$

$$\text{with } r_o \approx \frac{C_\pi + C_\mu}{C_\mu} \cdot \frac{1}{gm}. \quad (3)$$

The transistor load is matched to the output impedance of the transistor r_o , and the influence of the base resistance rb is neglected for r_o . Gps dependence with the current comes from the dependence of the transition pulsation ω_T with the current. The relation $\omega_T(I_c)$ exhibits a maximum at high collector current, hence Gps current dependency is moderate. However, the bias current modulation can significantly modify the gain compression Gpl and generate RF distortion.

2) *Second Imperfection*: A fast modulator design reduces the second imperfection. Although the dynamic supply PA principle does not require V_s to replicate exactly the envelope, the delay and the large amplitude errors, due to modulator speed limitations, have an impact on the RF distortion. The design of the modulator and its speed limits are studied in Section IV.

III. EQUIVALENT PA CIRCUIT AS LOAD FOR THE MODULATOR

The equivalent PA circuit as load for the modulator is the impedance seen from the V_s pin of Fig. 6. This impedance de-

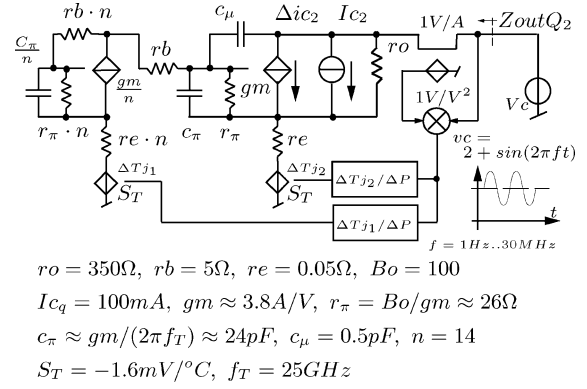


Fig. 7. Current-mirror small-signal model with thermal dependence.

pends on the low frequency applied to the V_s pin and the RF input signal power.

A. Low-Frequency Dependence

The current-mirror output impedance can be determined with a sine wave stimulus on V_s , the collector current variation obtained by either a simulation or a measurement. The low-frequency stimulus range covers the baseband frequency up to the switching frequency of the modulator. At these frequencies, the inductor in the collector of Q2 can be neglected, hence V_s and V_c are considered equal. The current-mirror output impedance is given by (4):

$$Z_{outQ2} = \left(\frac{\Delta V_c}{\Delta I_{c2}} \right). \quad (4)$$

To simulate the model of Fig. 6, the power to thermal transfer function $\Delta Tj_1/\Delta P$ and $\Delta Tj_2/\Delta P$ has to be known. Appendix A gives a method to determine these transfer functions based on a three-dimensional (3-D) meshing of the current-mirror PA die.

As the manufacturer does not provide any large-signal model, a small-signal model has to be used keeping in mind that simulation results remain valid only if the condition $|\Delta Tj| \cdot S_T \ll U_T$ is verified. The model parameters are extracted from the small-signal S parameters and from the bias current. Fig. 7 shows the current-mirror small-signal model with thermal dependence. A dc current source for the quiescent current of Q2 is part of the small-signal model to correctly evaluate the variation of the dissipated power ΔP which is given by (5):

$$P = (V_c + \Delta V_c \cos(\omega t)) (I_c + \Delta I_c \cos(\omega t + \varphi))$$

$$\Rightarrow \Delta P = V_c \Delta I_c \cos(\varphi) \cos(\omega t) +$$

$$[\Delta V_c I_c - V_c \Delta I_c \sin(\varphi)] \sin(\omega t). \quad (5)$$

Fig. 8 represents the simulation and measurement results of the current-mirror series equivalent output impedance. At low frequency, the output impedance is mainly resistive and actually much lower than the theoretical output resistance r_o of the transistor. From a frequency of 10 kHz, negative thermal feedback cancels, thermal collector current modulation is out of phase, and the output impedance becomes slightly inductive. Around a frequency of 1 MHz, the output impedance is mainly resistive and its value approaches r_o . From a few megahertz, self-heating

becomes negligible. The active impedance, made of the Miller capacitance C_μ , the total base resistance, and the transconductance gm , tends to shunt the output resistance r_o of the RF device.

The measurement and the model of the output impedance of the current mirror show close correlation, which validates the electrothermal model of Fig. 7.

B. RF Input Power Dependence

The power series expansion of the BJT exponential law under CW RF signal $v_{be} = V_{beo} + \Delta v_{be} \sin(\omega_{\text{RF}}t)$ produces a dc collector current given by (6) and a fundamental current at the RF frequency given by (7):

$$i_{c_{\text{DC}}}(A) = i_{c_o} \cdot \left(1 + \frac{1}{2 \cdot 2!} \cdot A^2 + \frac{3}{8 \cdot 4!} \cdot A^4 + \dots \right) \quad (6)$$

$$i_{c_{\text{RF}}}(A) = i_{c_o} \cdot \left(A + \frac{3}{4 \cdot 3!} \cdot A^3 + \frac{5}{8 \cdot 5!} \cdot A^5 + \dots \right). \quad (7)$$

The normalized RF input amplitude is $A = \Delta v_{be}/U_T$ and the voltage imposed bias current is $i_{c_o} = I_s \cdot \exp(V_{beo}/U_T)$. For small amplitudes and for a linear PA, whose input impedance remains almost constant over an RF cycle, the dc collector current variation is proportional to the input power (A^2).

A PA works in class A as long as the fundamental current $i_{c_{\text{RF}}}$ is smaller or equal to the dc current $i_{c_{\text{DC}}}$:

$$i_{c_{\text{RF}}}(A_A) = i_{c_{\text{DC}}}(A_A) \Rightarrow A_A \cong 1.15. \quad (8)$$

The dc current drawn by the class-A PA is given by

$$i_{c_{\text{DC}}}(A_A) \cong i_{c_o} \cdot 1.37. \quad (9)$$

To supply the same RF current, a class-AB PA with one fourth the bias current ($i_{c_o}/4$) requires a normalized amplitude A_{AB} given by the following condition:

$$i_{c_{\text{RF}}}(A_A) = \frac{1}{4} \cdot i_{c_{\text{RF}}}(A_{AB}) \Rightarrow A_{AB} \cong 2.6. \quad (10)$$

For this normalized amplitude (A_{AB}) the dc current drawn by the class-AB PA is 3.6 times the bias current $i_{c_o}/4$:

$$i_{c_{\text{DC}}}(A_{AB}) \cong \frac{i_{c_o}}{4} \cdot 3.6. \quad (11)$$

For the same RF output current, comparison of relations (9) and (11) proves that a reduced conduction angle PA has much more variation of its dc collector current than a class-A PA.

The small-signal model of Fig. 7 has to include the RF signal envelope dependence. Fig. 9 is the full model of the PA as load for the modulator. It includes two kinds of RF signal dependence. The first one is a current source proportional to the RF input power and the second one acts on the dissipated power. An increase of the RF output power cools down the PA, while an increase of its input power heats it up. The resulting dissipated power P_{RF} is given by (12):

$$P_{\text{RF}} = (1 - G_p(V_c)) \cdot P_{\text{inRF}}. \quad (12)$$

The RF output power is deducted from the power gain G_p of the PA which depends on the supply voltage V_c , as shown in Fig. 4.

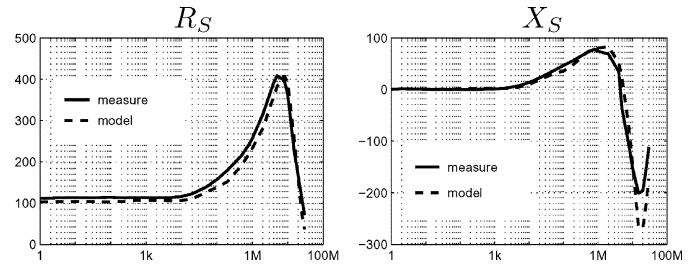


Fig. 8. Series equivalent of the current-mirror output impedance $Z_{outQ_2} = R_S + j \cdot X_S$.

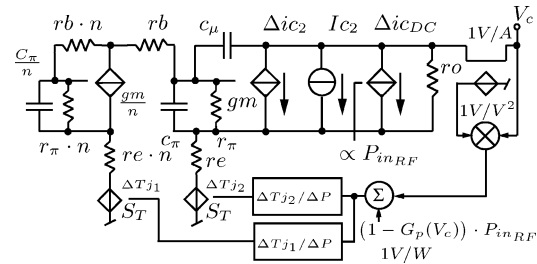


Fig. 9. Full model of the PA as load for the modulator.

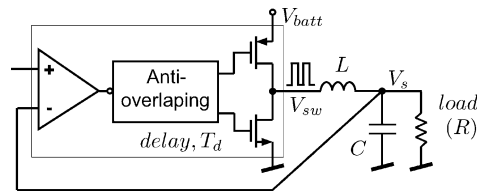


Fig. 10. Sliding-mode modulator with synchronous switch.

The full load model of Fig. 9 has two inputs, the collector voltage and the RF input power, both baseband signals. Thus, the full model allows to simulate the transient response of the modulator and its load without having to consider the RF frequency behavior of the PA.

IV. MODULATOR DESIGN

A. Modulator Requirements

The main concerns in the modulator design are speed and efficiency. The accuracy is less important because the supply voltage does not have to be a high-fidelity replica of the RF envelope as in the envelope elimination and restoration (EER) process [5]. Another constraint in the design of the modulator is to include the battery supply rail in its output range. This allows the PA to deliver maximum RF output power.

B. Sliding-Mode Modulator

Unlike conventional pulse width modulation (PWM) dc-dc converters, the sliding-mode modulator depicted in Fig. 10 does not have a slow feedback path. The output replicates the input with the filtered switched supply superimposed. The output can swing up to the supply voltage rails because the pulse width is not limited to a maximum or minimum value.

The synchronous switch reduces power losses associated with a standard buck converter by substituting an NMOS transistor for the commuting diode. This reduces the typical 0.7-V diode drop to 0.1 V or less and increases the system efficiency.

C. Design With a Resistive Load

Considering the load as a resistance R , the input-to-output transfer function is that of the LC filter. The switching frequency f_s can be predicted with the set of equations (13)–(15) assuming a 50% switched supply duty cycle and thinking of the modulator as an oscillator. The overall modulator delay T_d , the filter damping factor δ , and the LC filter natural frequency f_n determine the oscillation condition:

$$f_s \cdot T_d \cdot 2 \cdot \pi + \arctan \left(\frac{2 \cdot \delta \cdot \frac{f_s}{f_n}}{1 - \left(\frac{f_s}{f_n}\right)^2} \right) = \pi. \quad (13)$$

The damping factor is chosen equal to 0.7 for a flat frequency response. In this case, f_n and the -3 -dB cutoff frequency are the same. To get a low output ripple, f_s must be much larger than f_n . Thus, (13) expresses a tradeoff between the cutoff frequency and the output ripple. A small modulator delay T_d allows to achieve the best tradeoff, namely, maximizing the cutoff frequency while keeping the output ripple low. The comparator feedback inversion brings about the phase shift of π on the right side of the equation.

$$\delta = \frac{1}{2} \cdot \sqrt{\frac{L}{C}} \cdot \frac{1}{R} = \frac{1}{\sqrt{2}} \quad (14)$$

$$f_n = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}. \quad (15)$$

D. Output Ripple

Assuming a square switching supply waveform V_{sw} ranging from 0 V to the battery supply rail V_{batt} (Fig. 10) with variable duty cycle, the fundamental of this waveform, whose frequency is f_s , has an amplitude and phase characteristic shown in Fig. 11.

For a critical damping factor $\delta = 1/\sqrt{2}$, the LC filter attenuates the switching supply waveform fundamental. The filtered switched supply waveform fundamental mainly determines the output ripple, which is given by (16) for a 50% duty cycle.

$$v_{\text{ripple}} = \frac{2 \cdot V_{batt}}{\pi} \cdot \frac{1}{\sqrt{1 + \left(\frac{f_s}{f_n}\right)^4}} \cong \frac{2 \cdot V_{batt}}{\pi} \cdot \left(\frac{f_n}{f_s}\right)^2. \quad (16)$$

For duty cycles either above or below 50%, according to Fig. 11, the magnitude of the switching supply waveform fundamental decreases. The phase is a linear function of the duty cycle. Because of this phase change, (13) is not valid for duty cycles different from 50%. The LC filter phase [second term of (13)] has to change to compensate the switching supply waveform fundamental phase change and fulfill the oscillation condition. Hence, the switching frequency decreases and leads to less LC filter attenuation. However, thanks to the diminution of the switching supply waveform fundamental magnitude in Fig. 11, the output ripple remains almost constant with the duty cycle.

E. Design With a PA as Load

So far, the load has been considered constant. Recalling the analysis of the PA as a load in Fig. 8, the typical load at a switching frequency of 20 MHz is approximately $150 - j \cdot 220 \Omega$.

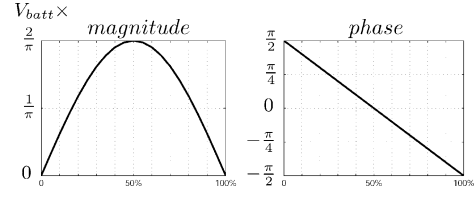


Fig. 11. Magnitude and phase of the switching supply waveform fundamental versus duty cycle.

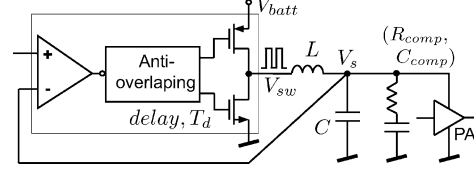


Fig. 12. Sliding-mode modulator with synchronous switch and compensation network.

In a parallel representation, the PA as a load has an equivalent circuit that is a resistance of 470Ω in parallel with a 24-pF capacitor. The capacitor can be part of C (Fig. 10) and it is good practice to have a proper broadband capacitive decoupling of the PA power supply. For example, referring to Fig. 10, with $C = 500$ pF, $R = 470 \Omega$, and $\delta = 1/\sqrt{2}$, the inductor should have a value given by (17):

$$L = 2 \cdot R^2 \cdot C \cong 220 \mu\text{H}. \quad (17)$$

The value of the inductor is much too large, at the switching frequency of 20 MHz. Such an inductor would work above or near the self-resonant frequency.

As the inductor value is proportional to the square of the load resistance R , it is obvious that the resistance has to be decreased. Fig. 12 proposes an RC compensation network that can be used to decrease the equivalent resistance at the switching frequency. For the example given here above, a typical compensation network would consist of $R_{\text{comp}} = 100 \Omega$ and $C_{\text{comp}} = 3.3$ nF. The capacitor is mainly used to block the dc current. The compensation network cutoff frequency is set such that the resistive part of R_s ($Z_{\text{out}Q_2}$) in Fig. 8 remains as constant as possible over the frequency. The equivalent resistance at f_s is now in the order of 80Ω , which allows to set the inductor to a value smaller than $10 \mu\text{H}$.

Within the modulation frequency range, the PA also represents a dynamic load for the modulator. Equation (9) shows that even the weak nonlinearity of a class-A PA can generate a variation of the current drawn by the PA (ΔI). When the envelope varies quickly during ΔT and approaches the compression, the inductor has to supply the load current demand ΔI . The inductor current change is limited by (18):

$$\frac{\Delta I}{\Delta T} \leq \frac{V_{sw} - V_s}{L}. \quad (18)$$

Moreover, when the compression is reached, the switched supply V_{sw} sticks to the upper rail and the output voltage V_s rises to the upper rail. Thus, the voltage across the inductor is small. If the inductor value is too large, the current demand ΔI cannot be supplied during ΔT . As a consequence, the output voltage is slew-rate limited.

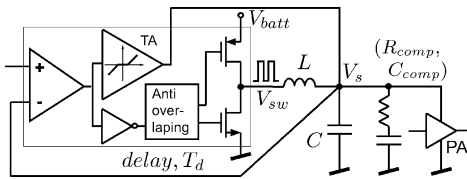


Fig. 13. Sliding-mode modulator with synchronous switch, compensation network, and transconductance amplifier (TA).

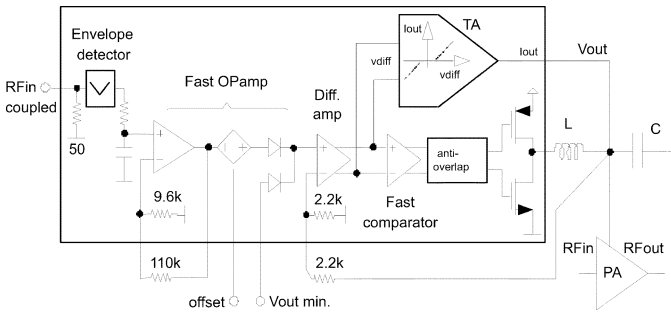


Fig. 14. Circuit diagram of the modulator IC.

To avoid slew rate and its associated PA distortion, the sliding-mode modulator of Fig. 12 is modified, according to Fig. 13, to include a transconductance amplifier (TA). The TA supplies the required current demand ΔI when the input error is greater than the expected output ripple.

V. CIRCUIT DESIGN

A. Technology Constraints

In the case of PA and modulator integration on a same chip, special care must be taken. Advanced technologies often have lower breakdown voltages which impacts negatively on the PA efficiency. Moreover, recalling (1), the dynamic supply PA principle is based on the maximum-to-minimum voltage ratio. Reducing the power supply lowers the potential efficiency benefit of this principle. Also, careful design of the package is mandatory. The on-chip supply voltages are noisy due to the sharp current transitions associated with the inductive nature of the package leads or bonds. Dedicated pads have to be used for the modulator and the PA supplies to reduce crosstalk. But substrate coupling and its impact on the RF output spectrum spurious are difficult to predict and makes the global result uncertain. Therefore, a conventional $0.35\text{-}\mu\text{m}$ CMOS process has been chosen to integrate only the modulator IC and to comply with most today's medium PA supply voltage requirements.

B. Design Aspects

The circuit diagram of the modulator IC shown in Fig. 14 consists of a broadband envelope detector with an on-chip $50\text{-}\Omega$ termination, a fast operational amplifier with 100-MHz unity gain bandwidth, a differential amplifier, a fast differential comparator, an output stage with R_{on} of $0.3\ \Omega$, and a TA. The chip microphotograph of the modulator is shown in Fig. 15. Many pads are used to output internal nodes and could be removed, which would halve the modulator size. The envelope detector has a sensitivity of $-10\ \text{dBm}$ and the on-chip termination has a measured voltage standing wave ratio (VSWR) of

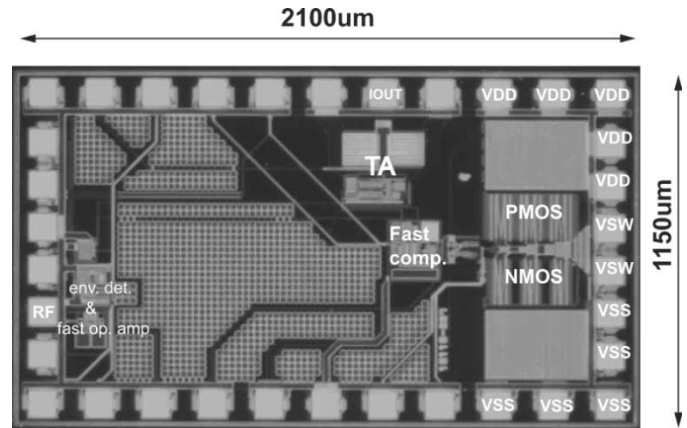


Fig. 15. Modulator chip microphotograph.

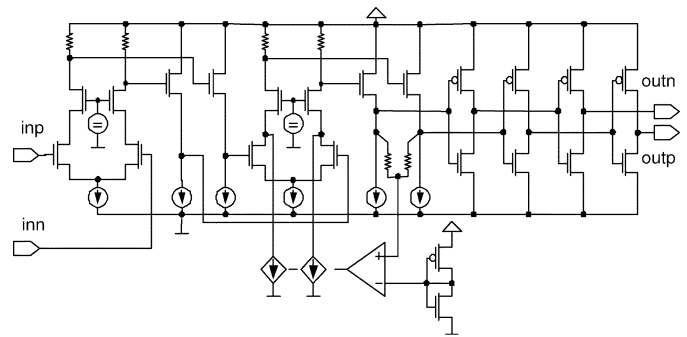


Fig. 16. Differential comparator schematic.

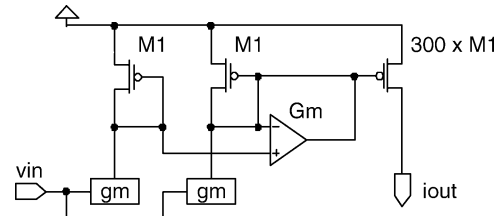


Fig. 17. Transconductance amplifier.

1.2 at 1900 MHz. The fast operational amplifier with the use of an external resistor ($110\ \text{k}\Omega$ in Fig. 14) sets the envelope amplification. An offset can be added to take into account the knee voltage V_{knee} . The minimum supply voltage of the PA can be set externally. The remaining part of the design aims at minimizing the propagation delay to achieve a high switching frequency operation. The fast comparator, whose schematic is shown in Fig. 16, has a propagation delay of 1.2 ns, a dc gain of 80 dB, and a current consumption of $700\ \mu\text{A}$. An anti-overlap circuit avoids output-stage high transient shoot-through currents. The anti-overlap protection delay is 0.5 ns while the rise time on the gates of the output stage is about 1.6 ns. The output stage transistor sizes are $6000 \times 0.35\ \mu\text{m}^2$ for the NMOS and $10000 \times$ for the PMOS. These sizes give approximately equal resistive and capacitive losses for 100 mA and 20-MHz current switching. The overall resulting propagation delay from differential amplifier to output is in the order of 4 ns. The TA, whose half circuit principle is shown in Fig. 17, is based on a large ratio current mirror providing up to 20 mA of output current. The current-mirror buffer extends the frequency

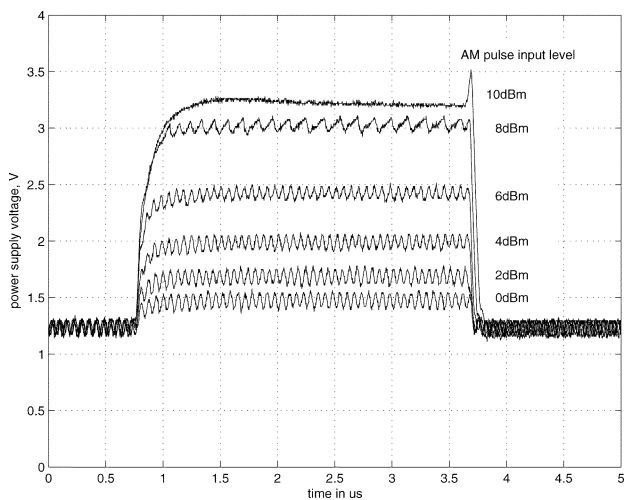


Fig. 18. Pulsed AM voltage supply response.

response. The efficiency of the modulator including the switch and the inductor losses is equal to 85% at an output voltage of 1.25 V and 95 mA of load current. Five wire bonds are used for each output MOS transistor source and chip-on-board assembly has been used to minimize supply bounce. Due to the relatively small amplitude of the RF signal, the envelope detector and the envelope amplifier have a dedicated power supply pin and a differential architecture to better reject the power supply variations.

VI. EXPERIMENTAL MEASUREMENT RESULTS

All the following measurement results have been performed with the modulator IC driving the commercial PA. The minimum and maximum supply voltages are, respectively, 1.25 and 3.3 V. The measurements are compared to the constant 3.3-V supply PA. The center frequency is 1900 MHz and the input passive coupler has 12-dB coupling factor.

A. Modulator Step Response

The measurement of Fig. 18 represents the modulator voltage response to the pulsed AM with different input levels. The rise time is smaller than 200 ns and presents some dependence on the input level due to the dynamic nature of the PA load. The typical ripple is 180 mVpp and the switching frequency is 16 MHz.

B. Spurious Due to the Switching Supply Output Ripple

Due to the power gain collector voltage dependence, the output ripple mixes with the RF signal generating output spurious. To reduce the spurious, it is desirable to have a low ripple. Fig. 19 shows spurious 55 dB lower than the fundamental for an IS-95 CDMA input signal of 5 dBm.

C. Two-Tone Linearity Test

The measurement of Fig. 20 is the linearity two-tone test which has a peak-to-average power of 3 dB. The intermodulation distortion (IMD) of third order is plotted as a function of the average output power and the tone spacing. Due to the extended linear gain characteristic of the dynamic supply PA,

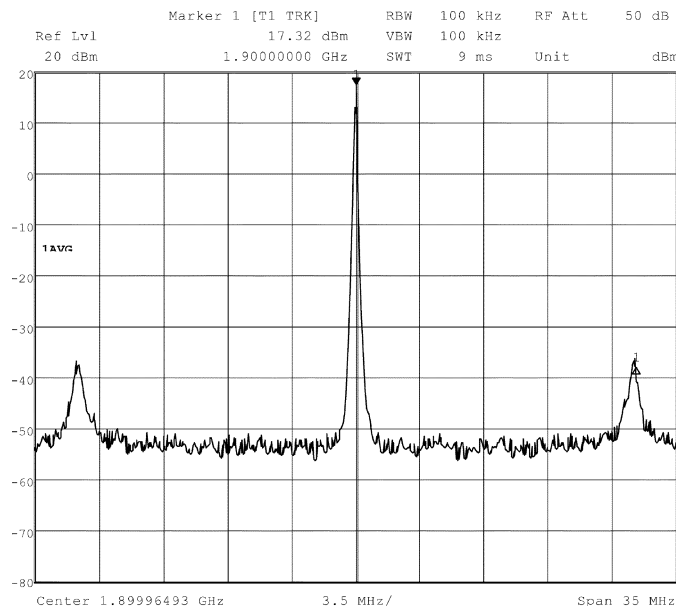


Fig. 19. Spurious due to the switching supply output ripple.

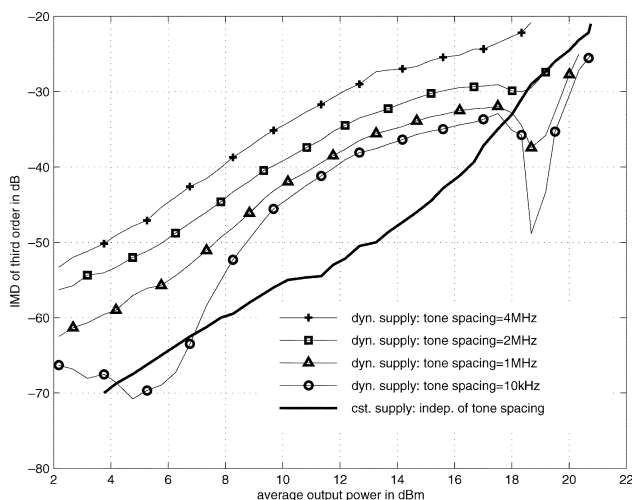


Fig. 20. Measured two-tone linearity test.

IMD is lower at high output power levels and low tone frequency spacing. At low output power levels, the supply voltage is constant and minimum. Therefore, the 1-dB power compression point is lower and the dynamic supply PA generates higher IMD. The IMD dependence on tone spacing becomes significant from 2 MHz because of the modulator phase and amplitude response limitations.

D. IS-95 CDMA Measurement

This section concerns linearity and efficiency measurements achieved with the IS-95 CDMA standard. This standard is well adapted to the performance of the modulator. The peak-to-average power is about 5.5 dB and the modulation bandwidth is 1.23 MHz.

1) ACLR Measurement: The adjacent channel leakage ratio (ACLR) of the constant and varying supply PA are given in Fig. 21 as a function of the main channel output power. Like the two-tone test, the ACLR is a measure of the PA linearity and

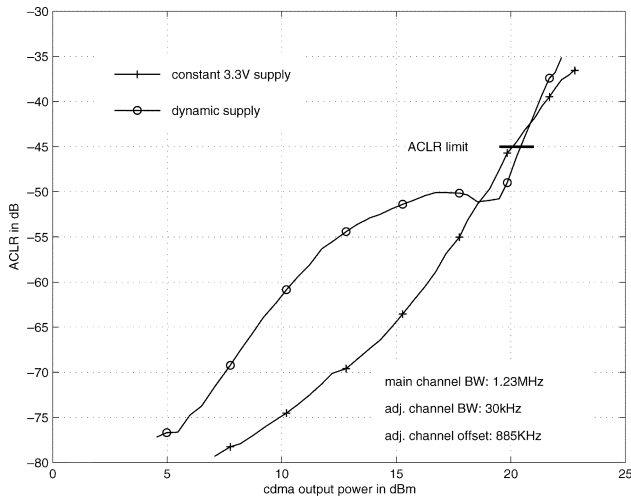


Fig. 21. IS-95 ACLR versus main channel output power.

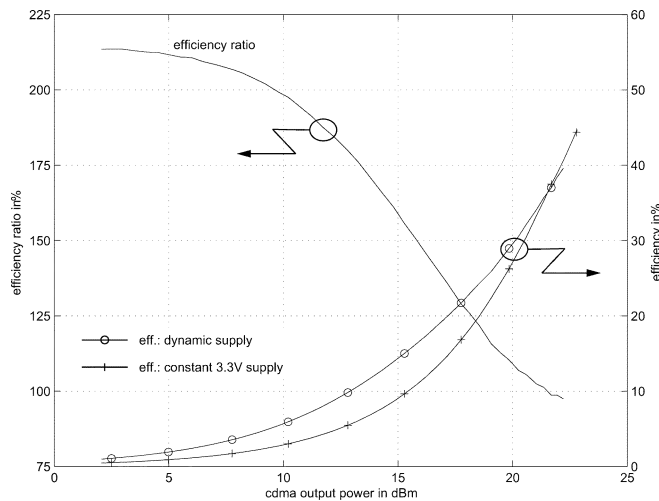


Fig. 22. IS-95 efficiency and efficiency ratio versus CDMA main channel output power.

the result obtained in Fig. 21 presents some similarity with the 1-MHz tone spacing curve of Fig. 20. At the IS-95 ACLR limit of -45 dB, the varying supply PA linearity is higher than its constant supply counterpart. This can be related to the extended linear range (higher 1-dB compression point) of the dynamic adaptation in Fig. 5.

2) *Power-Efficiency Measurement*: In Fig. 22, the power efficiency and the efficiency ratio are plotted versus CDMA main channel output power. Within the linear range defined by the ACLR limit of -45 dB, the efficiency of the dynamic supply PA is improved up to 210%.

3) *Error Vector Magnitude Measurement*: In Fig. 23, rms and peak error vector magnitude (EVM) of the dynamic supply and the constant PA are plotted versus CDMA main channel output power. As the EVM is also a linearity measurement, the aspect of both plots presents similarities with the ACLR linearity measurement of Fig. 21.

VII. RF SIMULATION OF THE DYNAMIC SUPPLY PA

The simulation of the dynamic supply PA aims mainly at predicting the intermodulation distortion for envelope varying

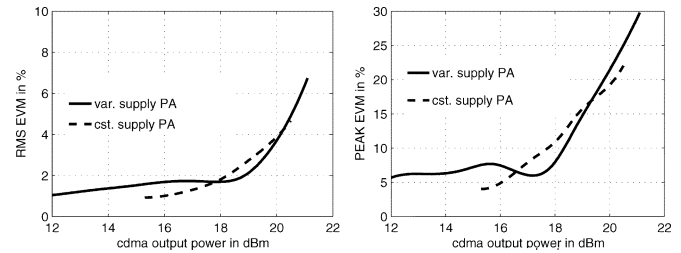


Fig. 23. IS-95 rms and peak EVM measurement versus CDMA main channel output power.

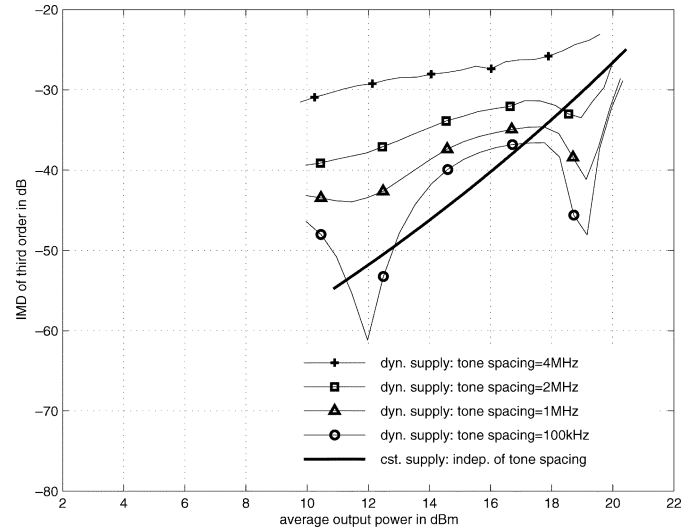


Fig. 24. Simulated two-tone linearity test.

signals. It is not an obvious issue. The PA working at the highest frequency determines the minimum time step for a transient analysis, assuming its large-signal model exists. Hence, covering few periods of the low-frequency modulation signal requires very long simulation time. The dynamic supply PA system, with regard to the switching modulator, is a too nonlinear process to allow the convergence of an harmonic balance or an envelope simulation.

The proposed simulation method consists of two stages. In the first stage, a transient analysis is ran with a behavioral model of the modulator and the model of the PA as load (Fig. 9). The signal of interest is the PA supply voltage V_s . In the second stage, the model used is an interpolation based on the measured PA AM-AM and AM-PM characteristics. Then an envelope simulation is performed with this model to extract the intermodulation distortion and shown in Fig. 24. The first and second simulation stages can be found in Appendix B.

Fig. 24 has the same axis than Fig. 20, which allows direct comparison. The simulation output power range has been limited from 10 to 20 dBm to decrease the simulation time. The general aspect of the simulated IMD is close to the measurement except for a tone spacing of 100 kHz where a minimum occurs at higher output power level. The simulated IMD is 2 dB better, which is an optimistic prediction with respect to the measurement. The reason of this difference is not obvious, but using a measurement-based model for the PA implies some inaccuracy. With the mirrored PA configuration used, the quasi-static measurement (see Fig. 29) is only valid up to about 10 kHz.

From this frequency, thermal feedback cancels (see Fig. 28) and the collector current experiences less modulation. This does not strongly affect the small-signal power gain [(3)] but it can increase the compression of both AM-AM and AM-PM characteristics. Also, the transient analysis of the first simulation stage can give slight supply voltage V_s differences.

VIII. CONCLUSION

Design and system aspects of a 0.35- μm CMOS fast modulator IC for dynamic supply linear RF PA are presented. The modulator integrates all the required functions to efficiently convert a low-level varying RF envelope to a fast high-level varying supply for an external RF power transistor. The modulator is designed to achieve bandwidth in the order of 2 MHz. With respect to the constant supply PA, measurements on the dynamic supply PA (the modulator IC driving the external PA) shows increased efficiency with, in some cases, linearity improvement. Higher efficiency improvement can be obtained with a reduced conduction angle PA increasing efficiency to the detriment of linearity and modulator slew-rate limitation. To further improve efficiency without compromising the linearity, the envelope tracking technique applied to the base bias along with dynamic supply on the collector of the BJT can be used.

A linearized baseband model for the external PA as load for the modulator is developed. It takes into account thermal effects and allows to simulate the modulator with its load without having to consider the RF behavior of the PA.

A two-stages simulation procedure to simulate the dynamic supply PA linearity is presented. It allows to predict the level of IMD with an error of about 2 dB.

APPENDIX A

THERMAL MESHING OF THE PA DIE

This Appendix presents a method to determine the transfer functions $\Delta T_{j1}/\Delta P$ and $\Delta T_{j2}/\Delta P$. Referring to Fig. 6, ΔP is the variation of the dissipated power in Q2, ΔT_{j2} is the junction temperature variation of Q2, and ΔT_{j1} is the junction temperature variation of Q1.

A 3-D meshing of the current-mirror PA die with the dissipated power stimulus is shown in Fig. 25. Each elementary volume of the meshing has variable dimensions Δx , Δy , and Δz . The corresponding electrothermal model parameters R_x , R_y , and R_z of Fig. 26 are functions of these dimensions. The RF device is made of 14 transistors and the mirror device of a single transistor. The current-mirror ratio is $n = 14$. Fig. 25 shows the location of the vertical transistor emitters. Electrical energy is converted in thermal energy in the collector-base depletion layer near the die surface. It is assumed here that the power stimuli are injected on the die surface on five equally distributed points of each emitter of Q2. The sum of the 14×5 ac current sources is normalized to 1-A stimulus corresponding to a dissipated power of 1 W. Referring to Fig. 25, the junction temperature variations of Q2 and Q1 are given by (19):

$$\Delta T_{j1} = \frac{1}{5} \sum_{y=1}^5 \Delta T_{0y}$$

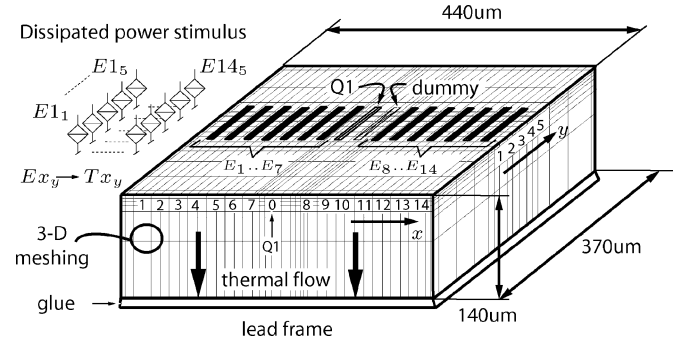
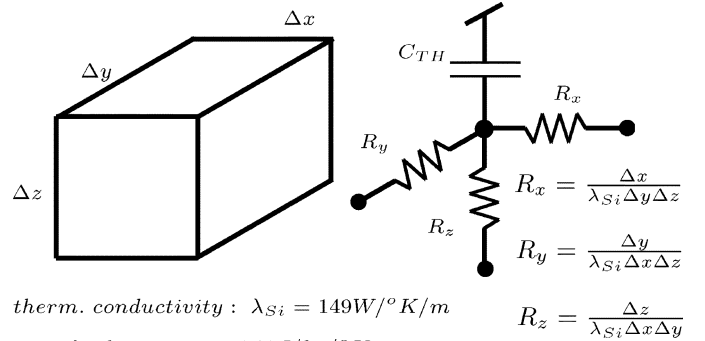


Fig. 25. Dissipated power stimulus and die dimensions with 3-D thermal meshing of the commercial RF BJT mirror.



therm. conductivity : $\lambda_{Si} = 149 \text{ W/}^\circ\text{K/m}$

specific heat : $c_{Si} = 760 \text{ J/kg/}^\circ\text{K}$

density : $\rho_{Si} = 2.33 \text{ kg/m}^3$

$C_{TH} = c_{Si} \rho_{Si} \Delta x \Delta y \Delta z$

Fig. 26. Meshing cell and equivalent electrothermal model.

$$\Delta T_{j2} = \frac{1}{14 \times 5} \sum_{x=1}^{14} \sum_{y=1}^5 \Delta T_{xy}. \quad (19)$$

The die is stuck on the emitter lead frame, which provides a low thermal path to the PCB, considered here as a heatsink for the thermal study. The thermal influence of the plastic package is neglected because the thermal conductivity of plastic is much lower than that of silicon.

The meshing of Fig. 25 generates about 4000 cells, each cell containing the model of Fig. 26. The automatically generated netlist counts up more than 16 000 resistances and capacitances. After an ac SPICE type of analysis is run, an automatic routine is required to display the temperature distribution at the die surface (Fig. 27). The meshing is a tradeoff between precision obtained in Fig. 27 and the simulation time. Fig. 27 shows that the mirror device temperature variation ΔT_{j1} is not identical to that of the RF device ΔT_{j2} . Because of the high thermal conductivity of the silicon, x and y temperature gradients are high and the thermal coupling of the emitters is weak. Fig. 28 represents the frequency response of the junction temperature difference ΔT_j and the thermal impedance seen from the junction to the solder point of Q2 (Z_{THQ2}). The variation of the junction temperature difference, normalized to a dissipated power in Q2 of 1 W, is about 17°C and remains constant up to 10 kHz. The thermal impedance of Q2 is the image of the junction temperature variation ΔT_{j2} . Hence, at a frequency of 10 kHz, the junction temperature variation of Q1 drops to zero ($\Delta T_{j1} = Z_{THQ2} \cdot \Delta P - \Delta T_j$). Thus, negative thermal feedback provided by Q1 works only up to 10 kHz.

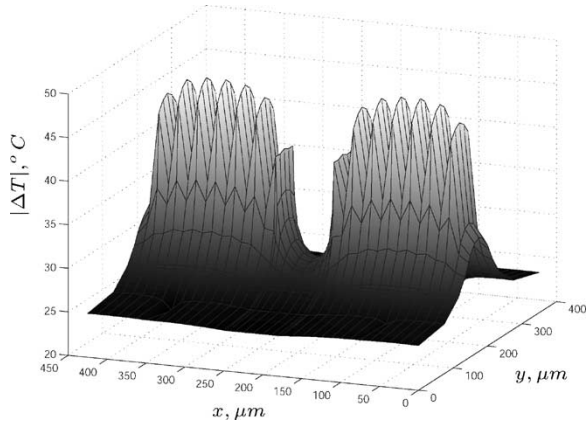


Fig. 27. Distribution of the die surface temperature variation normalized to 1 W. Power stimulus frequency is 1 Hz.

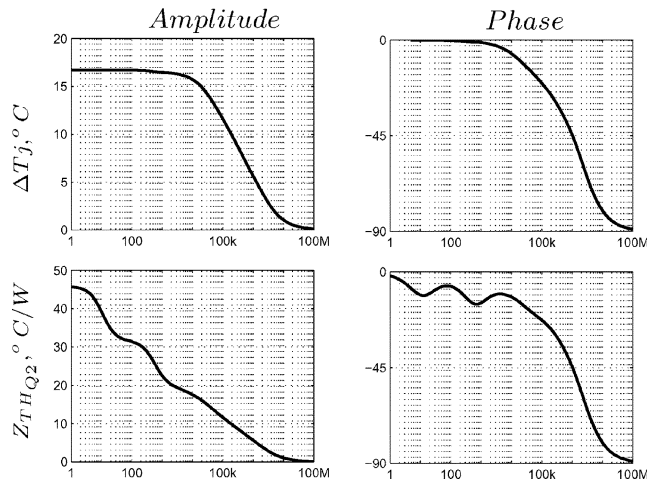


Fig. 28. Frequency response of junction temperature difference and thermal impedance of Q2. Stimulus power is normalized to 1 W.

The transfer functions $\Delta T_{j1}/\Delta P$ and $\Delta T_{j2}/\Delta P$ are fitted to an expression of the form

$$\frac{\Delta T_{j1,2}}{\Delta P} = K \frac{\left(1 + \frac{j\omega}{\omega_{z1}}\right) \dots \left(1 + \frac{j\omega}{\omega_{znz}}\right)}{\left(1 + \frac{j\omega}{\omega_{p1}}\right) \dots \left(1 + \frac{j\omega}{\omega_{pnp}}\right)}$$

APPENDIX B SIMULATION OF IM DISTORTION

A. First Simulation Stage

The stimulus used is the two tone linearity test signal whose envelope is a rectified sine wave. The input envelope level is swept for a corresponding input power ranging from -2 to 8.5 dBm. The frequency of the envelope is set for tone spacings of 100 kHz, 1 MHz, 2 MHz, and 4 MHz to compare with measurement made in Fig. 20. A low tone spacing frequency of 100 kHz is preferred to 10 kHz to reduce the simulation time. Nevertheless, both frequency tone spacings are well within the bandwidth of the modulator, and distortion is comparable.

The model used for the transient analysis mixes transistor level and behavioral blocks to decrease simulation time. The

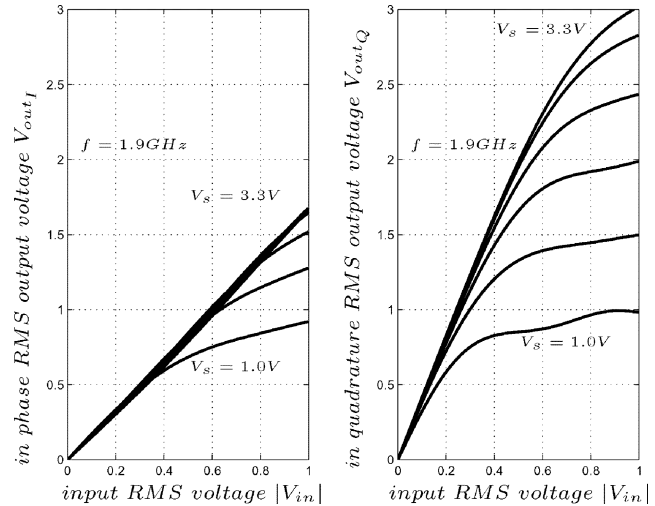


Fig. 29. Cartesian representation of the PA AM-AM and AM-PM characteristic versus rms input voltage V_{in} and supply voltage $V_s = 1.0, 1.5, 2.0, 2.5, 3.0,$ and 3.3 V.

input coupler is treated as a constant attenuation and the envelope detector is based on a polynomial approximation of the measured detected signal versus envelope level. The analog processing block, the fast comparator, and the transconductance amplifier are all transistor-based blocks. This allows to use the same prototype settings (minimum PA supply voltage, envelope gain G_{env} , and knee voltage offset) for the model. The comparator drives the output stage which is an ideal voltage-controlled voltage source with an output resistance of $R_{on} = 0.3 \Omega$. A small-signal inductor model is used because the maximum current of the prototype inductor is never reached.

The transient analysis is done over five periods of the modulating signal. The simulation result V_s is used in the second simulation stage.

B. Second Simulation Stage

The PA model is based on the measured PA AM-AM and AM-PM characteristics. The cartesian representation of these characteristics are shown in Fig. 29 for various supply voltage V_s . In phase and in quadrature output voltage can be approximated with a polynomial fit [3] given by (20) and (21):

$$V_{outI}(|V_{in}|) = a_1 \cdot |V_{in}| + a_3 \cdot |V_{in}|^3 + \dots + a_{11} \cdot |V_{in}|^{11} \quad (20)$$

$$V_{outQ}(|V_{in}|) = b_1 \cdot |V_{in}| + b_3 \cdot |V_{in}|^3 + \dots + b_{11} \cdot |V_{in}|^{11}. \quad (21)$$

A polynomial fit is made for each value of V_s ($1.0, 1.5, 2.0, 2.5, 3.0,$ and 3.3 V) with regard to the input envelope voltage $|V_{in}|$. For each measurement voltage V_s , there is a set of polynomial coefficients a_1, a_3, \dots, a_{11} and b_1, b_3, \dots, b_{11} . To make the polynomial-based model continuously dependent on V_s , each coefficient a_n and b_n ($n = 1, 3, \dots, 11$) can also be fitted with regard to V_s :

$$\begin{aligned} a_n(V_s) &= a_{n0} + a_{n1} \cdot V_s + a_{n2} \cdot V_s^2 + \dots + a_{n5} \cdot V_s^5 \\ b_n(V_s) &= b_{n0} + b_{n1} \cdot V_s + b_{n2} \cdot V_s^2 + \dots + b_{n5} \cdot V_s^5 \\ n &= 1, 3, 5, \dots, 11. \end{aligned} \quad (22)$$

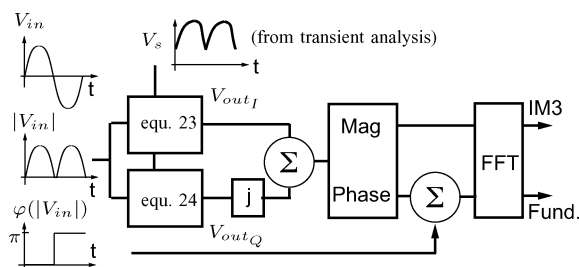


Fig. 30. Equivalent PA schematic for envelope simulation.

The general expressions for (20) and (21) become, respectively, (23) and (24):

$$V_{out_I}(|V_{in}|, V_s) = \sum_{n=1, \text{ odd}}^{11} a_n(V_s) \cdot |V_{in}|^n \quad (23)$$

$$V_{out_Q}(|V_{in}|, V_s) = \sum_{n=1, \text{ odd}}^{11} b_n(V_s) \cdot |V_{in}|^n. \quad (24)$$

The equivalent PA schematic is described in Fig. 30.

The double tone modulating signal is a sine wave and the envelope is its rectified replica. The envelope phase is either 0 or π to reconstruct the original modulating signal.

The output envelope is the sum of the in-phase and in-quadrature signals, both depending on $|V_{in}|$ and V_s . The fast Fourier transform on the reconstructed output modulating signal gives the intermodulation and fundamental tones from which the IMD is found and shown in Fig. 24.

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