A fast modulator for dynamic supply linear RF power amplifier

Nicolas Schlumpf
Electronics Laboratories
Swiss Federal Institute of Technology, Lausanne
nicolas.schlumpf@epfl.ch

Michel Declercq
Electronics Laboratories
Swiss Federal Institute of Technology, Lausanne
michel.declercq@epfl.ch

Catherine Dehollain
Electronics Laboratories
Swiss Federal Institute of Technology, Lausanne
catherine.dehollain@epfl.ch

Abstract

A fast modulator for dynamic supply linear RF amplifier has been integrated in a 0.35um CMOS technology. The use of this modulator with an external linear Power Amplifier (PA) allows to maintain its efficiency at a higher level than it would with the same PA supplied at constant voltage.

The modulator is designed to track rapid envelope variations at high efficiency without compromising the RF PA linearity.

1. Introduction

Conventional RF power amplifiers usually give their maximum efficiency near the maximum output power level. When the output power decreases, the efficiency drops sharply. Deep class AB or B PAs improve their efficiency by a self-adaptation of the current drawn from the power supply. However, in many cases, both deep class AB and B do not provide enough linearity like, for instance, in CDMA applications where spectral re-growth is of first concern. From class A to class B, RF PAs face the linearity-efficiency trade-off. The class A is linear but power inefficient, whereas class B is efficient but has a poor linearity.

An alternative to the linearity-efficiency trade-off is to dynamically adapt the power supply voltage of a linear PA. The linear PA is of class A or of moderate class AB and its collector or drain voltage is adapted to avoid RF output voltage to saturate. This same principle has been called dynamic power supply in [1], bias adaptation in [2], and envelope tracking in [3].

2. Principle of dynamic supply RF PA

The detailed block diagram (Fig.1) shows a linear RF PA

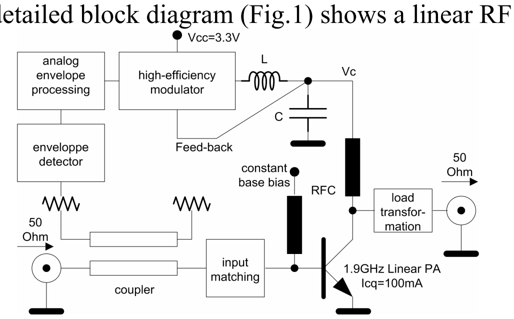

Fig. 1: detailed block diagram

with its input and output matching, a directional coupler, an envelope detector to measure the coupled incident power, an analogue envelope processing block and a high efficiency modulator. The modulator is a fast high-efficiency step down converter transforming the main 3.3V supply into a varying voltage for the PA. To implement the dynamic supply principle, a moderate class AB PA based on a commercial BJT has been realized and measured. As shown in fig. 2, increasing the collector voltage (*Vc*) of the PA improves the 1dB-compression point. Normally, the collector voltage can be decreased down to the knee voltage but gain reduction due to Miller capacitance limits the minimum voltage to approximately 1 Volt. The modulator efficiency times the maximum-to-minimum *Vc* ratio determines the best efficiency improvement.

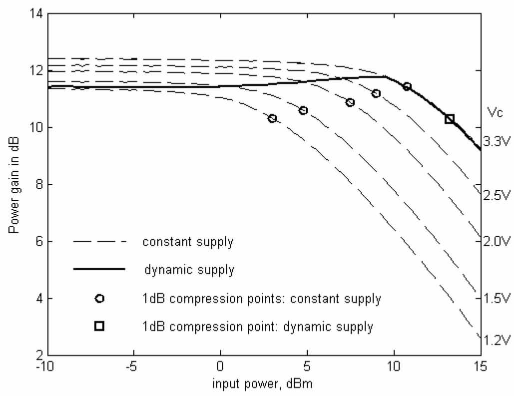

Fig.2: 1900MHz CW power gain vs. input power vs. Voltage supply Vc

Thus, the voltage supply varies, according to the input envelope, to keep the power gain constant over the widest input power range.

Considering the 1dB-compression point as a measure of linearity, the variable voltage supply PA has even a wider linear characteristic than the constant 3.3V supply voltage PA.

Fig. 2 illustrates a Continuous Wave (CW) measurement where the input power is swept from -10dBm to +15dBm with a long sweep time. In the case of rapid modulation, the envelope can vary quickly over a wide range. For the CW test of fig.2, this corresponds to a short sweep time.

In such a case, and with a variable supply, the gain response should remain unchanged. If the sweep time is reduced, several imperfections cause the gain response to deviate from the ideal response of fig.2. Two factors bring about these imperfections:

1) The transistor has large power variation and is self-heating sensitive. Temperature variations turn into variations of bias point because of the base-emitter temperature-to-voltage dependency. This is known as bias modulation [2].
2) The imperfect amplitude and phase response of the modulator introduces a gain error and a compression of the RF output signal.

A mirrored PA configuration (fig. 3) having a low thermal resistance corrects the first imperfection.

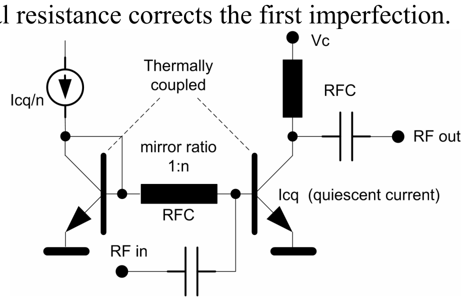

Fig. 3: mirrored PA configuration

A fast modulator design reduces the second imperfection. Although the dynamic supply PA principle does not require *Vc* to replicate exactly the envelope, the delay and the large amplitude errors, due to modulator speed limitations, have an impact on the RF distortion.

3. Modulator design

The main concerns in the modulator design are speed and efficiency, the accuracy being less important.
Unlike conventional PWM DC-DC converters, the sliding mode modulator depicted in fig. 4 does not have a slow feedback path.

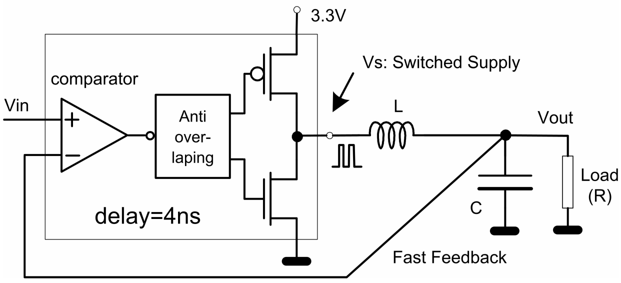

Fig.4: sliding mode modulator with synchronous switch

The output replicates the input with the filtered switched supply superimposed. The output can swing up to the supply voltage rails because the pulse width is not limited to a maximum or minimum value. Considering the load is constant, the input-to-output transfer function is given by that of the LC filter. The switching frequency *fs* can be predicted with the set of equations 1,2 and 3 assuming a 50% switched supply duty cycle and thinking about the modulator as an oscillator. The oscillation condition (equ.1) parameters are the overall modulator delay of 4ns, the filter damping factor δ and the LC filter natural frequency *fn*. The damping factor is chosen equal to 0.7 for a flat frequency response. In this case, *fn* and the -3dB cut-off frequency are the same. To get a low output ripple, *fs* must be much larger than *fn*. Thus, equ.1 expresses a trade-off between the cut-off frequency and the output ripple. A short modulator delay allows to achieve the best trade-off, i.e. maximizing the cut-off frequency while keeping the output ripple low.

$$fs \cdot delay \cdot 2 \cdot \pi + \tan^{-1}\left(\frac{2 \cdot \delta \cdot \frac{fs}{fn}}{1-\left(\frac{fs}{fn}\right)^2}\right) == \pi \qquad \text{(equ. 1)}$$

$$\delta = \frac{1}{2} \cdot \sqrt{\frac{L}{C}} \cdot \frac{1}{R} \cong 0.7 \quad \text{(equ. 2)} \quad \text{and} \quad fn = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \quad \text{(equ. 3)}$$

So far, the load has been considered constant. However, the impedance seen from the supply pin *Vc* of a PA at RF envelope frequencies can be simplified to the circuit of fig.5.

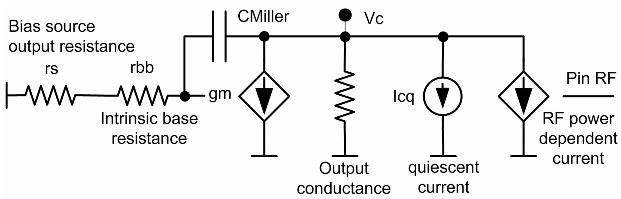

Fig. 5: simplified equivalent load of the PA

The impedance seen from *Vc* is dominated by the output conductance of the RF transistor at DC.
When the frequency increases, the active impedance, made of the Miller capacitance, the base resistance and the transconductance *gm,* tends to shunt the output conductance.
Furthermore, the impedance seen from *Vc* is dynamic. For a BJT, the exponential law of the transistor under CW RF signal (equ. 4) produces a DC collector current (equ. 6) proportional to the square of the RF input voltage level.

$$Ic \cong Is \cdot \exp\left(\frac{vbe_o + vin_{RF} \cdot \sin(\omega_{RF} \cdot t)}{Ut}\right) = Icq \cdot \exp(A \cdot \sin(\omega_{RF} \cdot t)) \quad \text{(equ. 4)}$$

$$\text{with} \quad A = \frac{vin_{RF}}{Ut} \quad \text{(equ. 5)}$$

$$Ic_{dc} = Icq \cdot \left(1 + \frac{A^2}{4} + \ldots\right) \quad \text{(equ. 6)} \qquad \Delta I \approx Icq \cdot \frac{A^2}{4} \quad \text{(equ. 7)}$$

For a moderate class AB or class A PA, the DC current increases significantly when the RF output compression is reached. When the envelope varies quickly during ΔT and reaches the compression, the inductor has to supply the load current demand ΔI. The inductor current change is limited by equ.8.

$$\frac{\Delta I}{\Delta T} \leq \frac{Vs - Vout}{L} \qquad \text{(equ. 8)}$$

Moreover, when the compression is reached, the switched supply *Vs* sticks to the upper rail and the output voltage *Vout* rises to the upper rail. Thus, the voltage across the inductor is small. If the inductor value is too large, ΔI can not be supplied during ΔT. As a consequence, the output voltage is slew rate limited.

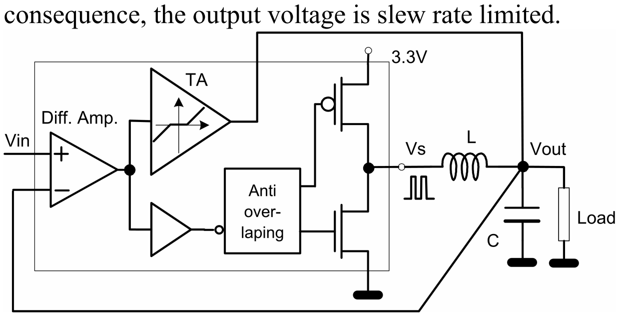

Fig.6: sliding mode modulator with TA

To avoid slew rate and its associated PA distortion, the sliding mode modulator of fig. 4 is modified, according to fig.6, to include a transconductance amplifier (TA). The TA supplies the required ΔI when the input error is greater than the expected output ripple.

4. Circuit design

The circuit functionality shown in fig.7 consists of a broad-band envelope detector with an on chip 50Ω termination, a fast operational amplifier with 100MHz unity gain bandwidth, a differential amplifier, a fast differential comparator, an output stage with *Ron* of 0.3Ω and a TA.

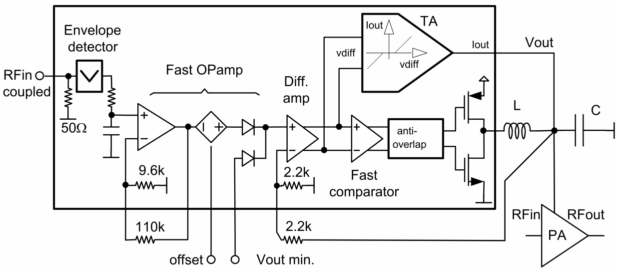

Fig.7: integrated circuit schematic

The envelope detector has a sensitivity of -10dBm and the on chip termination has a measured VSWR of 1.2 at 1900MHz. The fast operational amplifier with the use of an external resistor (110kΩ in fig. 7) sets the envelope amplification and an offset can be added to obtain the PA variable gain response (fig. 2). The minimum supply voltage of the PA can be set externally.

The remaining part of the design aims at minimizing the propagation delay to achieve a high switching frequency operation. The fast comparator, whose schematic is shown in fig. 8, has a propagation delay of 1.2ns, a DC gain of 80dB and a current consumption of 700uA. An anti-overlap circuit avoids output stage high transient shoot-through currents. The anti-overlap protection delay is 0.5ns while the rise time on the gates of the output stage is about 1.6ns. The output stage transistor sizes are 6′000x0.35um^2 for the NMOS and 10′000x0.35um^2 for the PMOS. These sizes give approximately equal resistive and capacitive losses for 100mA and 20MHz current switching.

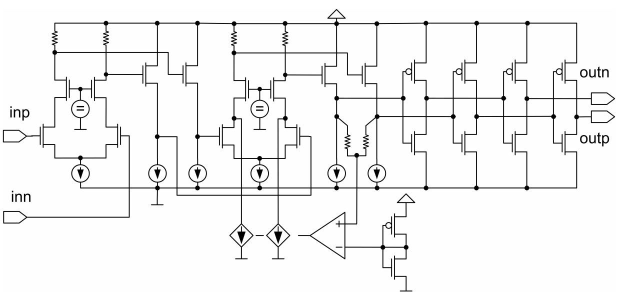

Fig.8: differential comparator schematic

The overall resulting propagation delay from differential amplifier to output is in the order of 4ns.

The TA, whose half circuit principle is shown on fig. 9, is based on a large ratio current mirror providing up to 20mA output current. To extend the frequency response, the current mirror is buffered.

The efficiency of the modulator including the switch and the inductor losses is 85% at an output voltage of 1.25V and 95mA load current.

Five wire bonds are used for each MOS output transistor source and chip on board assembly has been used to minimize supply bounce. Due to the relative small amplitude of the RF signal, the envelope detector and the envelope amplifier have a dedicated power supply pin and a differential architecture to better reject the power supply variations.

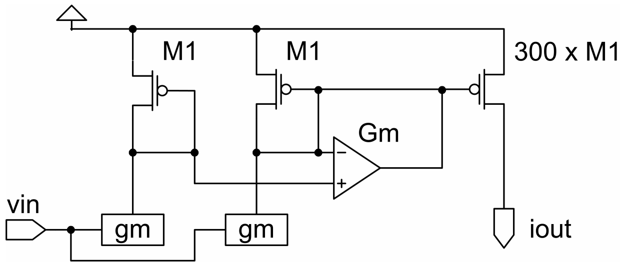

Fig.9: transconductance amplifier

5. Experimental results

All the following measurement results have been performed with the system described previously at a center frequency of 1900MHz.

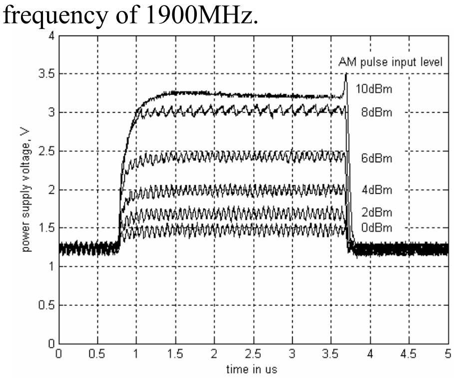

Fig.10: pulsed AM voltage supply response

First measurement (fig. 10) represents the modulator voltage response to the pulsed AM with different input levels. The rise time is smaller than 200ns and has some dependency with the input level due to the dynamic nature of the PA load. The typical ripple is 180mVpp and the switching frequency is 16MHz. Due to the power gain collector voltage dependency, the output ripple mixes with the RF signal generating output spurious. To reduce the spurious, it is desirable to have a low ripple.

The second measurement (fig. 11) is the linearity two-tone test which has a peak-to-average power of 3dB.

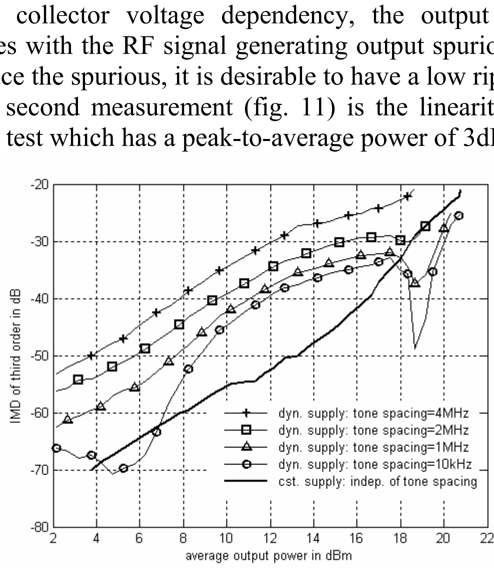

Fig.11: two tones linearity test

The intermodulation distortion (IMD) of third order is traced as a function of the average output power and the tone spacing. Due to the extended linear gain characteristic of the dynamic supply PA, IMD is lower at high output power levels and low tone frequency spacing. At low output power levels, the dynamic supply PA generates higher IMD. The IMD dependence on tone spacing becomes significant from 2MHz because of the modulator phase and amplitude response limitations.
The third measurement compares the adjacent channel leakage ratio (ACLR) of the fixed and dynamic supply PA for the IS-95 and 3GPP CDMA modulation standards. The IS-95 and 3GPP modulation standards produce an envelope bandwidth of 1.23MHz respectively 3.84MHz and a peak-to-average power ratio of 4.8dB respectively 5.8dB. Figures 12 and 14 show the ACLR for the IS-95 and the 3GPP modulation standards. Because of the lower envelope bandwidth, the dynamic supply PA gives better ACLR with the IS-95 standard. The 3GPP envelope bandwidth is larger than the 3MHz modulator LC cut-off frequency. In figures 13 and 15, the power efficiency and the efficiency ratio as a function of the average output power are traced. The efficiency of the dynamic supply PA is well improved in its linear range and the maximum efficiency ratio is greater than 210%.

6. Conclusions

A fast modulator for dynamic supply linear RF PA is presented. The modulator integrates all the required functions to efficiently convert a low-level varying RF envelope to a high-level supply for an external RF power transistor.
The linearity of the dynamic supply PA supplied by the modulator is a function of the input power and of the envelope bandwidth. Thanks to the fast modulator design, the linearity dependence on the envelope bandwidth remains controlled up to 2MHz. Within the linear range of the dynamic supply PA, the efficiency is greater than its constant supply counter part.

7. Acknowledgement

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8. References

[1] Gary Hanington et al., “High efficiency Power amplifier Using Dynamic Power Supply Voltage for CDMA Applications”, IEEE Transactions on microwave theory and techniques, vol. 47, n°8, pp. 1471-1476, august 1999

[2] Steve C. Cripps, “RF Power Amplifiers for Wireless Communications”, Artech House 1999

[3] Peter B. Kenington,”High-Linearity RF Amplifier Design”, Artech House 2000

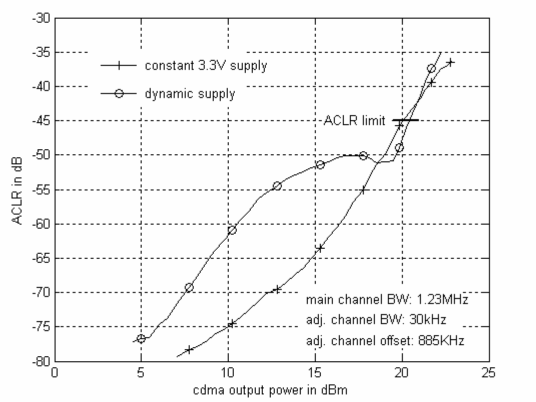

Fig.12: IS-95 ACLR

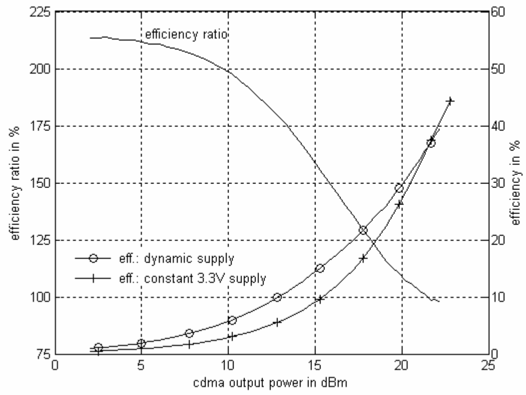

Fig.13: IS-95 power efficiency comparison

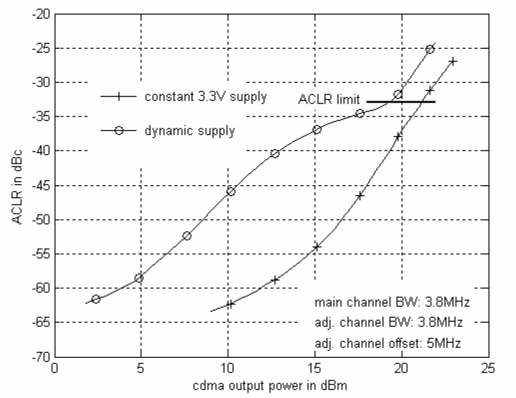

Fig.14: 3GPP ACLR

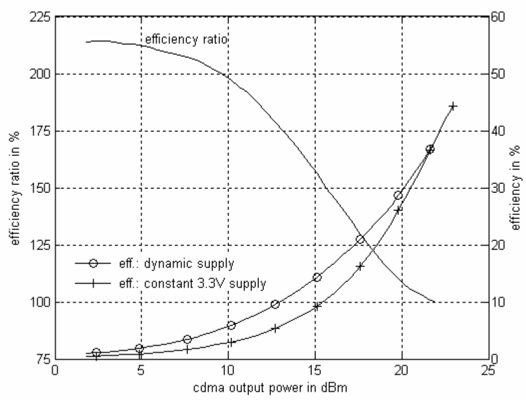

Fig.15: 3GPP power efficiency comparison