A FULLY DIFFERENTIAL CMOS INTEGRATED 4th ORDER RECONFIGURABLE GM-C LOWPASS FILTER FOR MOBILE COMMUNICATION

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ABSTRACT

A fully re-configurable channel select filter is presented which is used as a part of a multi mode direct conversion receiver. The filter supports different modes including GSM, IS-95, and UMTS. A 4^{th} order Butterworth filter is realized in a g_mC filter topology. The filter circuit is implemented in a standard 0.35 μm CMOS process. The filter is able to handle large input signals up to 600mVpp at a supply voltage of 2.7V. The circuit has a low current consumption of 620μA, whereas the needed die size is only 530×520 μm.

1. INTRODUCTION

During the last decades more and more wireless standards have been introduced. For 2G wireless cellular systems several standards are used depending on the geographic region, like the Personal Digital Cellphone (PDC), the European Global System for Mobile Communications (GSM) or the American North American Digital Cellular (IS-95). The next generation of mobile communication (3G) will use wide-band CDMA signals. Furthermore new standards will be introduced in the future , like the UMTS HSDPA (High Speed Downlink Packet Access), which is the extension of UMTS towards 10 Mbits/s [1].

In order to receive many standards with the same mobile terminal, the RF frontend needs to have re-configurable building blocks. Since direct conversion receivers (DCR) require only lowpass filtering in the analogue basband, this architectures has been applied for the multi mode transceiver (Fig. 1)[2]. Low-pass filters are an essential part of the analogue baseband circuit of modern communication receivers, because of the ability to re-configure the bandwidth, gain, or linearity in order to fulfil the requirements of different standards.

The presented re-configurable low pass filter is part of a DCR which is able to receive 2G (GSM) and 3G standards with the same receive path. The filters are placed between the mixer output and ADC input. The specifications and characteristic of the filters are mainly determined by the need to suppress interference and blocking signals that will be discussed in section 3.

In section 4 the used filter topology and the implementation of the circuit in a standard 0.35 μm CMOS technology is discussed. Also the design flow of the different circuit blocks and the derivation of the filter parameters is presented. Section 5 describes the simulation results for the filter and shows the re-configurability. In section 6 the measurement results are presented. Finally, section 7 gives a conclusion of the presented work.

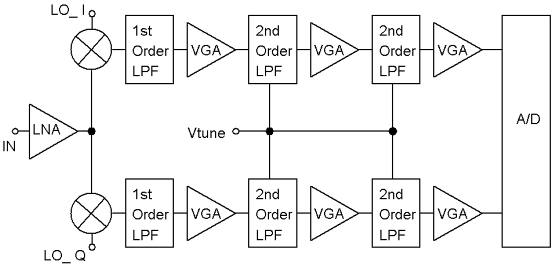

Figure 1: Direct conversion receiver (DCR) block diagram.

2. IMPLEMENTATION OF THE RE-CONFIGURABLE LOWPASS FILTER

2.1. Filter Specification

The filter specifications have been derived to meet the specifications for GSM, IS-95 and WCDMA. Therefore, the corner frequency of the filter has to be tunable from about 200 kHz (GSM) up to 2.5 MHz (WCDMA). In order to meet new and upcoming standards between these limits the filter is tunable by means of an analogue tuning voltage, so that tuning over a wide frequency range is possible. The system specifications indicate the need of a 5^{th} order Butterworth filter to fulfil both demands, for the GSM and WCDMA mode. The characteristic is the output of a system analysis where the adjacent channel rejection requirement and intersymbol interference have been considered. The used Butterworth characteristic has less than < 120 ns of group delay for a corner frequency of 2.5 MHz. The first pole of the filter is already part of the mixer output stage. Hence, for the I and Q path of the receiver a 4^{th} order Butterworth filter has to be implemented, respectively, consisting of two 2^{nd} order filters.

Due to the high blocking and intermodulation requirements of cellular standards, like GSM and UMTS the maximum input signal level is 600mVpp (diff). In the receiver system the remaining 4th order filter is split into two 2nd order filters which are separated by a variable gain amplifier (VGA). The normalized ($\omega_0 = 1$) transfer function of the 4th order Butterworth filter is [3]

$$H(s) = \frac{V_{Out}}{V_{In}} = \frac{A(0)}{\left(s^2 + 1.848s + 1\right)\left(s^2 + .765s + 1\right)} \qquad (1)$$

From the system specification a filter gain of about 0 dB is given. So A(0) is set to 1. With this assumption the transfer functions of the 2nd order filters are:

$$H_1(s) = \frac{1}{\left(s^2 + 1.848s + 1\right)} \qquad (2a)$$

$$H_2(s) = \frac{1}{\left(s^2 + .765s + 1\right)}\,. \qquad (2b)$$

Both transfer functions differ only in the linear term of the denominator polynomial which gives the quality factor of the filter.

The two 2nd order filters can be built up very similar. Only one component has to be modified. Therefore, the design of only one filter will be described in this paper.

2.2. Gm-C Filter Circuit

There are several channel filter topologies which could be implemented, like g_mC, active RC or switch cap architectures. The topologies distinguish from each other in maximum tuning range, input referred noise floor, and dynamic range [4]. For the implementation of the filter the g_mC approach [5] has been chosen because of the easy tuning capability by varying the g_m value of the transconductors. The g_mC filter also has a low noise floor but the ability to handle large signals is limited. In order to archive the required value in terms of linearity the g_m which depends on the width, length and the bias current of the CMOS transistor has to be chosen carefully.

A biquad circuit realization for the 2nd order filter is used because of its advantages in design and layout. As will be shown later similar circuit blocks can be used to implement both transfer functions. All filter stages operate with one common bias generating circuit which improves the matching between the filter stages over the tuning range.

Although it has not been used in this circuit, biquad filters can also amplify the signal, so that it could be used to combine the filter and VGA circuits. A disadvantage of the biquadratic filters compared to the LC-ladder filters is the larger sensitivity to component variations.

2.3. Implementation of the Biquadratic Filter Sections

The topology of the fully differential biquad circuit block is shown in Figure 2.

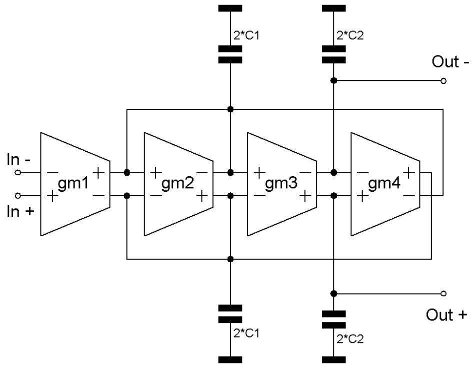

Figure 2: 2nd order Biquad Gm-C low-pass filter circuit.

The transfer function of this biquad is [6]

$$H(s) = \frac{V_{Out}}{V_{In}} = \frac{\dfrac{g_{m1}}{g_{m4}}\,\dfrac{g_{m3}g_{m4}}{C_1C_2}}{s^2 + \dfrac{g_{m2}}{C_1}s + \dfrac{g_{m3}g_{m4}}{C_1C_2}} \qquad (3).$$

Recognizing the common transfer function of a 2nd order low-pass filter as

$$H(s) = \frac{\omega_0^2}{s^2 + \dfrac{\omega_0}{Q}s + \omega_0^2} \qquad (4)$$

one obtains the corner frequency ω_0 and the quality factor Q of the biquad as,

$$\omega_0^2 = \frac{g_{m3}g_{m4}}{C_1C_2} \qquad \frac{\omega_0}{Q} = \frac{g_{m2}}{C_1} \qquad (5)$$

and $g_{m1}=g_{m3}=g_{m4}=g_m$ and $C_1=C_2=C$ leads to,

$$\omega_0 = \frac{g_m}{C} \qquad Q = \frac{g_m}{g_{m2}} \qquad (6).$$

Now the transconductance g_{m2} of the two 2nd order biquads can be calculated with (1) and (3)

$$g_{m2,1} = 1.848 * g_m \text{ (biquad 1) and}$$
$$g_{m2,2} = 0.765 * g_m \text{ (biquad 2)} \qquad (7).$$

Six of the eight OTAs of the 4th order filter are identical, both remaining OTAs can easily be adapted with only changing the OTA current. This clearly shows the simplification of the design that results from reuse of equal cells.

2.4. OTA Circuit

For the OTA circuits a CMOS fully differential folded-cascode OTA [7] has been chosen (Figure 3).

Transistors T2, T6, T7, T9, T8, T10 and T11 act as current sources with current I, while through T4 and T5 a current of 1.5*I flows. The transconductance g_m of the OTA in the linear region of the source coupled pair is

$$g_m = \sqrt{2K' \frac{W}{L} I} \tag{8}$$

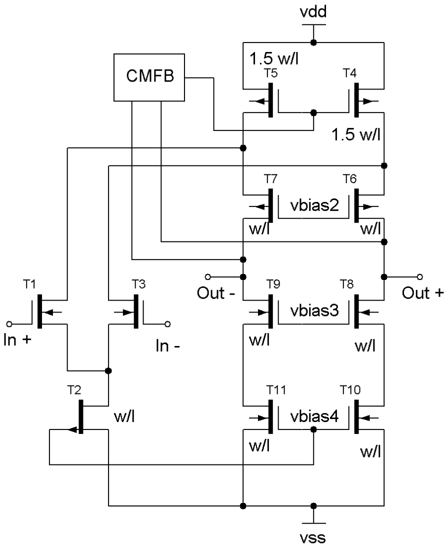

Figure 3: Fully differental folded-cascoded OTA.

and can easily be tuned by changing the current through the OTA. This property of the OTA is used to change the corner frequency of the filter. The ratio of the input transistors was chosen to meet the specification for the input voltage range of 600mVpp (diff).

2.5. CMFB Circuit

Because of the fully differential circuit a common-mode feedback circuit (CMFB) is needed to set the DC output level of the filter. A simple circuit is used that amplifies the common-mode signal while rejecting the differential signal (Figure 4).

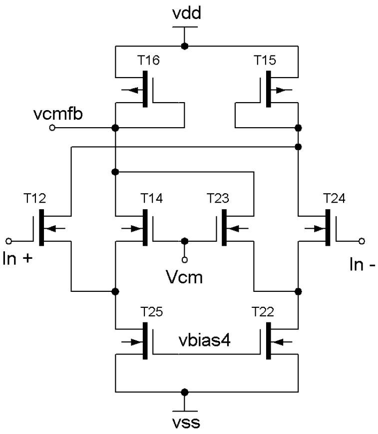

Figure 4: Common-mode feedback circuit.

2.6. Bias Circuit

The bias circuit is used to set the current-flow through the OTAs. With this current the corner frequency of the low-pass filter can be tuned. It is important to supply the same bias voltages to all OTAs to achieve the currect filter function at all corner frequencies. The circuit was derived from the output stage of the OTA.

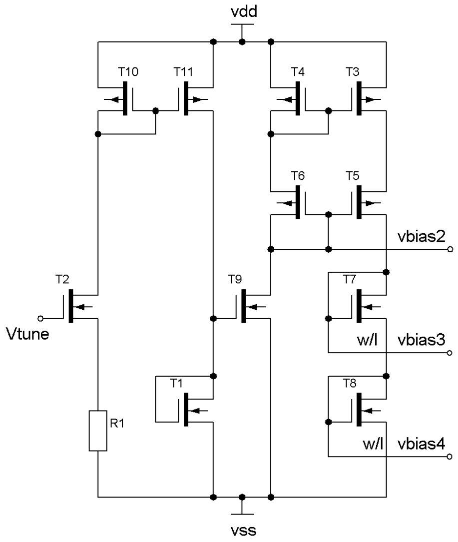

Figure 5: Bias circuit of the OTAs.

The current through transistor T2 can be set by applying the tuning voltage Vtune. This current is mirrored to the cascaded transistors T3, T5, T7 and T8 and sets the bias points for the OTAs. The current set by Vtune flows through the OTAs and sets their transconductance g_m. The different g_m of OTA2 of the biquads resulting from the filter transfer function can only be obtained by proper variation the W/L ratio of the transistors of that OTA.

2.7. Tuning Range of the Filter

By varying the current through the OTAs in a range of 1:10 a tuning range of the corner frequency of about 1:3 can be achieved (Eq. 8). As described earlier the requested tuning range of the filter is 1:12.5 (200 kHz to 2.5 MHz). Additionally switched capacitor arrays are used to cover the whole frequency range. In the design three parallel-circuited capacitors are used, switched by two transistors (Figure 6). From (6) can be derived that the corner frequency is inversely proportional to the capacitance C.

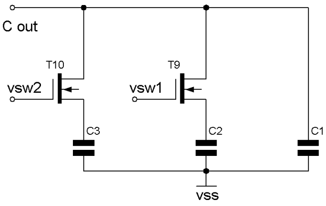

Figure 6: Switched capacitor array.

A capacity ratio of 1:4 extends the filter tuning range to the required value of 1:12. By using three capacitors all corner frequencies between the lower and upper limit can be addressed.

3. SIMULATION RESULTS

In figure 7 the simulated frequency response of the filter is depicted. In order to achieve the needed tuning range capacitors are switched, so that the complete range can be covered. Depending on the used capacitor values also other bandwidth can be achieved. For minimum and maximum capacitance four different tuning voltages are simulated.

The simulated values are obtained at a supply voltage of 2.7 V. For the maximum corner frequency of 2.5 MHz the filter consumes 620 µA whereas the filter can handle input voltages of about 600mVpp.

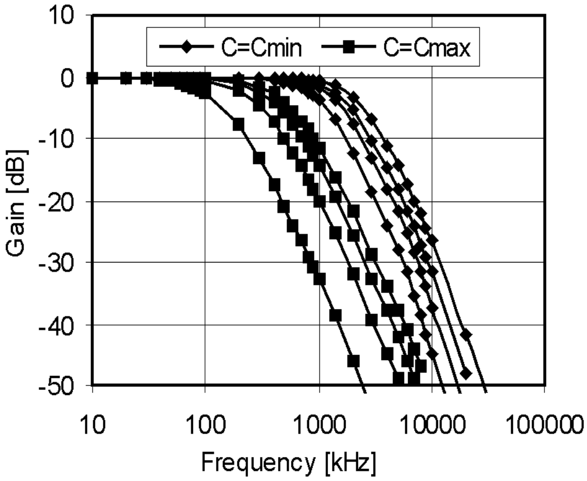

Figure 7: Frequency response of the re-configurable filter.

4. MEASUREMENT RESULTS

Fig. 8 shows the final layout of the filter. In Table 1 the proposed measurement results are summarized.

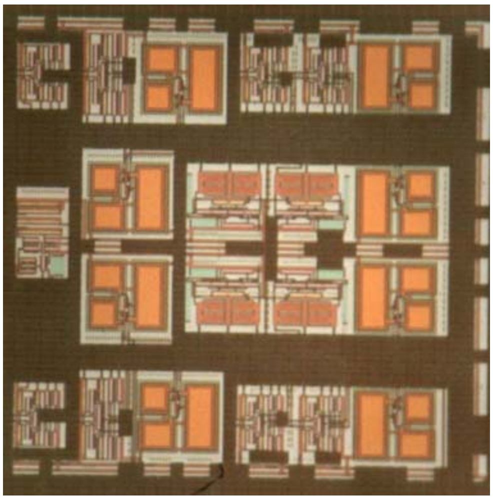

Figure 8: Chip microphotograph of the fully differential IQ filter (chip size 530um x 520um).

Parameter	Value
Tuning Range	200 kHz – 2.5 MHz
Linearity 1 dB Comp.	620 mVpp diff.
Input Referred Noise	$41\text{nV/Hz}^{0.5}$
In Band Ripple	<0.2 dB
Group Delay Ripple @ f_{corner}=2.5 MHz	<120 ns
Current Consumption	<620uA @ 2.7 V

Table 1. Summary of proposed results.

5. CONCLUSION

A fully differential integrated low-pass filter has been implemented in a standard 0.35µm CMOS process. The corner frequency of the filter can be adjusted between 200 kHz and 2.5 MHz by applying a single control voltage. By using the same biasing network for all OTAs of the filter stages the filter shape remains constant while changing the corner frequency. The filter works with a supply voltage of 2.7 V. At f_C = 2.5 MHz the supply current of the filter is 620 µA. The filter can be used as one 2nd order part of the 4th order Butterworth baseband low-pass of a re-configurable communication receiver. The other 2nd order biquad can be easily derived from this biquad by only changing the g_m value of the 2nd OTA.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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